Advanced Micro Devices

Bipolar Microprocessor Logic and Interface Data Book

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Processor (Bit Slice) Devices

Description	Part Number	Number of Pins	Package(s)
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4-Bit Microprocessor Slice, Improved Speed Am2901B.	Am2901C	40 (42)	P, D, (F)
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Status and Shift Control Unit Generates Carry-In to ALU, Contains Shift Linkages, and Stores and Tests ALU Status Flags	Am2904	40 (42)	D, (F)
4-Bit Slice Microprogram Sequencer Slice for Sequencing through Microinstructions in PROM.	Am2911	20	P, D
4-Bit Microprogram Sequencer Slice, Improved Speed Am2911.	Am2911A	20	P, D
4-Bit Microprogram Sequencer Slice. Microsequencer with OR Inputs for Branching	Am2909	28	P, D, F
4-Bit Microprogram Sequencer Slice, Improved Speed Am2909.	Am2909A	28	P, D, F
Microprogram Controller 12-Bit Address Microsequencer with 16 Sequencer Control Instructions	Am2910	40 (42)	D, (F)
Priority Interrupt Expander	Am2913	20	P, D, F
Vectored Priority Interrupt Controller	Am2914	40 (42)	D, (F)
System Clock Generator and Driver Variable Microcycle Length Controller	Am2925	24	D
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Program Control Unit	Am2932	20	D, F
DMA Address Generator	Am2940	28	D, F
Programmable Timer Counter, DMA Address Generator	Am2942	22	D, F
8-Bit Bidirectional I/O Port with Handshake	Am2950/2951	28	D, F
8-Bit Bidirectional I/O Port	Am2952/53	24	D, F
16-Way Branch Control Unit	Am29803A	16	P, D, F
Next Address Control Unit	Am29811A	16	P, D, F

Controller Products

Description	Part Number	Number of Pins	Package(s)
Status and Shift Control Unit Generates Carry-In to ALU. Contains Shift Linkages. Stores and Tests ALU Status Flags	Am2904	40 (42)	D, (F)
Microprogram Controller 12-Bit Address Microsequencer with 16 Sequencer Control Instructions	Am2910	40 (42)	D, (F)
Priority Interrupt Expander	Am2913	20	P, D, F
Vectored Priority Interrupt Controller	Am2914	40 (42)	D, (F)
System Clock Generator and Driver	Am2925	24	D
DMA Address Generator	Am2940	28	D, F
Programmable Timer/Counter, DMA Address Generator	Am2942	22	D, F
8-Bit Bidirectional I/O Port with Handshake	Am2950/2951	28	D, F
8-Bit Bidirectional I/O Port	Am2952/53	24	D, F
Interruptable 8-bit Microprogram Sequencer	Am29112	48	D
16-Bit Bipolar Microprocessor	Am29116	52	D

Package Designations 25, 26, 29, Z81, 93 Series

P – Molded Plastic Package
D – Hermetic DIP Package
F – Hermetic Flat Package

54, 74 Series

J – Hermetic DIP
W – Hermetic Flat
N – Molded Plastic

RAM/PROM

Description	Part Number	Address to Output Access Time (Typ)	Number of Pins	Package(s)
High Speed 1024-Bit RAM	Am2952, Am2953	–		
Noninverting Schottky 64-Bit RAM	Am29700/701	22	16	P, D, F
64-Bit RAM	Am29702/703	22	16	P, D, F
16 Word by 4-Bit 2-Port RAM	Am29705	53	28	P, D, F
16-Word by 4-Bit 2-Port RAM. Improved Speed 29705	Am29705A	–	28	P, D, F
16-Word by 4-Bit 2-Port RAM	Am29707	–	28	P, D, F
Low-Power Schottky 256-Bit RAM	Am29720/721	35	16	P, D, F
256-Bit Generic Series Bipolar PROM	Am29750/751A	25	16	D, F
1024-Bit Generic Series Bipolar PROM	Am29760A/761A	25	16	D, F
2048-Bit Generic Series Bipolar PROM	Am29770/771	30	16	D, F
4096-Bit Generic Series Bipolar PROM	Am29774/775	–	22	D

Dynamic Memory Support Products

Description	Part Number	Data Width	Function	Inv/Non-inverting	Number of Pins	Package(s)
Error Detection and Correction Unit (EDC)	Am2960/ AmZ8160	16	Expandable Hamming Code EDC Slice w/Diagnostics/Initialization and Byte-Level I/O Interface	I to Bus	48	D
EDC Data Bus Buffer	Am2961/ AmZ8161	4	4-Port EDC Interface for RAM, EDC and 24mA I_{OL} Data Bus Drive	I to Bus	24[1]	D
EDC Data Bus Buffer	Am2962/ AmZ8162	4	4-Port EDC Interface for RAM, EDC and 24mA I_{OL} Data Bus Drive	N to Bus	24[1]	D
EDC and Refresh Controller	AmZ8163	–	Memory Timing and Controls for AmZ8160/AmZ8164 (used w/AmZ8127)	–	40	D, P
Dynamic Memory Controller	Am2964B/ AmZ8164B	–	Memory Address Controller w/Refresh Counter, RAS Decoder, CAS Inhibit Buffer	–	40	D, P
Dynamic RAM Driver	Am2965/ AmZ8165	8	RAM Driver w/3-State, Undershoot Protected Outputs	I	20	D, P
Dynamic RAM Driver	Am2966/ AmZ8166	8	RAM Driver w/3-State, Undershoot Protected Outputs	N	20	D, P

Transmission Line Interface

Description	Part Number	t_{PD} ns (Typ)	t_{SKEW} ns (Typ)	V_{HYST} mV (Typ)	V_{TH} mV (Typ)	Diff/ Single-Ended	Output	Number of Pins	Package(s)
Dual Party Line Transceiver	Am26LS27	In Development				D	D, 3S	20	D, P
Dual Party Line Transceiver	Am26LS28					D	D, 3S	20	D, P
Quad RS-423 Line Driver	Am26LS29	120				S	3S	16	D, F, P
Dual/Quad RS-422/423 Line Driver	Am26LS30	120				D/S	TTL	16	D, F, P
Quad RS-422 Line Driver	Am26LS31	12	±2			D	D, 3S	16	D, F, P
Quad RS-422 Line Receiver	Am26LS32	13	±1	100	200	D	3S	16	D, F, P
Quad High V_{CM} Line Receiver	Am26LS33	16	±1	170	500	D	3S	16	D, F, P
Quad Party Line Receiver	Am26LS34	16	±1	170	200	D	3S	16	D, P
Quad Party Line Receiver	Am26LS35	16	±1	170	200	D	3S	16	D, P

Digital Signal Processing Products

Description	Part Number	Output	Number of Pins	Package(s)
8-Bit Serial Parallel Multiplier	Am25LS14/Am54/74LS385	TTL	16	D, F, P
Quad Serial Adder/Subtractor	Am25LS15/Am54/74LS385	TTL	20	D, F, P
8 x 8-Bit Serial/Parallel Multiplier Accumulator	Am25LS2516	3S	40	D
4 x 2-Bit Multiplier	Am25S05	TTL	24	D, F, P
8 x 8-Bit Parallel Multiplier	Am25S557/Am25S558	3S	40	D
Microprogrammable Signal Processor	Am29501	TTL	64	D
16 x 16-Bit Parallel Multiplier	Am29516/Am29517	3S	64	D
Multilevel Pipeline Registers	Am29520/Am29521	3S	24	D
Programmable FFT Address Sequencer	Am29540	3S	40	D

Microcomputer Interface and Support Circuits

Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inv/Non-inverting	Output	Number of Pins	Package(s)
DMA Address Generator	Am2940	24*	0.5	12	N	3S	28	D, F
Programmable Timer/Counter, DMA Address Generator	Am2942	24*	0.5	12	N	3S	22	D, F
8-Bit Bidirectional I/O Port	Am2950/ Am2951	24*	0.5	15	N/I	3S	28	D, F
Octal Bus Transceiver w/T/$\overline{R}$, CD	AmZ8103	24/48	0.5	11	I	3S	20	D, P
Octal Bus Transceiver w/T/$\overline{R}$, CD	AmZ8104	24/48	0.5	14	N	3S	20	D, P
Octal Bus Transceiver wT/$\overline{R}$	AmZ8107	24/48	0.5	11	I	3S	20	D, P
Octal Bus Transceiver w/$\overline{T}$, $\overline{R}$	AmZ8108	24/48	0.5	14	N	3S	20	D, P
Octal Register w/CP, $\overline{CLR}$, $\overline{OE}$, CP Enable	AmZ8120	8.0	0.45	24	N	3S	24[1]	D
8-Bit Equal-to Comparator	AmZ8121	12	0.5	9.0		TTL	20	D, P
AmZ8000 Clock Generator w/Run/Halt, Single-Step, Wait and Timeout Controls	AmZ8127	See Data Sheet					24[1]	D
Octal Latch w/G, $\overline{OE}$	AmZ8133	24	0.5	15	I	3S	20	D, P
3-to-8 Decoder w/Control Storage	AmZ8136	24	0.5	30		3S	20	D, P
Octal Bus Driver w/$\overline{OE}$, $\overline{OE}$	AmZ8140	48	0.55	9.0	I	3S	20	D, P
Octal Bus Driver w/$\overline{OE}$, $\overline{OE}$	AmZ8144	48	0.55	11	N	3S	20	D, P
3-to-8 Chip Select Decoder w/$\overline{ACK}$	AmZ8148	8.0	0.45	19		TTL	20	D, P
Octal Latch w/G, $\overline{OE}$	AmZ8173	24	0.5	12	N	3S	20	D, P
Octal Input/Output Port	8212	15	0.45	12	N	3S	24	D, P
Quad Bidirectional Bus Driver	8216	50	0.6	15	N	3S	16	D, P
Clock Generator/Driver	8224	15	0.45			8080 Levels	16	D, P
Quad Bidirectional Bus Driver	8226	50	0.6	15	I	3S	16	D, P
System Controller	8228	2/10	0.45	15-30	Generates 8080 Control and Data Bus Interface		28	D, P
System Controller	8238	2/10	0.45	15-30			28	D, P

Note: 1. 24-pin, 0.3" wide package.

*Commercial version only.

Registers and Latches

Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inverting/ Noninverting	Output	Number of Pins	Package(s)
Hex Register, Common Enable	Am25LS07	8.0	.45	13	N	TTL	16	D, F, P
Hex Register, Common Enable	Am25S07	20	0.5	11	N	TTL	16	D, F, P
Hex Register, Common Enable	54/74S378	20	0.5	11	N	TTL	16	J, W, N
Quad Register, Common Enable	Am25LS08	8.0	0.45	13	N/I	TTL	16	D, F, P
Quad Register, Common Enable	Am25S08	20	0.5	11	N/I	TTL	16	D, F, P
Quad Register, Common Enable	54/74S379	20	0.5	11	N/I	TTL	16	J, W, N
Quad Register, Multiplexer Inputs	Am25LS09	8.0	0.45	13	N	TTL	16	D, F, P
Quad Register, Multiplexer Inputs	Am25S09	20	0.5	11	N	TTL	16	D, F, P
Quad Register, Multiplexer	54/74S399	20	0.5	11	N	TTL	16	J, W, N
Octal Serial/Parallel Register	Am25LS22/ 54/74LS322	8.0	0.45	18	N	3S	20	D, F, P
Octal Shift Register, SYN $\overline{CLR}$	Am25LS23/ 54/74LS323	8.0	0.45	23	N	3S	20	D, F, P
Octal Register w/CP and $\overline{CLR}$	Am25LS273	8.0	0.45	15	N	TTL	20	D, F, P
Octal Register w/CP and $\overline{CLR}$	54/74LS273	8.0*	0.5	18	N	TTL	20	D, F, P
Octal Register w/CP, $\overline{CLR}$ (Buffered Outputs)	Am25LS273B	8.0	0.45	25	N	TTL	20	D, F, P
Octal Shift Register, Asyn $\overline{CLR}$	Am25LS299	8.0	0.45	22	N	3S	20	D, F, P
Octal Shift Register, Asyn $\overline{CLR}$	54/74LS299	8.0*	0.5	–	N	3S	20	J, W, N
Octal Latch w/G, $\overline{OE}$	Am25LS373	24	0.5	20	N	3S	20	D, F, P
Octal Latch w/G, $\overline{OE}$	54/74LS373	24*	0.5	20	N	3S	20	D, F, P
Octal Latch w/G, $\overline{OE}$	Am25S373	32	0.5	12	N	3S	20	D, F, P
Octal Latch w/G, $\overline{OE}$	54/74S373	20	0.5	12	N	3S	20	D, F, P
Octal Register w/CP, $\overline{OE}$	Am25LS374A	24	0.5	15	N	3S	20	D, F, P
Octal Register w/CP, $\overline{OE}$	54/74LS374	24*	0.5	22	N	3S	20	D, F, P
Octal Register w/CP, $\overline{OE}$	Am25S374	32	0.5	11	N	3S	20	D, F, P
Octal Register w/CP, $\overline{OE}$	54/74S374	20	0.5	11	N	3S	20	D, F, P
Octal Register w/CP, CP Enable	Am25LS377	8.0	0.5	14	N	TTL	20	D, F, P
Octal Register w/CP, CP Enable	54/74LS377	8.0*	0.5	18	N	TTL	20	D, F, P
Octal Register w/CP, CP Enable (Buffered Outputs)	Am25LS377B	8.0	0.5	23	N	TTL	20	D, F, P
Octal latch w/G, $\overline{OE}$	Am25LS533	24	0.5	20	I	3S	20	D, F, P
Octal Latch w/G, $\overline{OE}$	54/74LS533	24*	0.5	20	I	3S	20	D, F, P
Octal Latch w/G, $\overline{OE}$	Am25S533	32	0.5	14	I	3S	20	D, F, P
Octal Latch w/G, $\overline{OE}$	54/74S533	20	0.5	19	I	3S	20	D, F, P
Octal Register w/CP, $\overline{OE}$	Am25LS534	24	0.5	15	I	3S	20	D, F, P
Octal Register w/CP, $\overline{OE}$	54/74LS534	24*	0.5	22	I	3S	20	D, F, P
Octal Register w/CP, $\overline{OE}$	Am25S534	32	0.5	11	I	3S	20	D, F, P
Octal Register w/CP, $\overline{OE}$	54/74S534	20	0.5	11	I	3S	20	D, F, P
Quad Register	Am25LS2518/ 54/74LS388	12	0.5	18	N	TTL/3S	16	D, F, P
Quad Register	Am25S18/ 2918	20	0.5	6.0	N	TTL/3S	16	D, F, P
Quad Register Dual Outputs	Am25LS2519/ Am2919	12	0.5	20	N/I	3S	20	D, F, P

*Commercial version only.

Registers and Latches (Cont.)

Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inverting/ Noninverting	Output	Number of Pins	Package(s)
Octal Register w/CP, $\overline{CLR}$, $\overline{OE}$, CP Enable	Am25LS2520	8.0	0.45	24	N	3S	22	D, F, P
Quad Register	Am29LS18	12	0.5	18	N	TTL/3S	16	D, F, P
Octal Register w/CP, $\overline{CLR}$, $\overline{OE}$ CP Enable	Am2920	8.0	0.45	24	N	3S	22	D, F, P
8-Bit Bidirectional I/O Port	Am2950/51	24	0.5	15	I/N	3S	28	D, F
Octal Register w/CP, $\overline{OE}$	Am2954	32	0.5	11	N	3S	20	D, F, P
Octal Register w/CP, $\overline{OE}$	Am2955	32	0.5	11	I	3S	20	D, F, P
Octal Register w/G, $\overline{OE}$	Am2956	32	0.5	9.0	N	3S	20	D, F, P
Octal Latch w/G, $\overline{OE}$	Am2957	32	0.5	14	I	3S	20	D, F, P

*74LS only, see data sheet for 54LS application.

Transceivers

Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inverting/ Noninverting	Output	Number of Pins	Package(s)
Octal Transceiver w/T/$\overline{R}$, CD	Am2946	24/48	0.5	11	I	3S	20	D, P
Octal Transceiver w/T/$\overline{R}$, CD	Am2947	24/48	0.5	14	N	3S	20	D, P
Octal Transceiver w/$\overline{T}$/$\overline{R}$	Am2948	24/48	0.5	11	I	3S	20	D, P
Octal Transceiver w/$\overline{T}$/$\overline{R}$	Am2949	24/48	0.5	14	N	3S	20	D, P
Quad IEEE-488 Transceiver	3448A	48	0.5	12	N	3S/OC	16	D, P
Quad Transceiver w/$\overline{OE}$, OE	Am25LS242	48	0.55	12	I	3S	20	D, F, P
Quad Transceiver w/$\overline{OE}$, OE	54/74LS242	24*	0.5	12	I	3S	20	D, F, P
Quad Transceiver w/$\overline{OE}$, OE	54/74S242	64	0.55	4.5	I	3S	20	D, P
Quad Transceiver w/$\overline{OE}$, OE	Am25LS243	48	0.55	12	N	3S	20	D, F, P
Quad Transceiver w/$\overline{OE}$, OE	54/74LS243	24*	0.5	12	N	3S	20	D, F, P
Quad Transceiver w/$\overline{OE}$, OE	54/74S243	64	0.55	6.0	N	3S	20	D, P
Octal Transceiver w/T/$\overline{R}$, CD	73/8303	16/48	0.5	11	I	3S	20	D, P
Octal Transceiver w/T/$\overline{R}$, CD	73/8304B	16/48	0.5	14	N	3S	20	D, P
Octal Transceiver w/$\overline{T}$/$\overline{R}$	73/8307	16/48	0.5	11	I	3S	20	D, P
Octal Transceiver w/$\overline{T}$/$\overline{R}$	73/8308	16/48	0.5	14	N	3S	20	D, P

*74LS only, see data sheet for 54LS specification.

3-Port Transceivers

Quad Transceiver	Am26S10	100	0.8	10	I to Bus	3S	16	D, F, P
Quad Transceiver	Am26S11	100	0.8	12	N to Bus	3S	16	D, F, P
Quad Transceiver, V_{HYST} (Rcvr) = 0.6V	Am26S12	100	0.85	14	I	3S	16	D, F, P
Quad Transceiver V_{HYST} (Rcvr) = 1.05V	Am26S12A	100	0.85	14	I	3S	16	D, F, P
Quad 2-Input Transceiver w/3S Rcvr	Am2905	100	0.8	21	I	OC	24	D, F, P
Quad 2-Input Transceiver w/Parity	Am2906	100	0.8	21	I	OC	24	D, F, P
Quad Transceiver w/3S Rcvr and Parity	Am2907	100	0.8	21	I	OC	20	D, F, P
Quad Transceiver w/3S Rcvr and Parity (DEC Compatible)	Am2908	100	0.8	21	I	OC	20	D, F, P

*Commercial version only.

3-Port Transceivers (Cont.)

Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inverting/ Noninverting	Output	Number of Pins	Package(s)
Quad Transceiver	Am2912	100	0.8	10	I	3S	16	D, F, P
Quad 2-Input Transceiver w/3S Rcvr	Am2915A	48	0.5	21	I	3S	24	D, F, P
Quad 2-Input Transceiver w/Parity	Am2916A	48	0.5	21	I	3S	24	D, F, P
Quad Transceiver w/3S Rcvr and Parity	Am2917A	48	0.5	21	I	3S	24	D, F, P
Quad Transceiver	Am2926	48	0.5	10	I	3S	16	D, P
Quad Transceiver w/Clock Enable (Latched Output)	Am2927	48	0.5	18	I	3S	20	D, F, P
Quad Transceiver w/Clock Enable (Register Output)	Am2928	48	0.5	18	I	3S	20	D, F, P
Quad Transceiver	Am2929	48	0.5	13	N	3S	16	D, P
Quad Transceiver	8T26A	48	0.5	10	I	3S	16	D, P
Quad Transceiver	8T28	48	0.5	13	N	3S	16	D, P

Drivers/Buffers

Octal Driver w/$\overline{OE}$, $\overline{OE}$	Am25LS240	48	0.55	12	I	3S	20	D, F, P
Octal Driver w/$\overline{OE}$, $\overline{OE}$	54/74LS240	24*	0.5	12	I	3S	20	D, F, P
Octal Driver w/$\overline{OE}$, $\overline{OE}$	Am25S240	64	0.55	4.5	I	3S	20	D, P
Octal Driver w/$\overline{OE}$, $\overline{OE}$	54/74S240	64	0.55	4.5	I	3S	20	D, P
Octal Driver w/$\overline{OE}$, OE	Am25LS241	48	0.55	12	N	3S	20	D, F, P
Octal Driver w/$\overline{OE}$, OE	54/74LS241	24*	0.5	12	N	3S	20	D, F, P
Octal Driver w/$\overline{OE}$, OE	Am25S241	64	0.55	6.0	N	3S	20	D, P
Octal Driver w/$\overline{OE}$, OE	54/74S241	64	0.55	6.0	N	3S	20	D, P
Octal Driver w/$\overline{OE}$, $\overline{OE}$	Am25LS244	48	0.55	12	N	3S	20	D, F, P
Octal Driver w/$\overline{OE}$, $\overline{OE}$	54/74LS244	24*	0.5	12	N	3S	20	D, F, P
Octal Driver w/$\overline{OE}$, $\overline{OE}$	Am25S244	64	0.55	6.0	N	3S	20	D, P
Octal Driver w/$\overline{OE}$, $\overline{OE}$	54/74S244	64	0.55	6.0	N	3S	20	D, P
Octal Driver w/$\overline{OE}$, $\overline{OE}$	Am2958	64	0.55	4.5	N	3S	20	D, P
Octal Driver w/$\overline{OE}$, $\overline{OE}$	Am2959	64	0.55	6.0	I	3S	20	D, P
Octal Buffer w/$\overline{G}1$, $\overline{G}_2$	71/81LS95	16	0.5	15	N	3S	20	D, P
Octal Buffer w/$\overline{G}_1$, $\overline{G}_2$	71/81LS96	16	0.5	13	I	3S	20	D, P
Octal Buffer w/$\overline{G}_1$ $\overline{G}_2$	71/81LS97	16	0.5	15	N	3S	20	D, P
Octal Buffer w/$\overline{G}_1$, $\overline{G}_2$	71/81LS98	16	0.5	13	I	3S	20	D, P

*74LS only, see data sheet for 54LS specification.

Counters

Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Output	Number of Pins	Package(s)
BCD Decade Up/Down Counter	Am25LS2568/ 54/74LS568	8.0	0.45	13	3S	20	D, F, P
4-Bit Binary Up/Down Counter	Am25LS2569/ 54/74LS569	8.0	0.45	13	3S	20	D, F, P
BCD Decade Counter	54/74S160	20	0.5	6.0	TTL	16	D, F, P
4-Bit Binary Counter Async Clear	54/74S161	20	0.5	6.0	TTL	16	D, F, P
4-Bit Binary Counter Sync Clear	54/74S163	20	0.5	6.0	TTL	16	D, F, P
4-Bit BCD Counter	93S10	20	0.5	6.0	TTL	16	D, F, P
4-Bit Binary Counter	93S16	20	0.5	6.0	TTL	16	D, F, P
Progammable Timer/Counter	Am2942*	24	0.5	13		22	D, F

*Commercial version only.

Operators

Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inverting/ Noninverting	Output	Number of Pins	Package(s)
4-Bit ALU/Function Generator	Am25LS381	8.0	0.15	14	N	TTL	20	D, F, P
4-Bit ALU/Function Generator	54/74LS381	8.0*	0.5	14	N	TTL	20	D, F, P
4-Bit ALU/Function Generator	Am25LS2517/8 54/74LS382	8.0	.45	14	N	TTL	20	D, F, P
8-Bit Comparator	Am25LS2521	12	.5	9.0	I	TTL	20	D, F, P
4-Bit Shifter	Am25S10	20	0.5	5.0	N	3S	16	D, F, P
4-Bit Shifter	54/74S350	20	0.5	5.0	N	3S	16	D, F, P
Look-ahead Carry Generator	Am2902A	20	0.5	6.5	N	TTL	16	D, F, P
Twelve Input Parity Checker/Generator	93S48	20	0.5	19	N	TTL	16	D, F, P

Decoders/Demultiplexers, Multiplexers, Priority Encoders

Priority Encoder	Am25LS2513	12	0.5	11	N	3S	20	D, F, P
8-Input Multiplexer, Control Storage	Am25LS2535/ Am2922	20	0.5	16	N/I	3S	20	D, F, P
8-Bit Decoder Control Storage	Am25LS2536	24*	0.5	20	N	3S	20	D, F, P
One-of-Ten Decoder	Am25LS2537	12	0.5	17	N/I	3S	20	D, F, P
One-of-Eight Decoder	Am25LS2538/ Am2921	12	0.5	15	N/I	3S	20	D, F, P
Dual One-of-Four Decoder	Am25LS2539	12	0.5	17	N/I	3S	20	D, F, P
Chip Select Address Decoder	Am25LS2548	8.0	0.45	14	I	TTL	20	D, F, P
8-Input Multiplexer	Am2923	20	0.5	12	N/I	TTL/3S	16	D, F, P
3-Line to 8-Line Decoder/ Multiplexer	Am2924	20	0.5	4.5	I	TTL	16	D, F, P

One-Shots

Retriggerable, Resettable, Monostable Multivibrator	Am26S02	20	0.5	28	N OR I	TTL	16	D, F, P

Note: 1. New 24-pin, 0.3" wide package.

*Commercial version only.

APPLICATION NOTE INDEX

INTRODUCTION TO ADVANCED MICRO DEVICES HIGH PERFORMANCE SCHOTTKY AND LOW-POWER SCHOTTKY MSI/LSI PRODUCTS

DESIGNER'S GUIDE TO HIGH PERFORMANCE LOW-POWER SCHOTTKY LOGIC

By David A. Laws and Roy J. Levy.

1

Advanced Micro Devices is a leading supplier of low-power Schottky MSI and LSI devices. Two basic families of product are offered:

AM54/74LS Series

- Typical tpd 10ns/gate at 2mW
- Typical Register fmax = 40MHz

Pin for pin and electrical alternate source devices to the standard performance LS logic family.

AM25LS Series

- Typical tpd 5ns/gate at 2mW
- Typical Register fmax = 65MHz

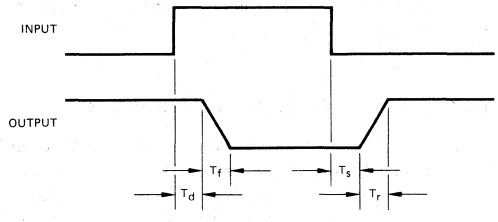
Advanced Micro Devices' proprietary high performance LS logic family. This includes both original designs and enhanced specification versions of the AM54/74LS devices. Improvements include twice the fan-out over the military temperature range, higher noise margin and faster switching speeds.

THE SCHOTTKY DIODE STRUCTURE

The major components of switching delays in digital integrated circuits are listed in Figure 1. One of the most significant of these is the storage time constant of a transistor driven into saturation Ts. Older TTL circuits minimized this parameter with a process technique known as gold doping. This increased the rate of recombination of charge stored in the base region.

The desired result of improved speed was achieved. Unfortunately it also reduced available design β at low temperatures and was marginally effective when hot. This resulted in lowered performance over the full military temperature range.

The development of the Schottky diode provides a more effective solution. A feature of the Schottky diode is its lower forward voltage at a given current level compared to a diffused (P-N) diode of the same area, Figure 2. Connecting a Schottky diode between the base and collector of a transistor, Figure 3, will shunt excess base current drive from the base to the collector, once the collector drops to a low enough voltage to forward bias the Schottky. This prevents the build up of stored charge and eliminates the Ts component of the delay.



PARAMETERS	DETERMINING FACTORS
$\frac{T_d}{T_f}$	R, C β, Cob, Base Drive, Signal Amplitude
T_s	Storage Time Constant of a Saturated Transistor
T_r	Cob, Signal Amplitude

Figure 1. Major Causes of Propagation Delay.

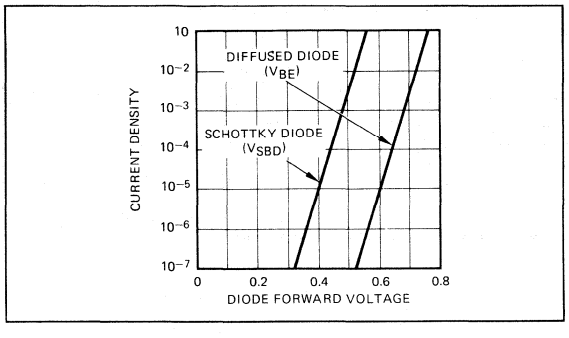


Figure 2. Comparison of V_F for Schottky and Diffused Diodes.

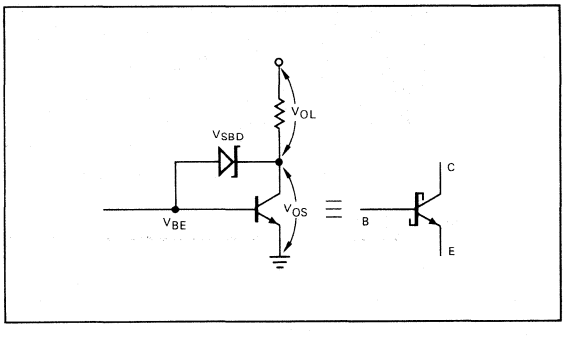


Figure 3. Schottky Clamped Transistor and its Conventional Circuit Symbol.

A Schottky diode is formed at a metal to semiconductor junction when the semiconductor doping is at the level normally found in the collector region of TTL devices. A Schottky-clamped transistor is constructed by extending the metal contact for the base region over the collector as shown in Figure 4. The same metallization structure forms a simple ohmic contact at the base, collector and emitter contact windows because of the higher doping levels in the silicon at these locations.

The selection of the forward voltage drop across the Schottky diode, V_{SBD}, is a compromise between a high value to insure a minimum V_{OL} but low enough to prevent charge storage in the base. Platinum silicide Schottky diodes provide this optimum voltage drop. Platinum is deposited and platinum-silicide is formed by sintering and annealing. As aluminum has a high affinity for silicon, in order to prevent the aluminum interconnect metallization from diffusing through the platinum material, with resulting lower V_{SBD}, a barrier of tungsten-titanium is evaporated after the platinum and before the aluminum metallization. This structure has been extensively evaluated and proven to have excellent reliability characteristics. It is now widely employed in the manufacture of Schottky devices. Reliability data is available from Advanced Micro Devices on request.

CHARACTERISTICS OF SCHOTTKY DEVICES

The primary reason for the development of Schottky devices was to improve AC (switching) performance and the first integrated circuits to employ this technique offered propagation delays as fast as 3ns. However, their fast rise and fall times and high power requirements have restricted their application to highest performance systems. It was realized that the technique could be used to decrease the charging current required to achieve the 10ns speed specification of older TTL gates. This insures considerably lower operating power requirements. The resulting family of devices are known as Low-Power Schottky (LS) circuits.

2. D.C. Circuit Characteristics

CIRCUIT CONFIGURATIONS

The basic circuit design configuration of a Low-Power Schottky gate is similar to that of the original standard TTL elements. However, certain refinements have been made to optimize device performance when fabricated with the LS process.

In order to analyze the circuit configuration, Table 1 shows terms used in describing Advanced Micro Devices' LS circuits:

TABLE 1
D.C. CIRCUIT PARAMETER DEFINITIONS

I_{IL}	The current out of an input at a specified LOW voltage.
I_{IH}	The current into an input at a specified HIGH voltage.
I_{OL}	The current into an output when in the LOW state.
I_{OH}	The current out of an output when in the HIGH state (pull-up circuit only).
I_{SC}	The current out of an output in the HIGH state when shorted to ground. (Also called I_{OS})
V_{CC}	The range of supply voltage over which the device is guaranteed to operate.
V_{IL}	The guaranteed maximum input voltage that will be recognized by the device as a logic LOW.
V_{IH}	The guaranteed minimum input voltage that will be recognized by the device as a logic HIGH.
V_{OL}	The maximum guaranteed logic LOW voltage at the output terminal while sinking the specified load current I_{OL}.
V_{OH}	The minimum guaranteed logic HIGH voltage at the output terminal when sourcing the specified source current I_{OH}.
I_{OZH}	Three-state off-state output current, high level voltage applied.
I_{OZL}	Three-state off-state output current, low-level voltage applied.

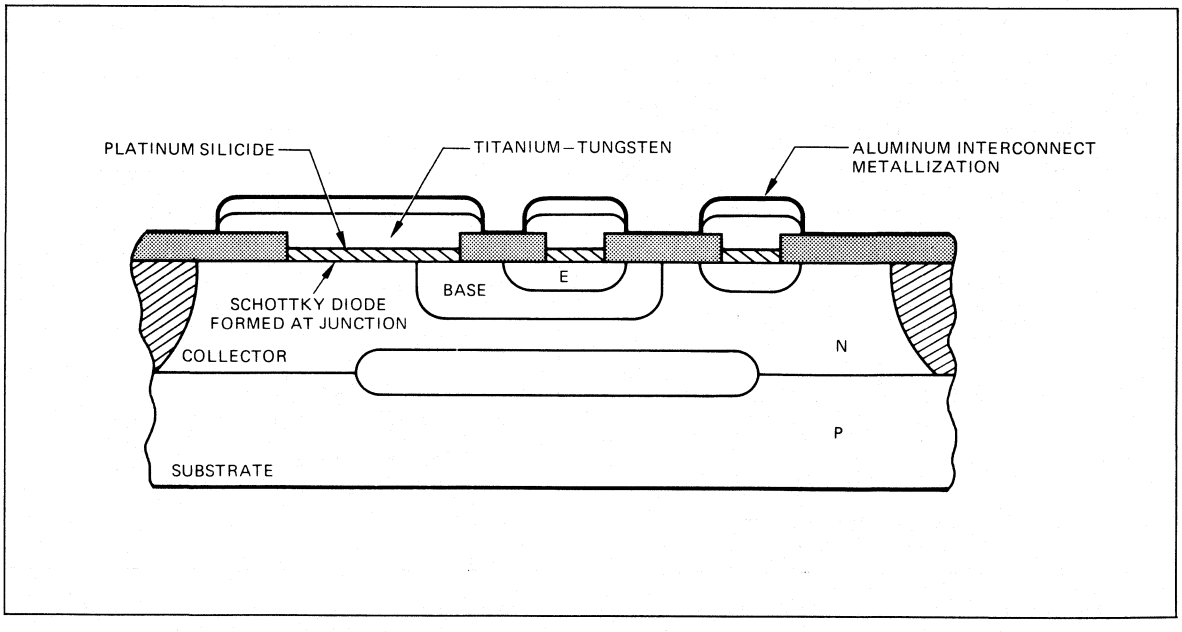


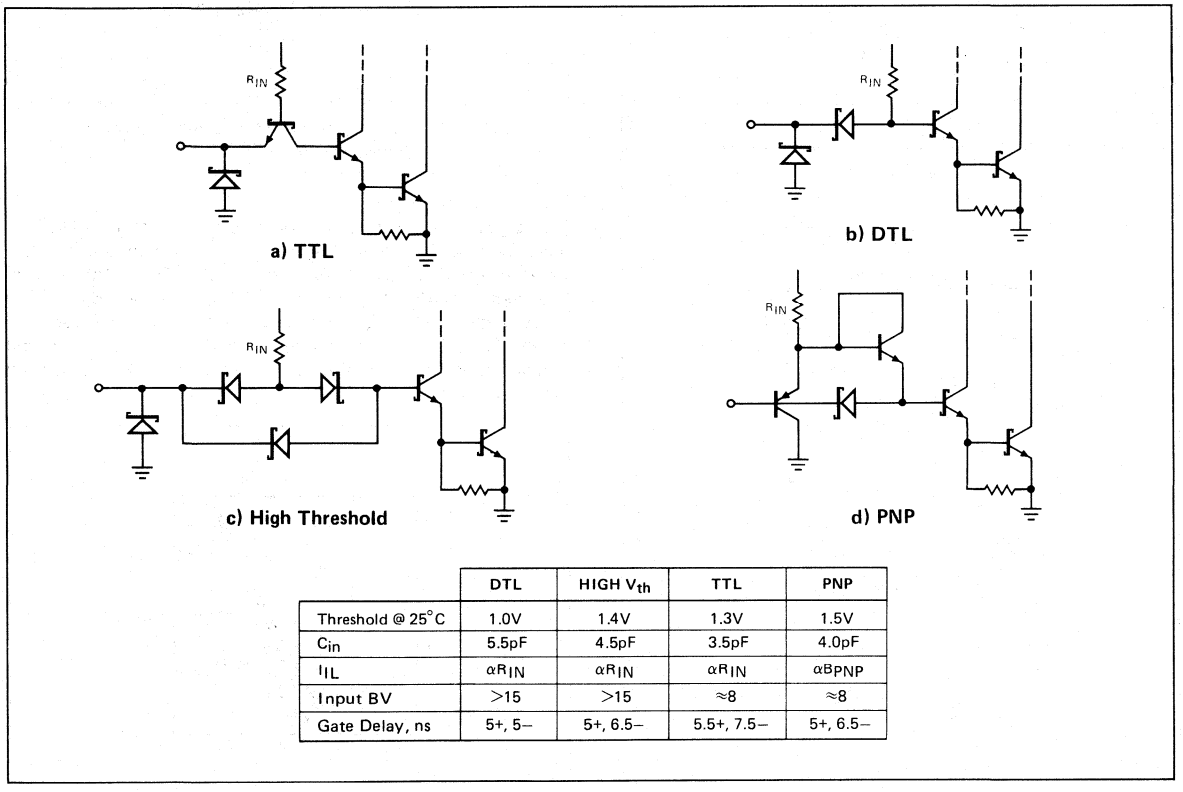
Figure 4. Schottky Diode Clamped Transistor Structure.

Both the input and output structures of the LS devices themselves have evolved through a number of configurations as designers have attempted to optimize circuit performance.

Depending on the function of the device any one of four commonly used inputs may be employed. The significant characteristics of each of these configurations are summarized in Figure 5.

The first LS designs used the familiar multi-emitter TTL input of Figure 5a. However because of low breakdown voltage and slow speed it is now used only where the geometry offers a significant advantage in circuit mask layout.

The second and still most widely used structure is the simple DTL style input of Figure 5b. This is the fastest version and it has good input breakdown voltage. In output functions having only a single gate delay between input and output, such as a three-state enable input, the low threshold of the DTL configuration causes the output node to be at a sufficiently low voltage to risk leakage problems at high temperature. The input of Figure 5c raises the threshold by one diode to overcome this problem (Figure 6). However because it is slower and uses more silicon area, its use is limited to special situations. A PNP input, Figure 5d, insures low d.c. loading for devices with common input/output pins such as the Am25LS23. However it is slow and has low breakdown voltage, comparable to the multi-emitter TTL structure.



	DTL	HIGH V_{th}	TTL	PNP
Threshold @ 25°C	1.0V	1.4V	1.3V	1.5V
C_{in}	5.5pF	4.5pF	3.5pF	4.0pF
I_{IL}	αR_{IN}	αR_{IN}	αR_{IN}	α_{BPNP}
Input BV	>15	>15	≈8	≈8
Gate Delay, ns	5+, 5–	5+, 6.5–	5.5+, 7.5–	5+, 6.5–

Figure 5. Low-Power Schottky Input Configurations.

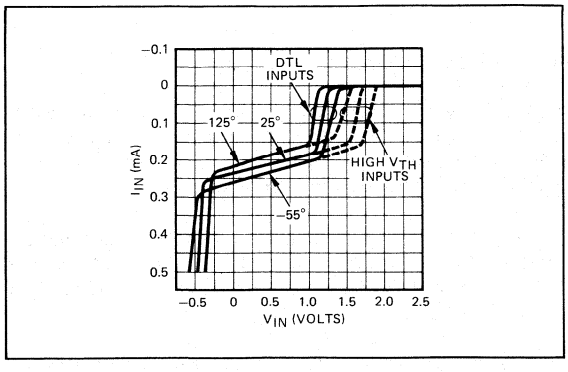


Figure 6. LS Input Characteristics for DTL and High Threshold Inputs.

Figure 7 compares the early LS output configuration with the design most frequently used today. The change was made to provide clamping of positive ringing and to allow the higher I_{SC} currents now specified (see section 3). The typical V_{OH} versus I_{OH} curves of Figure 8 are similar for both versions.

This example displays an I_{SC} of approximately 35mA. Note that both of these designs include the "squaring" network (R_3, R_4 and Q_5) at the base of the output pulldown transistor, Q_4, which was not included on standard TTL families. The result of this is a sharp transition of V_{OUT} with V_{IN} shown in Figure 9 for a simple gate function.

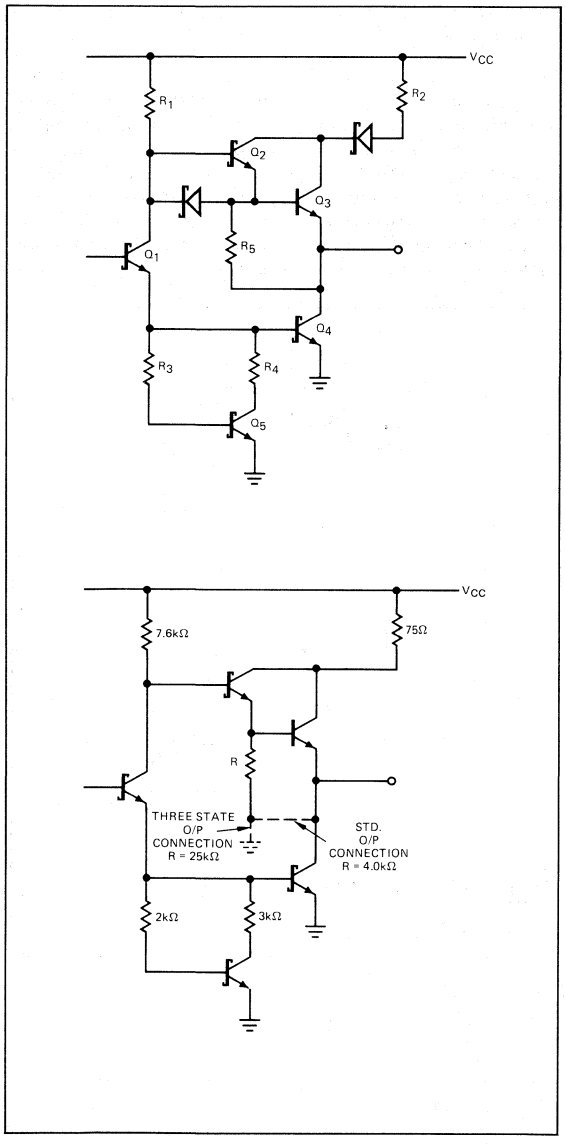


Figure 7. Low-Power Schottky Output Configurations.

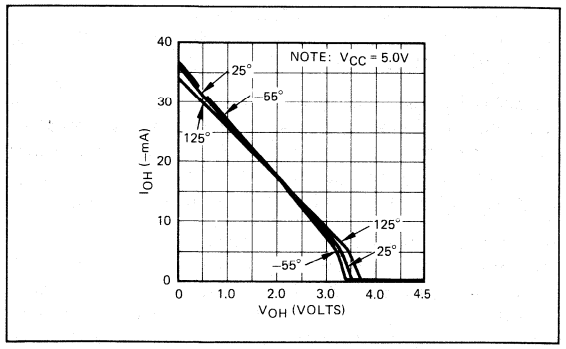


Figure 8. Typical V_{OH} Versus I_{OH} for Low-Power Schottky.

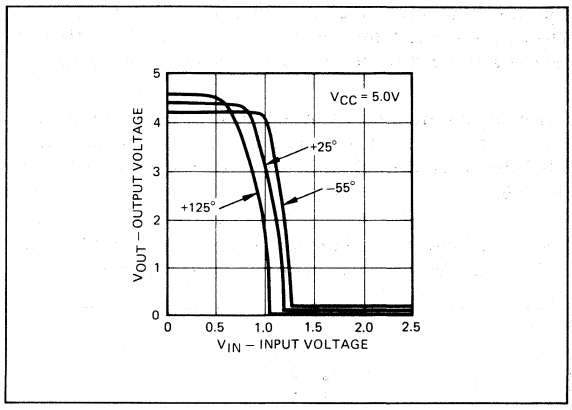


Figure 9. Typical Output Versus Input Voltage Characteristic.

The typical V_{OL} versus I_{OL} output characteristics of LS devices are shown in Figure 10. Most 74LS functions are specified at V_{OL} = 0.4V at I_{OL} = 4mA and 0.5V at 8mA. Am25LS are specified at 0.45V for I_{OL} = 8mA. Some newer designs are being guaranteed at I_{OL} of 12mA and 24mA. This curve indicates that lack of β at low temperature will not permit existing designs to be guaranteed to these higher values without severe yield loss.

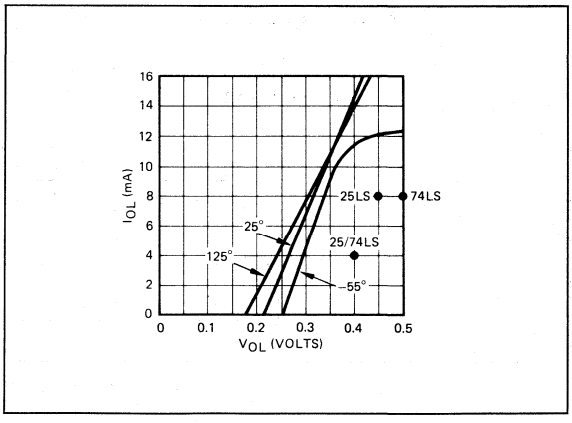


Figure 10. Typical LS V_{OL} Versus I_{OL} Characteristics.

INPUT/OUTPUT LEVELS

Table 2 shows the guaranteed d.c. parameters of the Am54LS/74LS and second generation Am25LS families. Input current requirements (I_{IH}, I_{IL}) and therefore output drive needs (I_{OH}, I_{OL}) are significantly reduced over older TTL.

A one unit load input current at logic HIGH, I_{IH}, for Am54LS/74LS is 20μA, compared with 40μA for Am54/74 standard TTL. Similarly at logic LOW, I_{IL} is reduced to –0.36mA from –1.6mA.

Corresponding reductions in the output drive requirements are I_{OL} = 4mA vs. 16mA at V_{OL} = 0.4V and I_{OH} = –400μA compared to 800μA.

TABLE 2
COMPARISON OF TTL DC PARAMETERS

Parameters	54LS/74LS LOW-POWER SCHOTTKY Conditions		Min.	Typ.	Max.	25LS LOW-POWER SCHOTTKY Conditions		Min.	Typ.	Max.	Units
V_{OL}	I_{OL} = 4.0mA				0.4	I_{OL} = 4.0mA				0.4	V
	I_{OL} = 8.0mA (COM'L Only)				0.5	I_{OL} = 8.0mA (MIL, COM'L)				0.45	
V_{OH}	I_{OH} = −400μA	MIL	2.5	3.4		I_{OH} = −440μA	MIL	2.5	3.4		V
		COM'L	2.7	3.4			COM'L	2.7	3.4		
V_{IL}	Logic LOW	MIL			0.7	Logic LOW	MIL			0.7	V
		COM'L			0.8		COM'L			0.8	
V_{IH}	Logic HIGH		2.0			Logic HIGH		2.0			V
I_{IL}	V_{IN} = 0.4V				−0.36	V_{IN} = 0.4V				−0.36	mA
I_{IH}	V_{IN} = 2.7V				20	V_{IN} = 2.7V				20	μA

Parameter	54S/74S AND 25S SCHOTTKY TTL Condition		Min.	Typ.	Max.	STANDARD TTL Condition	Min.	Typ.	Max.	Units
V_{OL}	I_{OL} = 20mA			0.3	0.5	I_{OL} = 16mA		0.2	0.4	Volts
V_{OH}	I_{OH} = −1.0mA	MIL	2.5	3.4		I_{OH} = −300μA	2.4	3.4		Volts
		COM'L	2.7	3.4						
V_{IL}	Logic LOW				0.8	Logic LOW			0.8	Volts
V_{IH}	Logic HIGH		2.0			Logic HIGH	2.0			Volts
I_{IL}	V_{IN} = 0.5V				−2.0	V_{IN} = 0.4V			−1.6	mA
I_{IH}	V_{IN} = 2.7V				50	V_{IN} = 2.4V			40	μA

FAN-OUT CAPABILITY

The fan-out capability of a logic family indicates the number of inputs which can be driven by a single output. It is defined as the maximum output drive current divided by the input current available.

Logic HIGH Fan-out = I_{OH}/I_{IH}
Logic LOW fan-out = I_{OL}/I_{IL}

Table 3 shows the fan-out capabilities of typical functions from the three families. The lower current operating levels of LS devices allow them to be specified at a logic LOW fan-out over the commercial range of more than twice that of standard TTL (22 vs. 10). The Am25LS family allows this advantage to be extended to the military range.

D.C. NOISE MARGIN

The D.C. noise margins of a digital system are defined from Figure 11 as follows:

Logic HIGH Noise Margin = $V_{OH1} - V_{IH2}$
Logic LOW Noise Margin = $V_{IL2} - V_{OL1}$

These parameters for LS devices are shown in Table 2. LS has a minimum logic HIGH output voltage of V_{OH} = 2.5V for military and 2.7V for the commercial temperature range. For standard TTL, V_{OH} is 2.4V. V_{IH} is 2.0V for both families.

Table 3 compares the guaranteed noise margin values for the standard TTL and LS devices. LS devices offer improved margin over standard TTL in the logic HIGH state, which is the most critical with regard to noise generation. At a similar fan-out, 10 for standard TTL and 11 for LS, noise margins in the LOW state are the same over the commercial range.

Military LS devices have a 100mV lower noise margin in the LOW state than standard TTL. In most systems, this does not present a problem as the lower power supply currents being switched with LS generally result in lower system noise generation.

The logic levels guaranteed over the operating temperature ranges are of course worst case. Figures 12 and 13 show the typical values to be considerably better than these.

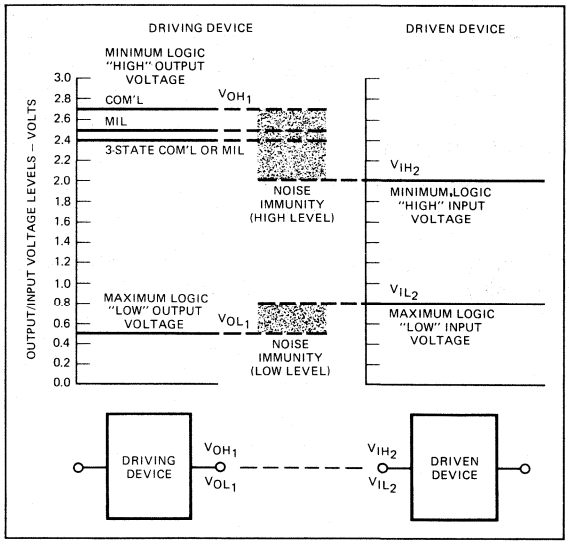


Figure 11. Input/Output Voltage Interface Conditions.

TABLE 3
FAN-OUT AND NOISE MARGIN
COMPARISON OF TTL AND LS FAMILIES.

a) LOGIC "HIGH" STATE

FAMILY	INPUT CURRENT I_{IH}	OUTPUT CURRENT I_{OH}	FAN-OUT		NOISE MARGIN	
			MILITARY	COMMERCIAL	MILITARY	COMMERCIAL
54/74	40μA	−800μA	20	20	400mV	400mV
54LS/74LS	20μA	−400μA	20	20	500mV	700mV
25LS	20μA	−440μA	22	22	500mV	700mV

b) LOGIC "LOW" STATE

FAMILY	INPUT CURRENT I_{IL}	OUTPUT CURRENT I_{OL}	FAN-OUT		NOISE MARGIN	
			MILITARY	COMMERCIAL	MILITARY	COMMERCIAL
54/74	−1.6mA	16mA	10	10	400mV	400mV
54LS/74LS	−0.36mA	4mA	11	11	300mV	400mV
		8mA	No Spec.	22	No Spec.	300mV
25LS	−0.36mA	4mA	11	11	300mV	400mV
		8mA	22	22	250mV	350mV

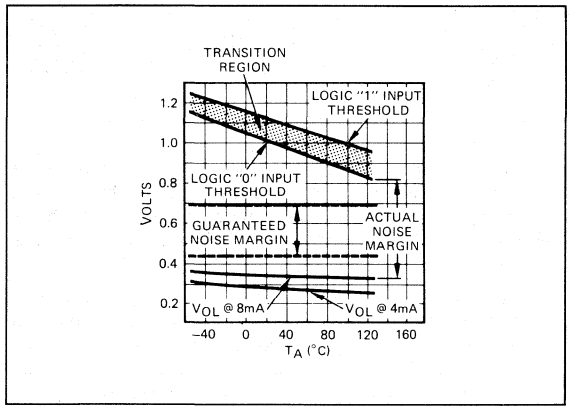


Figure 12. LS Logic "0" Noise Margin.

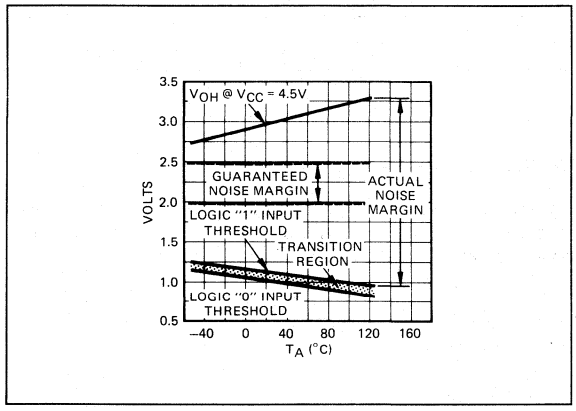


Figure 13. LS Logic "1" Noise Margin.

Am25LS D.C. FEATURES

The D.C. advantages offered by second generation Am25LS over 54/74LS devices can be seen from Table 3 as:

1. In the logic LOW state at a fan-out of 22 (8mA), Am25LS has 50mV greater noise margin (350mV vs. 300mV).
2. Am25LS products are guaranteed at a fan-out of 22 (8mA) over the military range. Am54LS is specified at fan-out of 10 (4mA) only.
3. Am25LS offers a symmetrical fan-out of 22 in both logic HIGH and logic LOW states, allowing full use of the logic LOW drive capability.

3. A.C. Characteristics

INTRODUCTION

Many Low-Power Schottky functions have been designed specifically to replace standard TTL elements in existing system designs. Their A.C. performance characteristics usually meet or exceed the limits of the earlier devices. The switching terms which are used on data sheets to describe the A.C. performance of these designs are summarized in Table 4. The more important parameters are discussed in detail in this section.

TABLE 4
DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.3V logic level unless otherwise noted.)

f_{MAX}	The highest operating clock frequency.
t_{PLH}	The propagation delay time from an input change to an output LOW-to-HIGH transition.
t_{PHL}	The propagation delay time from an input change to an output HIGH-to-LOW transition.
t_{PW}	Pulse width. The time between the leading and trailing edges of a pulse, measured at the 50% points.
t_r	Rise time. The time required for a signal to change from 10% to 90% of its measured values.
t_f	Fall time. The time required for a signal to change from 90% to 10% of its measured values.
t_s	Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.
t_h	Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.
t_{HZ} also t_{PHZ}	HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5V change).
t_{LZ} also t_{PLZ}	LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5V change).
t_{ZH} also t_{PZH}	Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.
t_{ZL} also t_{PZL}	Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

PROPAGATION DELAYS

The standard designations for delays through combinatorial logic networks are t_{PHL} and t_{PLH}. A delay from an input change to an output going LOW is called t_{PHL}, while t_{PLH} is the delay from an input change to an output going HIGH.

Figure 14 shows a typical waveform with the output changing during the interval indicated by the diagonal, sloping line. Note that all switching times shown are measured at the 1.3 volt logic level.

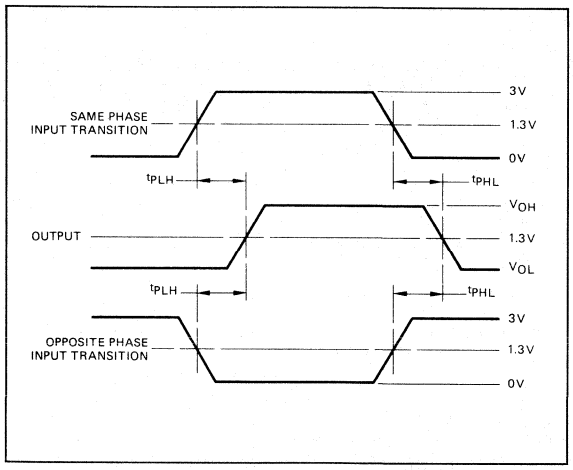


Figure 14. Propagation Delay.

Typical values for a single gate propagation delay t_{PHL} in Low-Power Schottky functions are 8–10ns into a 15pF load. Higher performance LS families, such as Am25LS, exhibit delays in the 4 – 6ns range. These propagation delays will increase by 2 – 4ns at an output loading of 50pF or approximately 0.1ns per pF.

EDGE RATES

The rise and fall times of Low-Power Schottky devices are similar to those of standard TTL. Into a 50pF load fall time, t_f, is typically 6-8ns, while rise time, t_r, is in the 9-12ns range. A.C. parameters are measured at $t_f \leqslant 6$ns and $t_r \leqslant 15$ns.

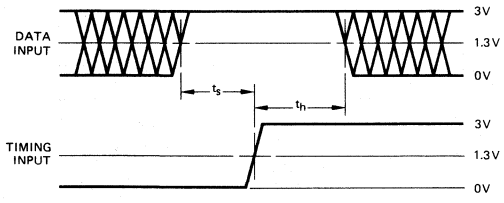
As with standard TTL, careful P.C. board layout rules should be employed to avoid problems which can occur at these relatively fast edge rates. In particular, precautions should be taken to insure that transmission line effects do not cause false switching or ringing and oscillation problems on lines longer than 18 inches. See Section 4 for more information.

SEQUENTIAL DEVICES

Set-up time, t_s, hold time, t_h, are the most important parameters for specifying sequential elements such as latches, flip-flops and registers.

For these synchronous devices, inputs must be stable for a certain period of time before the clock or enable pulse. This interval is the region in time during which devices are "sampling" their inputs. As an example, consider a latch with a D input and an active LOW clock. The latch will store the information present on its input just before the clock goes HIGH. The question is, how long does the input level have to be present and stable before the clock goes HIGH? A particular device will "sample" its input at some exact instant, but in a group of devices some are slower than others. The result is an interval of some time called set-up time during which all devices, fast or slow, will "sample" their inputs.

All devices exhibit a hold time. That is a period of time after the clock or enable pulse transition during which the data cannot be changed without loss of input intelligence. This hold time occurs after the clock goes HIGH. Figure 15 shows the input requirements and definitions for data entry.



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

Figure 15. Set-up and Hold Time Definitions.

f_{MAX}.

A frequently misunderstood parameter on data sheets is maximum clock frequency f_{MAX}. This was defined by the early TTL manufacturers as the maximum toggle frequency which can be attained by the device under ideal conditions with no constraints on t_r, t_f, pulse width, or duty cycle. Although f_{MAX} as specified cannot usually be attained in an operating system, it is a relatively easy parameter to test and provides a convenient measure of comparative performance between different devices.

EFFECTS OF TEMPERATURE AND POWER SUPPLY VARIATIONS

Standard TTL devices exhibit severe degradation in A.C. performance towards the recommended limits of the operating temperature and power supply voltage ranges.

At elevated temperature and/or high V_{CC} levels, charge storage begins to slow down A.C. response. At the other extreme, low temperature and/or low V_{CC}, the loss of β causes a similar problem. These combined effects can cause more than 50% degradation in performance over the full military temperature and power supply extremes.

TABLE 5
GUIDELINES FOR TYPICAL VARIATION OF A.C. PARAMETERS WITH COMBINED TEMPERATURE AND V_{CC} VARIATION

Temperature Range	V_{CC} Variation (Nominal 5V)	AC Derating Factor	
		System	Component
COM'L, 0°C to +70°C	None	5%	10%
COM'L, 0°C to +70°C	±0.25V	15%	30%
MIL, −55°C to +125°C	None	15%	30%
MIL, −55°C to +125°C	±0.5V	25%	50%

Low-Power Schottky technology reduces the impact of both of these effects on performance. β degradation at cold temperatures is far less severe and Schottky clamping largely eliminates the effects of charge storage at high temperature.

The system's designer would like a factor which will allow his system to meet specification with minimum design overkill. However, the component engineer often requires maximum delays to be guaranteed. For system design guidelines, the AC derating factors of Table 5 may be useful.

It must be emphasized that the values of Table 5 are typical. However as it is unlikely that any given system will contain all worst case devices they will usually yield a fairly safe prediction of the system performance which can be achieved.

Individual components will of course be slower than these typical numbers. These must be reflected on procurement specifications. A general rule of thumb would be to double the system design guidelines of Table 5. Am25LS specifications are published with worst case parameters guaranteed over the operating power supply and temperature ranges, as well as at a realistic system load condition of 50pF. A typical example of this format is shown in Table 6.

SHORT CIRCUIT OUTPUT CURRENT

To improve performance, in 1975 TI lowered the short-circuit current limiting resistor value. This increased the I_{SC} (I_{OS}) range from −6 to −42mA up to −30 to −130mA. The overall delay when driving very large capacitive loads (>150pF) was reduced somewhat as a result. However, the inherent circuit performance still dominates in normal applications such that the Am25LS and other high performance families remain faster even when driving large capacitive loads.

TABLE 6
Am25LS2513 THREE-STATE PRIORITY ENCODER
A.C. SPECIFICATION FORMAT FOR V_{CC} AND TEMPERATURE EXTREMES AND 50pF LOAD CONDITION

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	$\overline{I}_i$ to An (In-phase)	C_L = 15pF, R_L = 2.0kΩ		17	25	ns
t_{PHL}				17	25	
t_{PLH}	$\overline{I}_i$ to An (Out-phase)			11	17	ns
t_{PHL}				12	18	
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$			7.0	11	ns
t_{PHL}				24	36	
t_{PLH}	$\overline{EI}$ to $\overline{EO}$			11	17	ns
t_{PHL}				23	34	
t_{PLH}	$\overline{EI}$ to An			12	18	ns
t_{PHL}				14	21	
t_{ZH}	G_1 or G_2 to An			23	40	ns
t_{ZL}				20	37	
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to An			20	30	ns
t_{ZL}				18	27	
t_{HZ}	G_1 or G_2 to An	C_L = 5.0pF, R_L = 2.0kΩ		17	27	ns
t_{LZ}				19	28	
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to An			16	24	ns
t_{LZ}				18	27	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units
t_{PLH}	$\overline{I}_i$ to An (In-phase)	C_L = 50pF, R_L = 2.0kΩ		31		37	ns
t_{PHL}				30		34	
t_{PLH}	$\overline{I}_i$ to An (Out-phase)			22		27	ns
t_{PHL}				22		25	
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$			15		18	ns
t_{PHL}				48		60	
t_{PLH}	$\overline{EI}$ to $\overline{EO}$			19		21	ns
t_{PHL}				46		57	
t_{PLH}	$\overline{EI}$ to An			22		25	ns
t_{PHL}				27		32	
t_{ZH}	G_1 or G_2 to An			42		49	ns
t_{ZL}				43		49	
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to An			36		43	ns
t_{ZL}				35		43	
t_{HZ}	G_1 or G_2 to An	C_L = 5.0pF, R_L = 2.0kΩ		34		40	ns
t_{LZ}				34		40	
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to An			30		35	ns
t_{LZ}				31		35	

4. Design Guidelines

POWER SUPPLY CONSIDERATIONS

The recommended power supply voltage (V_{CC}) for all TTL circuits, including LS, is +5V. Commercial temperature range devices, designated 74LS or in the case of Am25LS with the suffix C, are specified with a ±5% supply tolerance (±250mV) over the ambient range 0°C to 70°C. Military range parts, designated 54LS or in the case of Am25LS with the suffix M, are guaranteed with a ±10% supply tolerance (±500mV) over an ambient temperature range of −55°C to +125°C. The power supply should be well regulated with a ripple less than 5% and with regulation better than 5%. Even though LS devices generate significantly smaller power supply spikes when switching than standard TTL, on-board regulation is still preferable to isolate this noise to one board.

A low-inductance transmission line power distribution bus with good RF decoupling is necessary for large systems. On all boards, ceramic decoupling capacitors of 0.01μF to 0.1μF should be used at least one for every five packages, and one for every one-shot (monostable), line driver and line receiver package. In addition, a larger tantalum capacitor of 20μF to 100μF should be included on each card. On boards containing a large number of packages, a low impedance ground system is essential. The ground can either be a bus or a ground which is incorporated with the V_{CC} supply to form a transmission line power system. Separate power transmission systems can be attached to the board to provide this same feature without the cost of a multi-layer PC card.

UNUSED INPUTS

An unused input to an AND or NAND gate should not be left floating as it can act as an antenna for noise. On devices with storage, such as latches, registers and counters, it is particularly important to terminate unused inputs (MR, PE, PL, CP) properly since a noise spike on these inputs might change the contents of the memory. This technique optimizes switching speed as the distributed capacitance associated with the floating input, bond wire and package leads is eliminated. To terminate, the input should be held between 2.4V and the maximum input voltage. One method of achieving this is to connect the unused input to V_{CC}. Most LS inputs have a breakdown voltage >7V and require no series resistor. Devices specified with a maximum 5.5 volt breakdown should use a 1kΩ to 10kΩ current limiting series resistor to protect against V_{CC} transients. Another method is to connect the unused input to the output of an unused gate that is forced HIGH. Do not connect an unused input to another input of the same NAND or AND function. Although recommended for standard TTL, with LS this increases the input coupling capacitance and reduces A.C. noise immunity.

TRANSMISSION LINE EFFECTS

The relatively fast rise and fall times of Low-Power Schottky TTL (5 to 15ns) can cause transmission line effects with interconnections as short as 18 inches. With one TTL device driving another and the driver switching from LOW to HIGH, if the propagation delay of the interconnection is long compared to the signal rise time, the arrangement can behave like a transmission line driven by a generator with a non-linear output. The initial voltage step at the output, just after the driver has switched, propagates down the line and reflects at the end. In the typical case where the line is open ended or terminated in an impedance greater than its characteristics impedance (Z_{OL}), the reflected wave arrives back at the source and increases V_{OUT}. If the total round-trip delay is longer than the rise time of the driving signal, a staircase response results at the driver output and along the line. If one of the driven devices is connected close to the driver, the initial output voltage (V_{OUT}) seen by it might not exceed V_{IH}. The state of the input is undetermined until after the round trip of the transmission line, thus slowing down the response of the system.

The longest interconnection that should be used with LS devices without incurring problems due to line effects is in the 10–12 inch range.

With longer interconnections, transmission line techniques should be used for maximum speed. Good system operation can be obtained by designing around 100 ohm lines. A 0.026 inch (0.65mm) trace on a 0.062 inch epoxy-glass board (E_r = 4.7) with a ground plane on the other side represents a 100Ω line. 28 to 30 gauge wire (0.25 to 0.30mm) twisted pair line has a characteristic impedance of 100 to 115Ω.

LINE DRIVING AND RECEIVING

For lines longer than 2 feet, twisted pairs of coaxial cable should be used. The characteristic impedance or the transmission media should be approximately 120Ω such as twisted pairs of #26 wire or 100Ω coax. A possible choice is cables with a characteristic impedance R_0 of 100Ω such as ribbon cable or flat cable with controlled impedance. Resistive pull-ups at the receiving end can be used to increase noise margin. Where reflection effects are unacceptable, the line must be terminated in its characteristic impedance. A method shown in Figure 16 has the output of the line tied to V_{CC} through a resistor equivalent to the characteristic impedance of the line. As the output impedance of the LS driver is low and must sink the current through it, in addition to the current from the inputs being driven, a useful technique is to terminate the line in a voltage divider with two resistors, each twice the line impedance. This

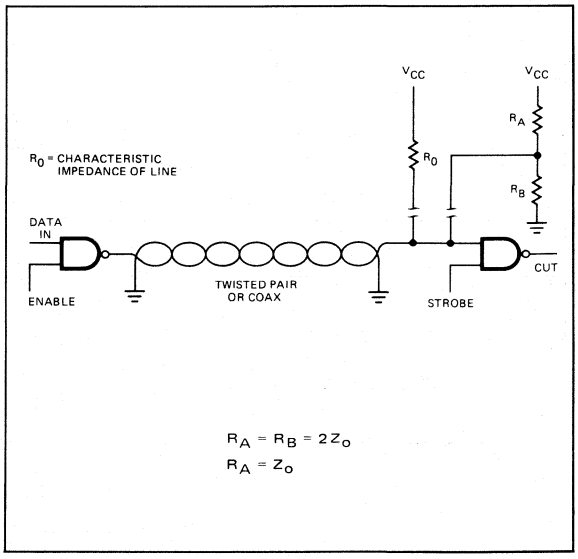


Figure 16. LS Driving Twisted Pair.

reduces the extra sink current by 50%. Where the line exceeds five feet in length it is preferable to dedicate gates solely to line driving.

For additional noise immunity when driving long lines, a differential line driver and line receiver may be used. These dedicated line interface circuits drive a twisted pair of wires differentially, permit easy termination of lines and provide excellent common mode noise rejection.

The Am26LS31 driver and Am26LS32 and Am26LS33 are quad differential line drivers and receivers satisfying the interface requirements of EIA RS-422 and 423 as well as military applications, Figure 17. They are designed to operate off the standard 5V power supplies of the LS logic devices. More applications information on line termination techniques is provided on the above mentioned device data sheets.

CROSS-TALK AND RINGING

These two problems may be experienced with all forms of high speed digital logic. Crosstalk is the coupling of energy from one circuit to another via real or parasitic capacitance and inductance. Ringing is the possible rebound of the signal into the input threshold region (0.8 – 2.0V) following a HIGH-to-LOW level change. When a driver switches from a HIGH-to-LOW state the output voltage should fall below the threshold value. However, a line having a very low characteristic impedance does not allow transistor Q5 in the NAND gate example to saturate, and the resulting output voltage may not be low enough to switch an adjacent device until two or more line delay times. The low current levels at which LS devices operate, coupled with the low output impedance in both HIGH and LOW Logic states, minimize crosstalk effects. Input clamp diodes provided on all LS devices are extremely effective in reducing ringing phenomenon.

Care should be taken to insure that signals with falling edges faster than 2.5-3ns/volt are not coupled into the input of an LS function. Even though the signal may not pass into the threshold region, if the pulse edge is fast enough, sufficient energy may be capacitively coupled into a sequential device to cause it to change state: High speed Schottky elements in a test setup can exceed this limit. However in an active system, the edges will generally be slowed sufficiently to eliminate any problem.

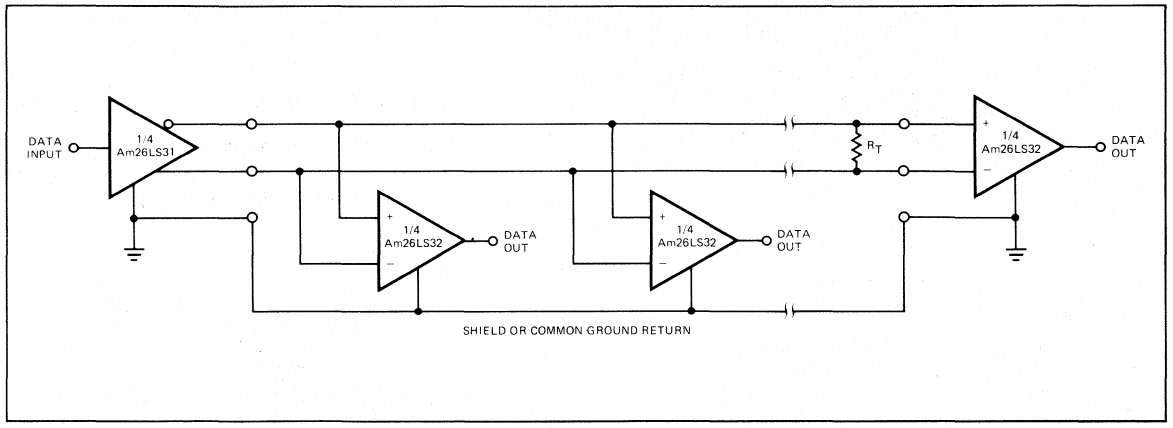


Figure 17. Differential Line Driving and Receiving with the Am26LS31 and Am26LS32.

DEFINITION OF STANDARD LOW-POWER SCHOTTKY TERMS

DEFINITION OF A.C. SWITCHING TERMS

(All switching times are measured at the 1.3V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_{HZ} HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5V change).

t_{LZ} LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5V change).

t_{ZH} Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

t_{ZL} Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

DEFINITION OF D.C. TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input

O Output

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

I_{OZH} Three-state off-state output current, HIGH-level voltage applied.

I_{OZL} Three-state off-state output current, LOW-level voltage applied.

V_{CC} The range of supply voltage over which the device is guaranteed to operate.

V_{IL} The guaranteed maximum input voltage that will be recognized by the device as a logic LOW.

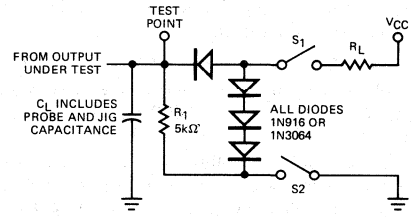
V_{IH} The guaranteed minimum input voltage that will be recognized by the device as a logic HIGH.

V_{OL} The maximum guaranteed logic LOW voltage at the output terminal while sinking the specified load current I_{OL}.

V_{OH} The minimum guaranteed logic HIGH voltage at the output terminal when sourcing the specified source current I_{OH}.

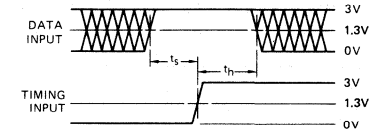
LOW-POWER SCHOTTKY PARAMETER MEASUREMENTS

LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



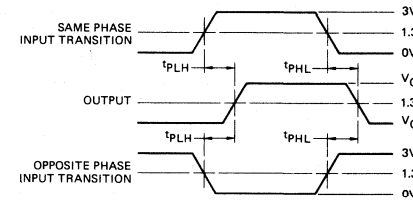
Note: For standard totem-pole outputs, remove R_1, S_1 and S_2 closed.

SET-UP, HOLD, AND RELEASE TIMES

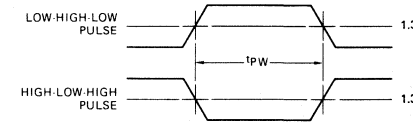


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

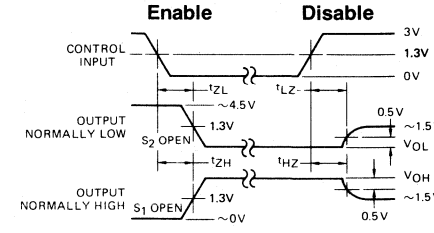
PROPAGATION DELAY



PULSE WIDTH



ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6ns.

DEFINITION OF STANDARD SCHOTTKY TERMS

DEFINITION OF A.C. SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

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t_{ZH} Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

t_{ZL} Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

DEFINITION OF D.C. TERMS

H HIGH, applying to a HIGH voltage level.

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I_{OL} LOW-level output current.

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I_{SC} Output short-circuit source current.

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I_{OZH} Three-state off-state output current, HIGH-level voltage applied.

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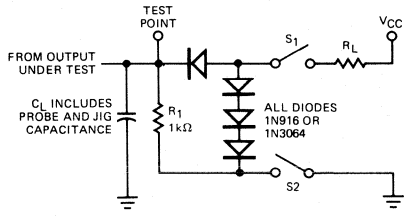
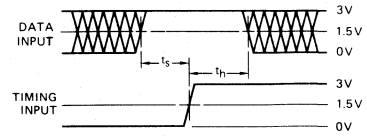
SCHOTTKY PARAMETER MEASUREMENTS FOR THREE-STATE OUTPUTS

LOAD TEST CIRCUIT

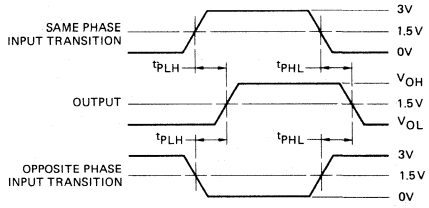


SET UP, HOLD, AND RELEASE TIMES

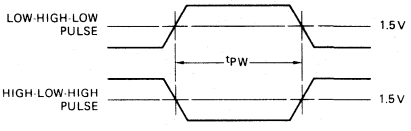


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

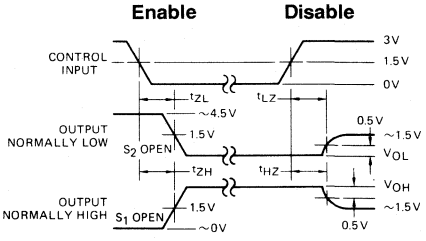
PROPAGATION DELAY



PULSE WIDTH



ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

Low Power Schottky Index

Am25LS07·Am25LS08

Hex/Quad Parallel D Registers With Register Enable

DISTINCTIVE CHARACTERISTICS

- 4-bit and 6-bit parallel registers
- Common Clock and Common Enable
- Positive edge triggered D flip flops
- Am25LS d. c. parameters including:
  V_{OL} = 0.45V at I_{OL} = 8mA
  Fan-out over military range = 22
  440μA source current
- Second sourced by TI as 54LS/74LS378 and 379
- 100% product assurance screening to MIL-STD-883 requirements

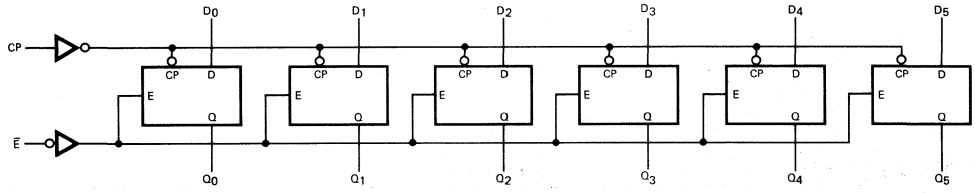
FUNCTIONAL DESCRIPTION

The Am25LS07 is a 6-bit Low Power Schottky register with a buffered common register enable. The Am25LS08 is a 4-bit register with a buffered common register enable. The devices are similar to the Am54LS/74LS174 and Am54LS/74LS175 but feature the common register enable rather than common clear.

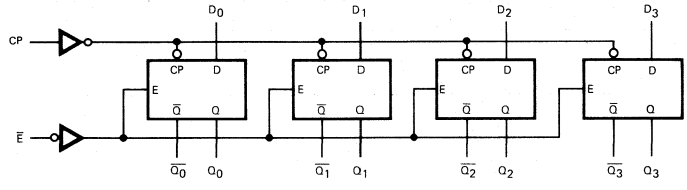
Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

LOGIC DIAGRAMS

Am25LS07



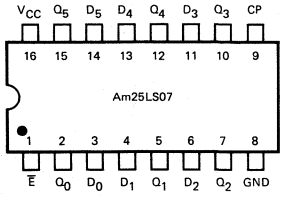
Am25LS08



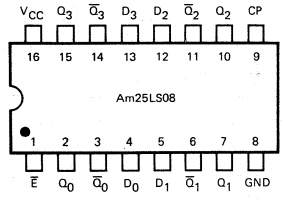
CONNECTION DIAGRAMS

Top Views

Am25LS07



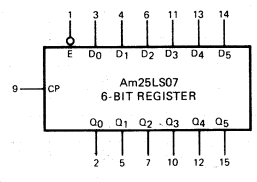
Am25LS08



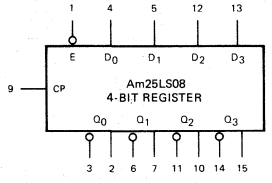
Note: Pin 1 is marked for orientation.

LOGIC SYMBOLS

Am25LS07



Am25LS08



V_{CC} = Pin 16
GND = Pin 8

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -440\mu A$ $V_{IN} = V_{IH}$ or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 4mA			0.4	Volts
			I_{OL} = 8mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	COM'L			0.8	Volts
			MIL			0.7	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	Clock, $\overline{E}$			−0.36	mA
			Others			−0.24	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	Clock, $\overline{E}$			20	μA
			Others			14	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)	LS07		16	22	mA
			LS08		11	18	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0,5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Output		13	20	ns	C_L = 15pF $R_L = 2.0k\Omega$
t_{PHL}	Clock to Output		13	20	ns	
t_{pw}	Clock Pulse Width	17			ns	
t_s	Data	20			ns	
t_s	Enable	30			ns	
t_h	Data	5.0			ns	
t_h	Enable	5.0			ns	
f_{max} (Note 1)	Maximum Clock Frequency	40	65		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output		30		35	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}	Clock to Output		30		35	ns	
t_{pw}	Clock Pulse Width	26		30		ns	
t_s	Data	30		35		ns	
t_s	Enable	43		50		ns	
t_h	Data	11		12		ns	
t_h	Enable	11		12		ns	
f_{max} (Note 1)	Maximum Clock Frequency	30		25		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{E}$ Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Q_i The TRUE register outputs.

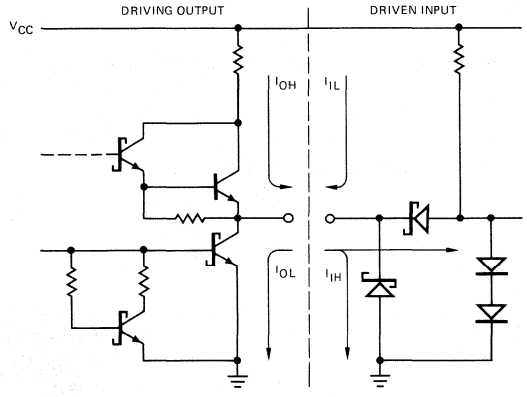
$\overline{Q}_i$ The complement register outputs

FUNCTION TABLE

Inputs			Outputs	
$\overline{E}$	D_i	CP	Q_i	$\overline{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

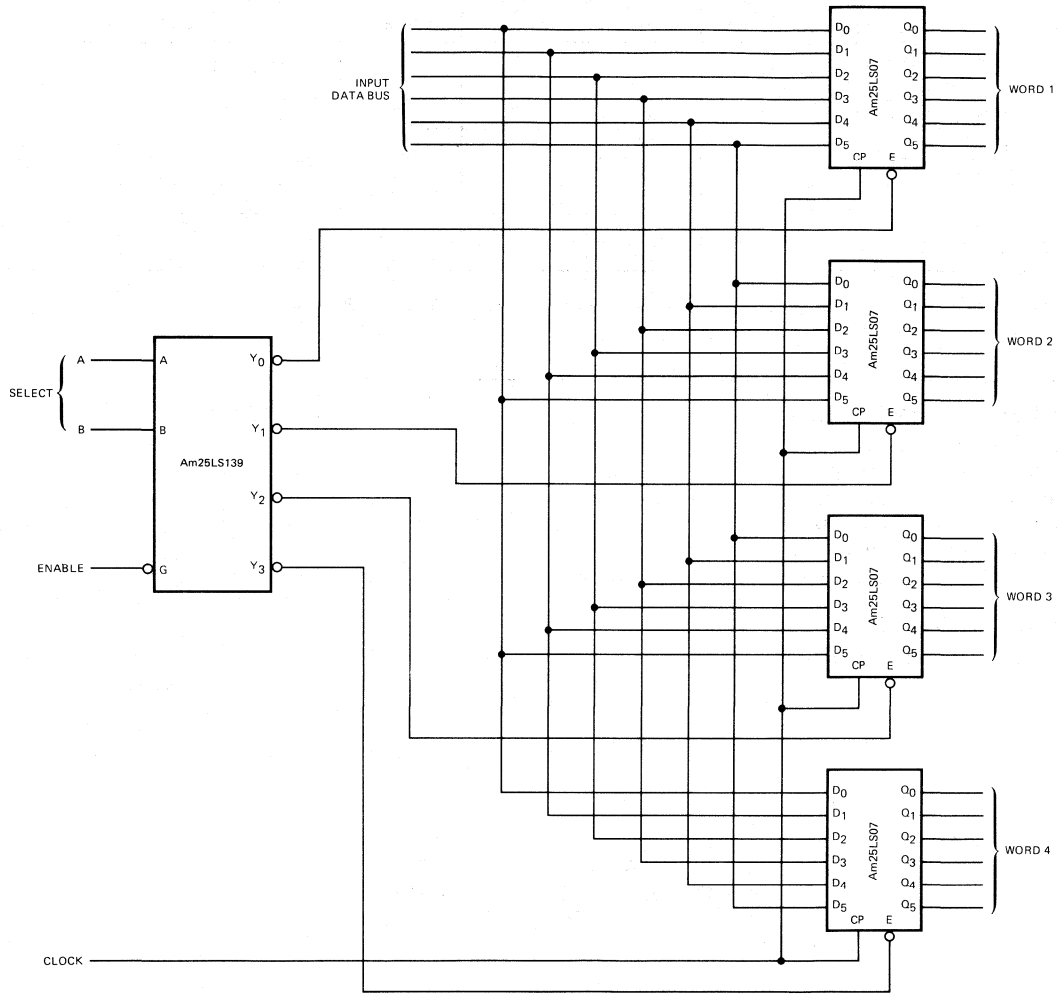
H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25LS08 Only

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

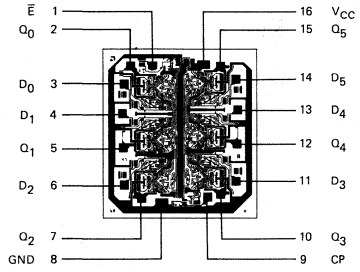
APPLICATION



Selective Register Loading of Data on Synchronous Clock.

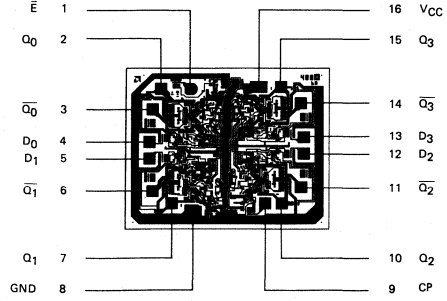
Metallization and Pad Layout

Am25LS07



DIE SIZE 0.075" X 0.084"

Am25LS08



DIE SIZE 0.075" X 0.061"

Am25LS09

Quad Two-Input, High-Speed Register

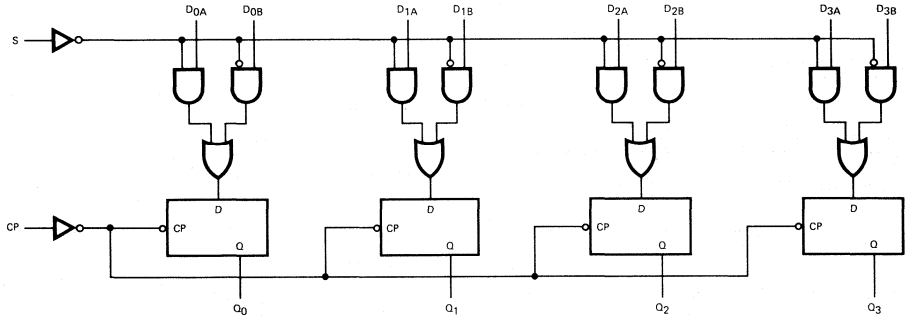
DISTINCTIVE CHARACTERISTICS

- 4-bit register accepts data from one-of-two 4-bit input fields
- Edge triggered clock action
- Second sourced by T.I. as 54LS/74LS399
- Am25LS d.c. parameters including:
  - V_{OL} = 0.45V at I_{OL} = 8mA
  - Fan-out over military range = 22
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

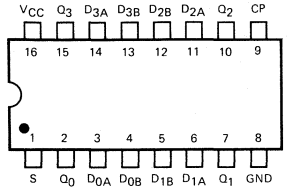
FUNCTIONAL DESCRIPTION

The Am25LS09 is a dual port four-bit register using advanced Low Power Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

LOGIC DIAGRAM

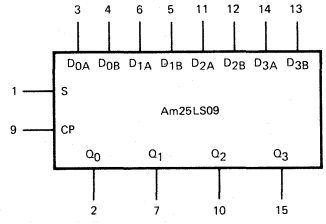


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	(MIN. = 4.75V MAX. = 5.25V)
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	(MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -440\mu A$ $V_{IN} = V_{IH}$ or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 4mA			0.4	Volts
			I_{OL} = 8mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	Clock, S			−0.36	mA
			Others			−0.24	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	Clock, S			20	μA
			Others			14	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)			11	18	mA

Notes: 1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q HIGH		13	20	ns	C_L = 15pF, $R_L = 2.0k\Omega$
t_{PHL}	Clock to Q LOW		13	20	ns	
t_{pw}	Clock Pulse Width	17			ns	
t_s	Data Set-up Time	20			ns	
t_s	Select Input Set-up Time	30			ns	
t_h	Data Hold Time	5			ns	
t_h	Select Input Hold Time	0			ns	
f_{max} (Note 1)	Maximum Clock Frequency	40	65		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Q HIGH		30		35	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}	Clock to Q LOW		30		35	ns	
t_{pw}	Clock Pulse Width	26		30		ns	
t_s	Data Set-up Time	30		35		ns	
t_s	Select Input Set-up Time	43		50		ns	
t_h	Data Hold Time	11		12		ns	
t_h	Select Input Hold Time	4		5		ns	
f_{max} (Note 1)	Maximum Clock Frequency	30		25		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_{0A}, D_{1A}, D_{2A}, D_{3A} The "A" word into the two-input multiplexer of the D flip-flops.

D_{0B}, D_{1B}, D_{2B}, D_{3B} The "B" word into the two-input multiplexer of the D flip-flops.

Q_0, Q_1, Q_2, Q_3 The outputs of the four D-type flip-flops of the register.

S Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH the B word is applied to the D inputs of the flip-flops.

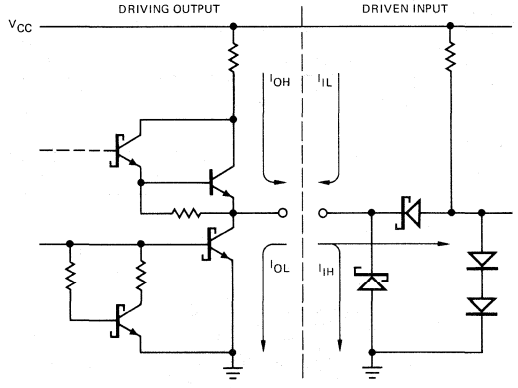
CP Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

FUNCTION TABLE

SELECT S	CLOCK CP	DATA D_{iA}	INPUTS D_{iB}	OUTPUT Q_i
L	↑	L	X	L
L	↑	H	X	H
H	↑	X	L	L
H	↑	X	H	H

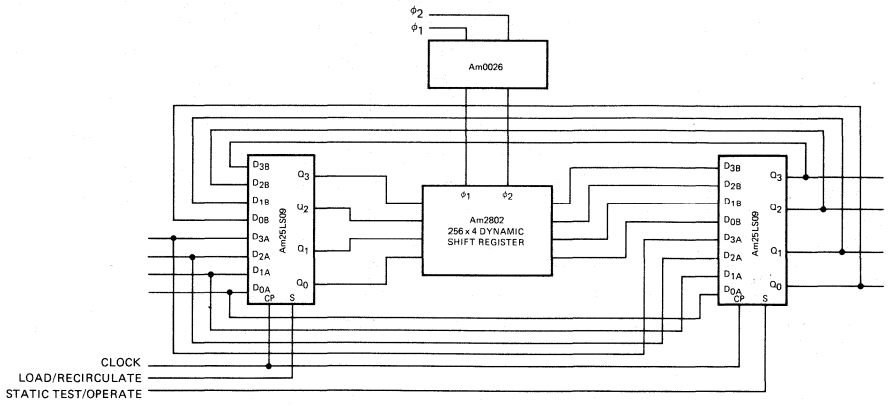
H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
L = LOW Voltage Level
i = 0, 1, 2, or 3

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

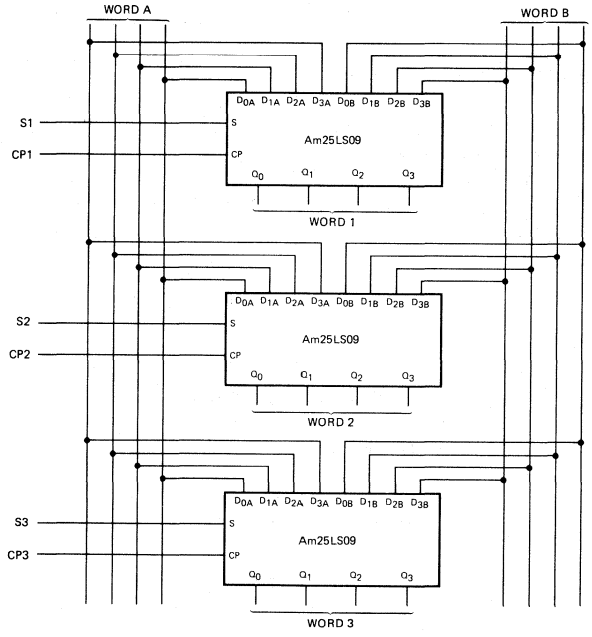


Note: Actual current flow direction shown.

APPLICATIONS

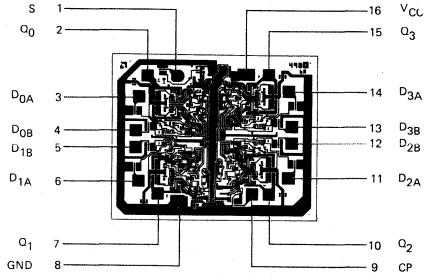


Am25LS09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.



Am25LS09 used to store a word from either data bus A or data bus B.

Metallization and Pad Layout



DIE SIZE 0.075" X 0.061"

Am25LS14

8-Bit Serial/Parallel Two's Complement Multiplier

DISTINCTIVE CHARACTERISTICS

- Two's complement multiplication without correction
- Magnitude only multiplication
- Cascadable for any number of bits
- 8-bit parallel multiplicand data input
- 25MHz minimum clock frequency
- Second sourced by T.I. as the SN54LS/74LS384
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

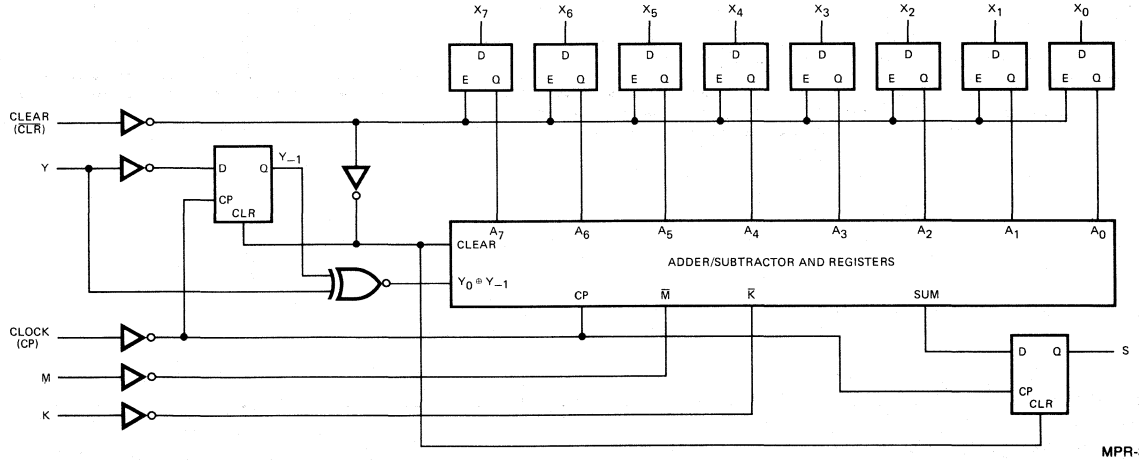
The Am25LS14 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream — least significant bit first. The product is clocked out the S output least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The Am25LS14 must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

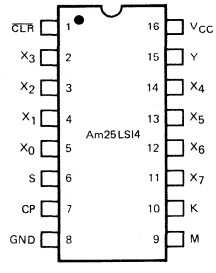
The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

LOGIC DIAGRAM



MPR-327

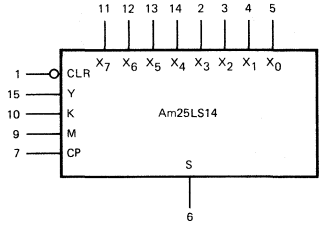
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-328

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-329

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25LS14XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am25LS14XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.4	Volts
			I_{OL} = 12mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	X, M			−0.48	mA
			K, $\overline{CLR}$			−1.2	
			CP			−1.6	
			Y			−3.2	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	X, M			20	µA
			K, $\overline{CLR}$			30	
			CP			40	
			Y			80	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			91	155	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Duration of the short circuit test should not exceed one second.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Output		13	20	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			13	20		
t_{PHL}	Clear to Output		17	25	ns	
t_s	Y to Clock	32			ns	
t_h		0				
t_s	K to Clock	18			ns	
t_h		0				
t_s	X_i to Clear	13			ns	
t_h		0				
t_{pw}	Clock (HIGH)	15			ns	
	Clock (LOW)	15				
t_{pw}	Clear Pulse Width	20			ns	
t_s	Clear Recovery Time (Inactive State)	18			ns	
f_{max} (Note 1)	Maximum Clock Frequency	25	30		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min.	 Max.	Am25LS MIL T_A = –55°C to +125°C V_{CC} = 5.0V ± 10% Min.	 Max.	Units	Test Conditions
t_{PLH}	Clock to Output		24		27	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			27		30		
t_{PHL}	Clear to Output		33		37	ns	
t_s	Y to Clock	38		45		ns	
t_h		0		0			
t_s	K to Clock	24		30		ns	
t_h		0		0			
t_s	X_i to Clear	19		23		ns	
t_h		0		0			
t_{pw}	Clock (HIGH)	18		22		ns	
	Clock (LOW)	18		22			
t_{pw}	Clear Pulse Width	33		38		ns	
t_s	Clear Recovery Time (Inactive State)	20		30		ns	
f_{max} (Note 1)	Maximum Clock Frequency	20		15		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7 The eight data inputs for the multiplicand (X) data.

Y The serial input for the multiplier (Y) data—least significant bit first.

S The serial output for the product of X • Y—least significant bit first.

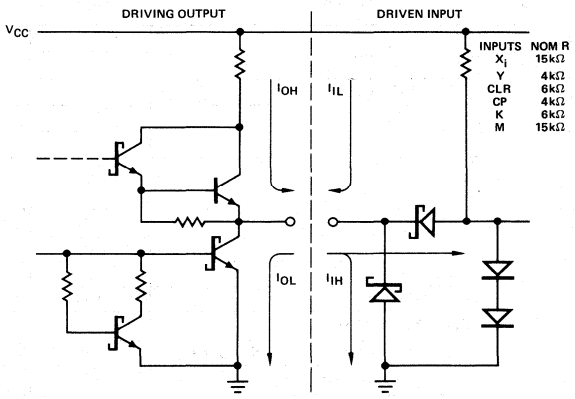
CP Clock. The buffered common clock input for the serial/parallel multiplier. All functions occur on the LOW-to-HIGH transition of the clock.

CLR Clear. The buffered common clear for all flip-flops within the device. When the clear is LOW all flip-flops are cleared. Also the buffered X-input latch enable. When the clear input is LOW, the X latches will accept new X-input data.

K The sum expansion input to the serial/parallel multiplier. Allows for cascading devices.

M The mode control input for the most significant bit of the multiplier. It is used in conjunction with cascading to determine the most significant bit.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



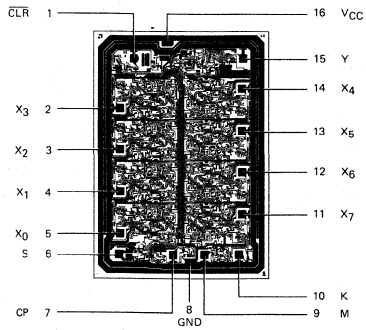
Note: Actual current flow direction shown.

FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{CLR}$	CP	K	M	X_i	Y	Y_{-1}	S	
–	–	L	L	–	–	–	–	Most Significant Multiplier Device
–	–	CS	H	–	–	–	–	Devices Cascaded in Multiplier String
L	–	–	–	OP	–	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	–	–	–	–	–	–	–	Device Enabled
H	↑	–	–	–	L	L	AR	Shift Sum Register
H	↑	–	–	–	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	–	–	–	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	–	–	–	H	H	AR	Shift Sum Register

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device
OP = X_i latches open for new data (i = 0, 7)
AR = Output as required per Booth's algorithm

Metallization and Pad Layout



DIE SIZE 0.097" X 0.137"

LOW-POWER SCHOTTKY LOADING RULES

Input/Output	Pin No.'s	Input Unit Load HIGH	Input Unit Load LOW	Output HIGH	Fan-out Output LOW 8mA	Fan-out Output LOW 12mA
$\overline{CLR}$	1	1.5	3.3	–	–	–
X_3	2	1.0	1.3	–	–	–
X_2	3	1.0	1.3	–	–	–
X_1	4	1.0	1.3	–	–	–
X_0	5	1.0	1.3	–	–	–
S	6	–	–	50	22	33
CP	7	2.0	4.4	–	–	–
GND	8	–	–	–	–	–
M	9	1.0	1.3	–	–	–
K	10	1.5	3.3	–	–	–
X_7	11	1.0	1.3	–	–	–
X_6	12	1.0	1.3	–	–	–
X_5	13	1.0	1.3	–	–	–
X_4	14	1.0	1.3	–	–	–
Y	15	4.0	8.8	–	–	–
V_{CC}	16	–	–	–	–	–

A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

STANDARD POWER SCHOTTKY LOADING RULES

Input/Output	Pin No.'s	Input Unit Load HIGH	Input Unit Load LOW	Output HIGH	Fan-out Output LOW 8mA	Fan-out Output LOW 12mA
$\overline{CLR}$	1	0.6	0.6	–	–	–
X_3	2	0.4	0.25	–	–	–
X_2	3	0.4	0.25	–	–	–
X_1	4	0.4	0.25	–	–	–
X_0	5	0.4	0.25	–	–	–
S	6	–	–	20	4.0	6.0
CP	7	0.8	0.8	–	–	–
GND	8	–	–	–	–	–
M	9	0.4	0.25	–	–	–
K	10	0.6	0.6	–	–	–
X_7	11	0.4	0.25	–	–	–
X_6	12	0.4	0.25	–	–	–
X_5	13	0.4	0.25	–	–	–
X_4	14	0.4	0.25	–	–	–
Y	15	1.6	1.6	–	–	–
V_{CC}	16	–	–	–	–	–

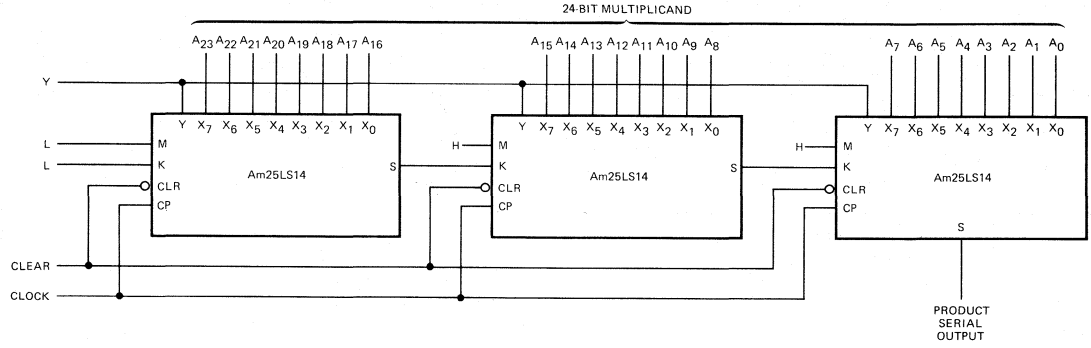
A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

ORDERING INFORMATION

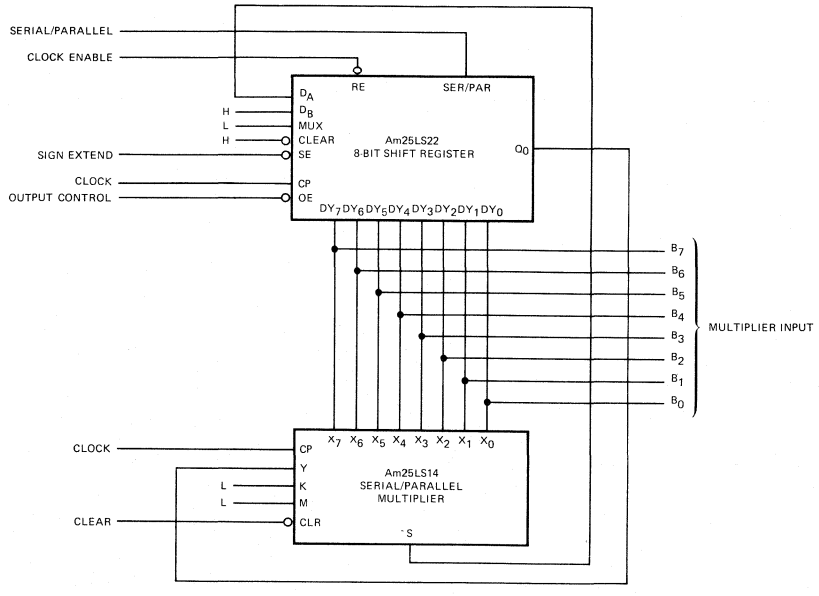
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS14PC
Hermetic DIP	0°C to +70°C	AM25LS14DC
Dice	0°C to +70°C	AM25LS14XC
Hermetic DIP	–55°C to +125°C	AM25LS14DM
Hermetic Flat Pak	–55°C to +125°C	AM25LS14FM
Dice	–55°C to +125°C	AM25LS14XM

APPLICATIONS

See also Digital Signal Processing Applications Section for more information.



Basic 24-Bit Serial/Parallel Connection



8-Bit by 8-Bit Multiplier, Bus Organized, with 8-Bit Truncated Product

A HIGH-SPEED SERIAL/PARALLEL MULTIPLIER THE Am25LS14*

By John Mick, John Springer and Clive Ghest

2

INTRODUCTION

The Am25LS14 is a complete 8-bit Serial/Parallel Multiplier fabricated as a single 16-pin LSI chip. The device accepts a parallel two's complement or unsigned multiplicand and multiplies it by any arbitrary length serial two's complement or unsigned multiplier. The resulting product is a correct and complete serial two's complement or unsigned product. The complete product of an 8 x 8 multiplication can be performed in 16 clock cycles. Any number of Am25LS14 devices can be cascaded with no additional logic, so that the parallel multiplicand can be easily expanded to any number of bits. Mixed signed (two's complement) and unsigned multiplication is possible, generating a product in signed two's-complement form.

MULTIPLIER CHARACTERISTICS

The requirements for a good general purpose IC multiplier for use in a wide range of commercial applications are as follows:

- It should be inexpensive
- It should be fast
- It should be easy to use
- It should be adaptable to any word length
- It should handle signed numbers in two's complement notation without correction.

The first two of these requirements tend to be incompatible and in the past have required two types of circuits: one which was designed to be as fast as possible and another which compromised speed for cost. The last two requirements limit the method used to perform the multiplication to an algorithm which works in two's complement notation and is the same for all bits, so that the "sign bit" is treated identically with the other bits.

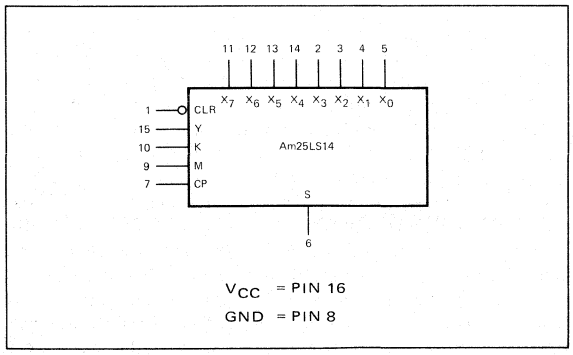


Figure 2. Logic Symbol for the Am25LS14 (16-Pin Device)

The Am25LS14 offers an optimum solution to these requirements. It operates by taking the whole multiplicand in parallel and utilizing a single bit at a time of the multiplier word to form partial products in an internal register. The output is a serial bit stream representing the product of the parallel multiplicand word and the serial multiplier word.

THE LOGIC FUNCTION

A simplified logic diagram of the Am25LS14 Serial/Parallel multiplier is shown in Figure 1 and the 16-pin logic symbol for the device is shown in Figure 2. The multiplier consists of four basic parts; a storage register used to hold the multiplicand word during the multiplication, the adder/subtractor logic containing both a partial product register and a carry/borrow register, a flip-flop and exclusive-NOR gate operating on the serial multiplier string presented at the Y input to provide a

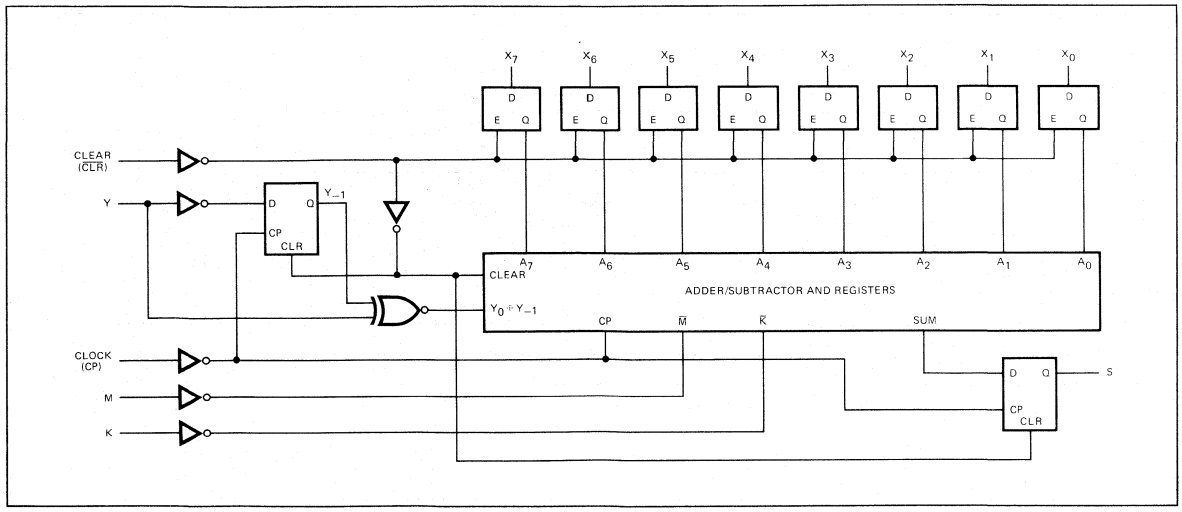


Figure 1. Functional Logic Diagram for the Am25LS14

*The Am25LS14 is manufactured under U. S. Patent No. 3,878,985 issued April 22, 1975.

control signal to the adder/subtractor logic, and a logic mode circuit to alter the multiplicand from two's complement to unsigned notation as controlled by the M input. The adder/subtractor logic and product and carry/borrow register is iterative; that is, it consists of eight identical cells with a small change in the eighth cell to efficiently incorporate the multiplicand word sign logic. For a detailed description of the logic design of the Serial/Parallel multiplier, refer to the application note "Mechanization of the Serial/Parallel Multiplier" by John R. Mick.

Prior to a multiplication, the internal multiplier sum and carry registers are reset by applying a LOW to the clear input. The 8-bit multiplicand data is applied to the X inputs and is latched into the multiplicand register as the clear input goes HIGH. This internal multiplicand storage is useful because the multiplicand need not be held constant during the multiplication allowing these inputs to be bus organized. The Serial/Parallel multiplier is now ready to receive the first least significant multiplier bit. The least significant bit of the multiplier word is presented at the Y serial input and when the clock changes from LOW to HIGH, the multiplier produces the first least significant product bit at the serial data output, S. In each succeeding clock period, the next more significant multiplier bit is presented at the Y input and the next more significant product bit is present at the S output. After 8 clock periods, the multiplier serial input string has been exhausted but the most significant half of the product is still in the internal registers of the Am25LS14 Serial/Parallel multiplier and must be clocked out. If the multiplier is an unsigned word, then during the extraction of the most significant half of the product, the multiplier Y input must be held at logic zero. If, however, the multiplier is a two's-complement signed word, then the most significant bit (sign bit) of the multiplier word must be repeated at the Y input until the complete product has been obtained. The multiplicand can be either an unsigned number or a two's-complement number depending upon the logic polarity of the mode input, M. This mode input should be held at a LOW logic level (ground) if the multiplicand is in two's-complement notation and the X_7 input is a two's complement sign bit, and it should be held at a HIGH logic level (pulled up through a register to V_{CC}) if the 8-bit multiplicand is unsigned (magnitude only number).

The K input is used for expansion purposes. To increase the length of the multiplicand word by using multiple devices, the S output of a higher order device is connected to the K input of the next lower order devices. The clear lines are connected together and the clock lines are connected together. All the mode inputs except the one on the most significant device are held at a HIGH logic level. Whether the multiplicand is signed or unsigned is determined only by the M input of the most significant device. A 24-bit by n-bit multiplier is shown in Figure 3. The K input is held LOW at the most significant device indicating a two's complement multiplicand. The multiplier input can be any length, with n + 24 clock periods required for the multiplication. The resulting product is n + 24 bits long.

If the multiplicand is not an even multiple of 8 bits, then for an unsigned multiplicand the remaining most significant multiplicand inputs are held LOW at logic zero, while for a two's-complement multiplicand, the remaining multiplicand inputs must be connected to the multiplicand sign bit so that the sign is extended and can be interpreted correctly. Figure 4 shows a 12 x n Serial/Parallel multiplier connection for a two's-complement signed multiplicand. The resulting product is n + 12 bits long and only n + 12 clock periods are required to generate the correct product.

The Function Table for the Am25LS14 multiplier operation is given in Figure 5. As shown, the K input is the sum expansion input and allows for the cascading of devices. The mode input, M, is used in conjuction with cascading to determine the most significant bit of the multiplicand and controls the multiplicand sign definition.

TIMING

Although the Serial/Parallel multiplier requires only m + n clock periods to produce a full length product, (where m is the multiplicand word length and n is the multiplier word length) a practical system may use two additional clock periods. The first additional clock period is used to reset the multiplier at the beginning of a multiplication by using the clear input. This is shown in the timing diagram of Figure 6. This clears the partial product register, the carry/borrow register and the

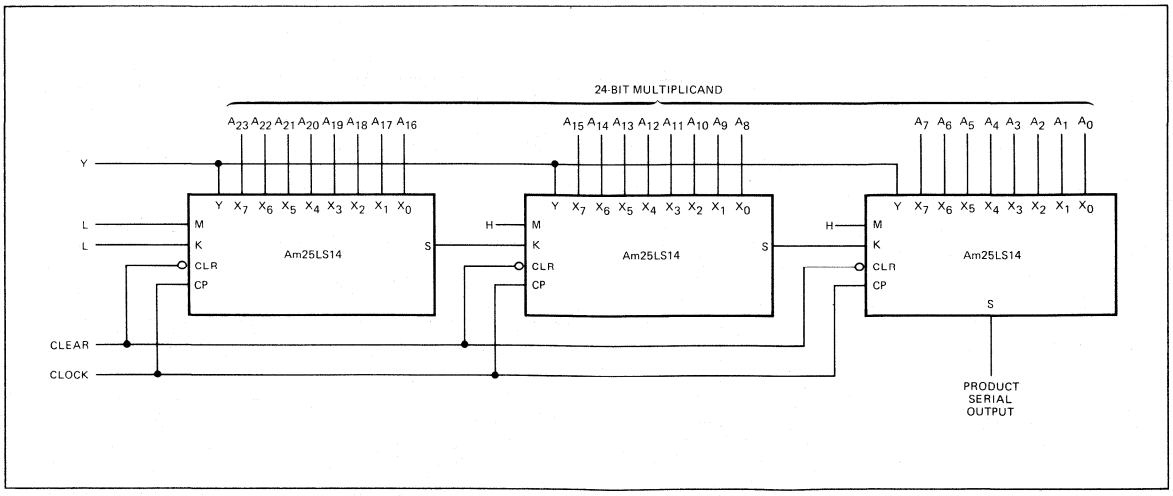


Figure 3. Three Am25LS14's Cascaded to Make a 1-Bit by 24-Bit Serial-Parallel Multiplier

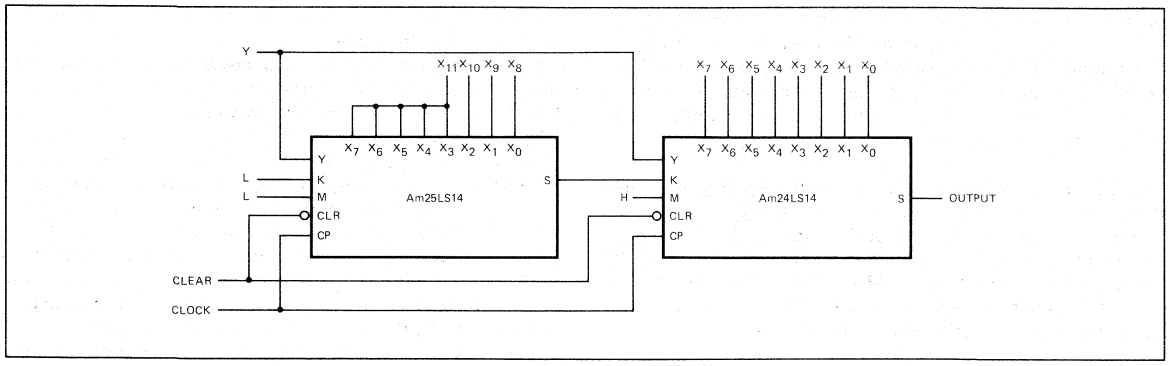


Figure 4. A 12-Bit by N-Bit Two's Complement Multiplier Using Two Am25LS14's

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{CLR}$	CP	K	M	X_i	Y	Y_{-1}	S	
–	–	L	L	–	–	–	–	Most Significant Multiplier Device
–	–	CS	H	–	–	–	–	Devices Cascaded in Multiplier String
L	–	–	–	OP	–	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	–	–	–	–	–	–	–	Device Enabled
H	↑	–	–	–	L	L	AR	Shift Sum Register
H	↑	–	–	–	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	–	–	–	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	–	–	–	H	H	AR	Shift Sum Register

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device
OP = X_i latches open for new data (i = 0, 7)
AR = Output as required per Booth's algorithm

Figure 5. Function Table Showing the Operation of the Am25LS14

control flip flop, and loads the new multiplicand into the X holding latch. At this same time, the multiplier word can be loaded into a Parallel-to-Serial converter (such as the Am25LS22) ready for presenting to the Serial/Parallel multiplier Y input. During the first time period after the clear signal, the least significant bit of the multiplier is presented to the Y input of the Am25LS14 and in the next clock period the first bit of the product, S_0, is available at the S output of the device. For the next n–1 clock periods, the multiplier bits are presented one at a time to the multiplier Y input and the

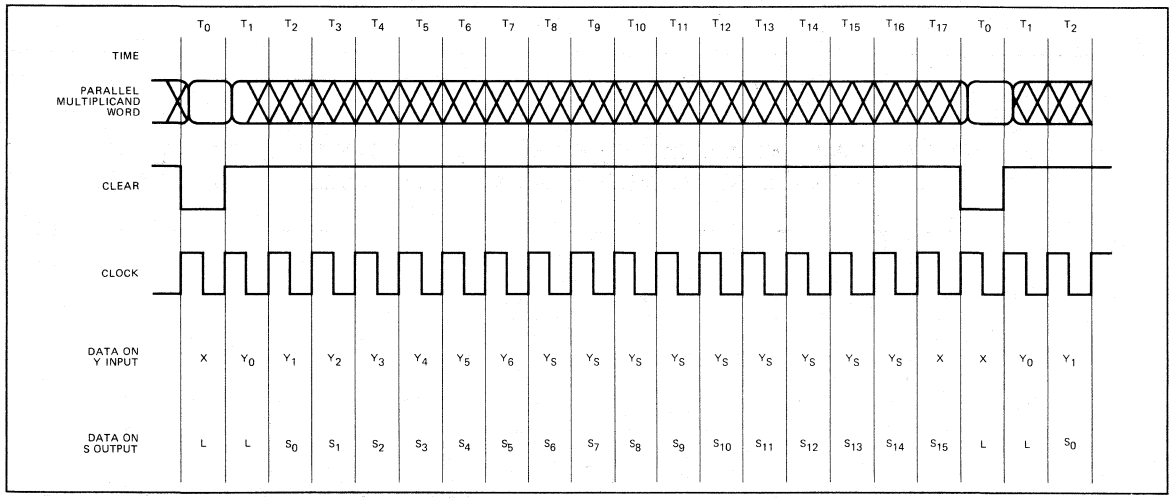


Figure 6. Timing Diagram Showing 18 Clock Cycle Operation of 8 x 8 Multiplication

product bits are available one at a time from the S output. For the remaining m clock periods, the Serial/Parallel multiplier requires that either the most significant bit of the multiplier word, Y, be repeated (two's complement operation) or a string of zeroes be applied (if the multiplier is to be treated as an unsigned number) to the Y input.

It is possible to perform an m + n multiplication using only one additional clock cycle. This requires that the clear pulse is presented at the same time as Y_0, the least significant Y multiplier bit. Since the minimum clear pulse width is 20ns and the clear recovery time is 18ns, the time duration must be at least 38ns minimum for this clock period. A timing diagram for this mode of operation is shown in Figure 7.

Many applications, especially when using two's complement operands, do not required a full n + m bit product but only an m + n−1 bit product. For example, if fractional operands in the number range of −1 to $1-2^{-(n-1)}$ and −1 to $1-2^{-(m-1)}$ are assumed, only the case of −1 times −1 requires m + n bits to represent the product. All other combinations can be represented correctly in two's complement notation by m + n −1 bits. That is, when dealing with fractions, only one bit to the left of the binary point carrying a weight of −1 is required except for the one special case. This can be used to remove one additional clock cycle from the multiplication process as shown in Figure 8. The same reasoning applies to integer representations where the largest negative numbers are $-2^{(m-1)}$ and $-2^{(n-1)}$. Only m + n bits are required to handle the case of $(-2^{(m-1)})(-2^{(n-1)})$. All other products require only m + n−1 bits for a correct two's complement product. Let's take an example. If m = 4 and n = 3, then seven bits are required to represent (−8)•(−4) = (+32) in two's complement. All other products for a 3-bit and 4-bit multiplicand and multiplier can be represented correctly in two's complement form with a 6-bit representation.

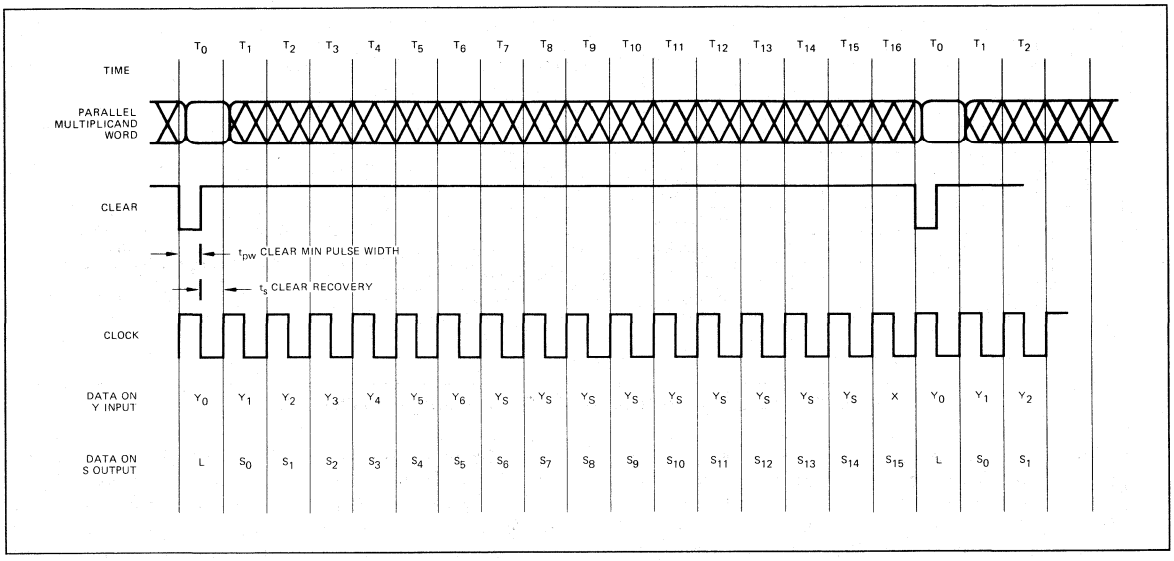


Figure 7. Timing Diagram Showing 17 Clock Cycle Operation of 8 x 8 Multiplication

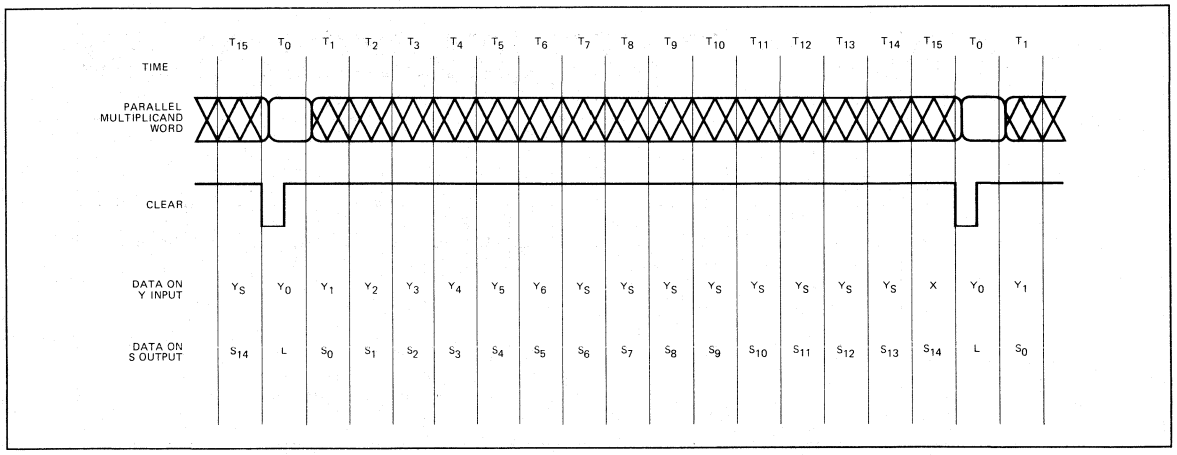


Figure 8. Timing Diagram Showing 16 Clock Cycle Operation for an 8 x 8 Multiplication (Assumes a 15-Bit Product Representation)

ROUNDING AND TRUNCATION

Truncation is performed in the Am25LS14 by ignoring the appropriate number of least significant bits (LSB's). Unfortunately, no clock cycles can be saved when truncating because the product is being developed LSB first. Therefore, the truncated bits are the first bits out of the Am25LS14 multiplier. The subsystem must be clocked the total number of times (m + n) to develop the two's complement product. This does have the advantage of saving register bits to hold the product from the device.

To date, the recommended method of rounding is to use one-fourth of an Am25LS15 to perform rounding. This technique involves adding a one at the bit prior to the LSB of the final product using one input of the Am25LS15. The product from the multiplier is connected to the other input. This does require one extra clock cycle to implement rounding. This technique works for any combination of multiplicand bits, multiplier bits and desired product bits.

APPLICATIONS

Eight-Bit by Eight-Bit Multiplier

A circuit which generates a 16-bit product from an 8-bit by 8-bit multiplication is depicted in Figure 9. This sub-system consists of one Am25LS14 serial/parallel multiplier and two Am25LS22 8-bit registers. This configuration accepts an 8-bit multiplicand and an 8-bit multiplier from an 8-bit data bus. It will return a 16-bit product (8-bit upper byte and 8-bit lower byte) using the same 8-bit bus.

The Am25LS22 is an 8-bit register designed for performing various functions with the Am25LS14. It can be used to hold the multiplier word initially, perform the sign-extend function and then hold part of the product. It has separate serial input/output capability as well as shared parallel input/outputs.

The timing sequence for controlling this circuit is shown in Figure 10. Twenty-two clock cycles are used in this example to fully load, multiply and unload the multiplier subsystem. Thus, such an arrangement can be used with any of the popular 8-bit MOS microprocessors such as the 8080, 6800, 2650, F8 and others. This allows the multiplication to be performed outside of the MOS microprocessor with about two to three orders of magnitude improvement in speed.

Referring to the timing sequence of Figure 10, the multiplier word is loaded into the Am25LS22 register at time T_1 and the multiplicand word is loaded in the Am25LS14 latches during time T_1. The multiplicand and multiplier words must be loaded in this order since there is no hold function on the Am25LS14 multiplier.

During time T_2 through T_{10}, the least significant product bits are generated and clocked into holding register B. Meanwhile the multiplier sign bit is being extended in Register A. The sign extend is performed only for the eight clock cycles T_2 through T_9. During time T_{11} through T_{18}, the most significant 8-bits of the product are developed in the Am25LS14 multiplier. T_8 is used to load the product sign bit from the multiplier into the Am25LS22 B register. During the time T_1 through T_8, the least significant half of the product is transferred from register B to register A. The remaining two clock cycles, T_{19} and T_{20} are used to unload the product upper and lower byte back onto the 8-bit data bus.

The control signals required for this multiplier are shown in Figures 9 and 10. Notice that the clear input to the Am25LS14 and the Serial/Parallel (S/P) input to the Am25LS22 can be connected together with the appropriate don't cares eliminated. Other control signals to the Am25LS22 include the register enable (RE), sign extend (SE), and the three-state control ($\overline{OE}$). These signals can be generated using a counter and combinatorial logic gates or a counter and small PROM.

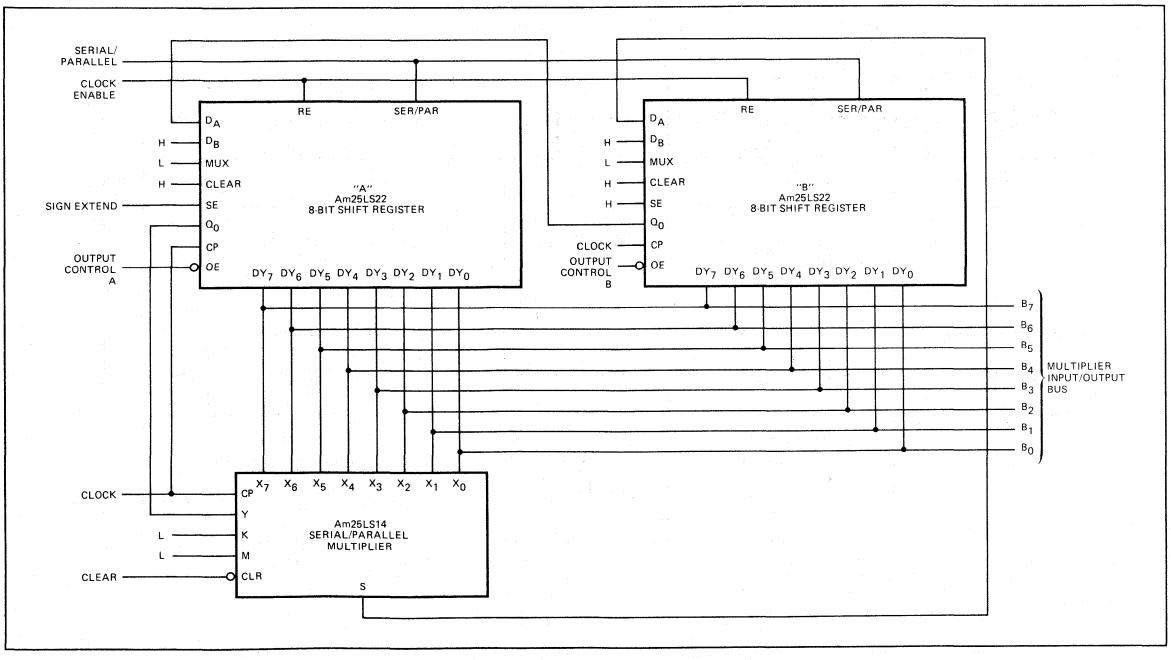


Figure 9. An 8-Bit by 8-Bit Multiplier with a Full 16-Bit Product Store. The Inputs and Outputs are Bus Organized on an 8-Bit Bus

		Am25LS14			Am25LS22's					
TIME	I/O BUS	Y	CLR	S	S/P	RE	SE	$\overline{OE}$ A	$\overline{OE}$ B	FUNCTION
T_0	Multiplier	X	X	X	L	L	X	H	H	Load Multiplier (Y)
T_1	Multiplicand	X	L	X	X	H	X	H	H	Load Multiplicand (X)
T_2	X	Y_0	H	L	H	L	L	H	H	
T_3	X	Y_1	H	S_0	H	L	L	H	H	
T_4	X	Y_2	H	S_1	H	L	L	H	H	
T_5	X	Y_3	H	S_2	H	L	L	H	H	Present Y_i to multiplier. Read S_i into Register B.
T_6	X	Y_4	H	S_3	H	L	L	H	H	Extend Y sign.
T_7	X	Y_5	H	S_4	H	L	L	H	H	
T_8	X	Y_6	H	S_5	H	L	L	H	H	
T_9	X	Y_S	H	S_6	H	L	L	H	H	
T_{10}	X	Y_S	H	S_7	H	L	H	H	H	
T_{11}	X	Y_S	H	S_8	H	L	H	H	H	
T_{12}	X	Y_S	H	S_9	H	L	H	H	H	
T_{13}	X	Y_S	H	S_{10}	H	L	H	H	H	Continue Multiplication using Y_S in register. Load
T_{14}	X	Y_S	H	S_{11}	H	L	H	H	H	least significant part of product into Register A
T_{15}	X	Y_S	H	S_{12}	H	L	H	H	H	and most significant in Register B.
T_{16}	X	Y_S	H	S_{13}	H	L	H	H	H	
T_{17}	X	Y_S	H	S_{14}	H	L	H	H	H	
T_{18}	X	X	H	S_{15}	H	L	H	H	H	Load MSB into Register.
T_{19}	Product Lower Byte	X	X	X	X	H	X	L	H	Unload product Lower byte onto bus.
T_{20}	Product Upper Byte	X	X	X	X	H	X	H	L	Unload product Upper byte onto bus.

H = HIGH L = LOW X = Don't Care

Figure 10. Timing Sequence for an 8 x 8 Multiplier with Full 16-Bit Product Register

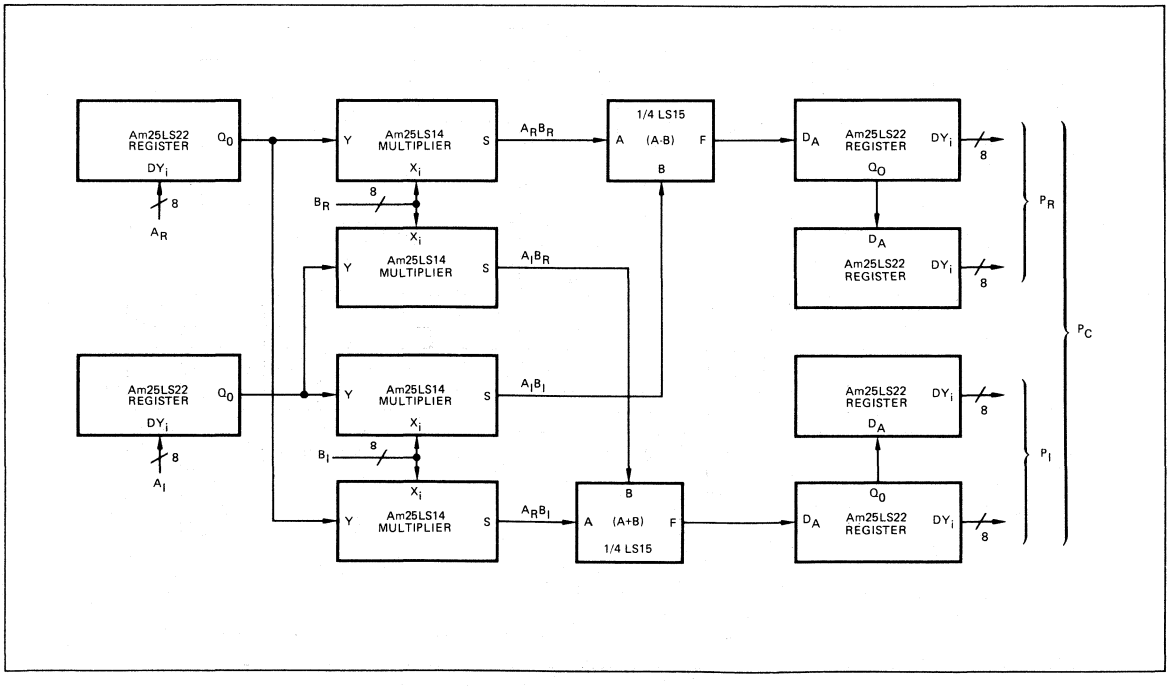


Figure 11. Complex Arithmetic Multiply $P_C = (A_RB_R - A_IB_I) + j(A_RB_I + A_IB_R)$

COMPLEX ARITHMETIC MULTIPLIER

The Am25LS14 serial/parallel multiplier, the Am25LS15 adder/subtractor, and the Am25LS22 eight-bit register can be used to perform rapid multiplication in complex arithmetic processors. In complex arithmetic notation, each variable is assumed to have a real part and an imaginary part. Thus, complex variables A_C and B_C may be represented as:

$$A_C = A_R + jA_I$$
$$B_C = B_R + jB_I$$

The product of A_C and B_C is, of course, complex product P_C where:

$$P_C = P_R + jP_I = A_C B_C$$
$$P_C = (A_R + jA_I)(B_R + jB_I)$$
$$P_C = (A_R B_R - A_I B_I) + j(A_R B_I + A_I B_R)$$

From this discussion, the real and imaginary values of the product P_C are readily identified. These are:

$$P_R = A_R B_R - A_I B_I$$
$$P_I = A_R B_I + A_I B_R$$

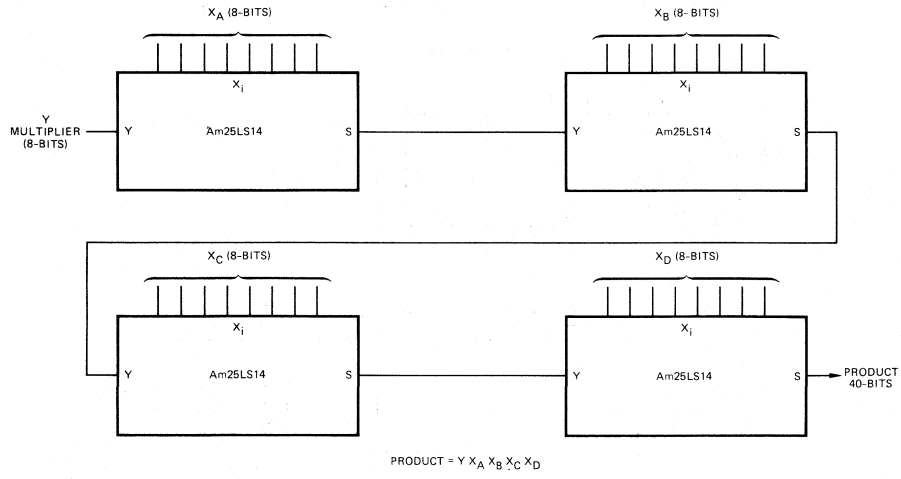
The circuitry required to implement this complex multiplier is shown in Figure 11. In this example, the real and imaginary values of the A_C variable are loaded into the two Am25LS22 registers. The real and imaginary values of the B_C variable are loaded into the latches of the Am25LS14. This loading of the data could be performed simultaneously using all four inputs A_R, A_I, B_R and B_I or it could be performed sequentially using a pair of inputs or a single input at a time.

Once the incoming A_C and B_C data have been loaded, the devices are clocked such that the four intermediate products are formed as shown in Figure 11. Then, two of the four adder/subtractors in the Am25LS15 are used to complete the generation of real product term P_R and the imaginary product term P_I.

These product terms P_R and P_I can be loaded into four additional Am25LS22 registers to hold the double length product terms P_R and P_I (assume least significant bit truncation). After the complex multiplication has been completed, the P_R and P_I variables can be returned to the processor, memory or other destination by using the parallel bus outputs of the Am25LS22.

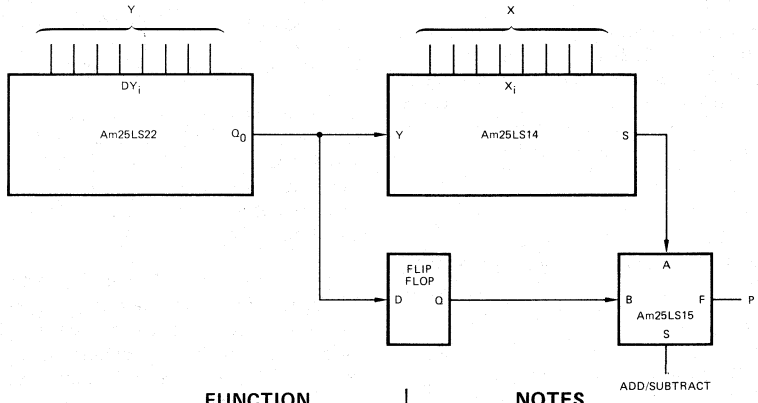
OTHER APPLICATIONS

Other examples of applications using the Am25LS14 as well as the Am25LS15 and Am25LS22 are shown in Figures 12 through 15. Each of these applications is intended to give the design engineer a new approach to solving numerical problems involving digital multiplication.



Four Am25LS14's can be used to implement the product of five variables Y, X_A, X_B, X_C and X_D. If each input variable is eight bits, a 40-bit product results and the multiplier array must be clocked 40 times. This requires the 8-bit Y variable to be sign extended for 32 additional clock cycles.

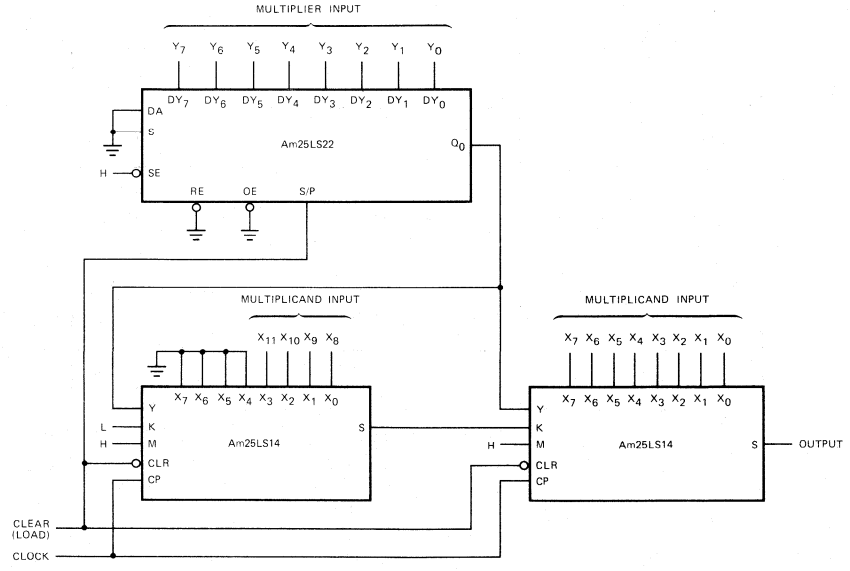
Figure 12. Multiple Operand Multiplications



	FUNCTION		NOTES
1	P = X · Y + Y	= Y (X + 1)	'LS15 in add mode
2	P = X · Y − Y	= Y (X − 1)	'LS15 in subtract mode
3	P = X · Y + Y + 1	= Y (X + 1) + 1	'LS15 is subtract mode for clear and add mode for multiply
4	P = Y − X · Y	= Y (1 − X)	'LS15 A & B inputs reversed

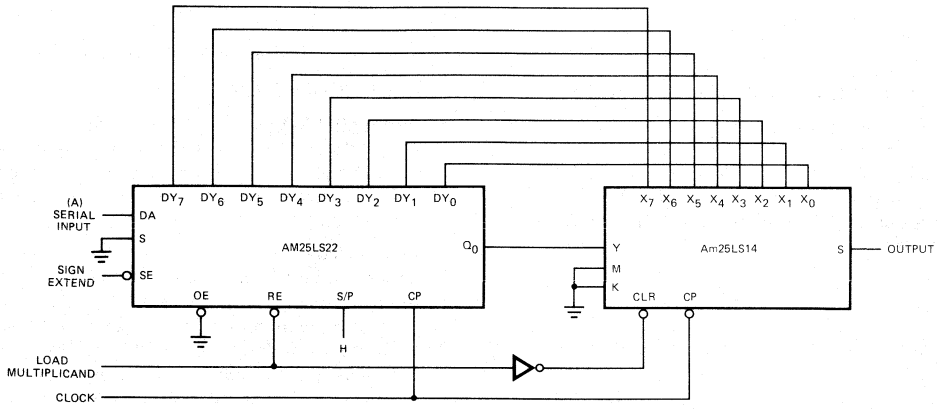
One Am25LS14, Am25LS15 and Am25LS22 can be used to perform several arithmetic functions. Four such functions are shown above. All use a product equal to the multiplicand times the multiplier in combination with a function of the multiplier. Additional combinations are possible, especially if more flip-flops are used to change the relative weight of the multiplier or product function.

Figure 13.



A 12-bit by 8-bit unsigned multiplication is performed by tying the four most significant multiplicand bits LOW to logic zero. The Am25LS22 is loaded with the 8-bit unsigned multiplier. As the multiplier is shifted, a "zero-fill" is accomplished using the D_A input on the Am25LS22. Note the MSB M-input is HIGH on the most significant Am25LS14.

Figure 14.



One Am25LS14 and Am25LS22 can be used to perform the function A^2 on an input variable A. The 8-bit value for A is loaded into the Am25LS22 register in serial form using the D_A input. Once loaded, the A value can be transferred to the Am25LS14 multiplicand latches via the DY_i outputs. Then the product of A·A is formed resulting in A^2 at the Am25LS14 output.

Figure 15.

Am25LS15

Quad Serial Adder/Subtractor

DISTINCTIVE CHARACTERISTICS

- Four independent adder/subtractors
- Use with two's complement arithmetic
- Magnitude only addition/subtraction
- Second sourced by T.I. as Am54LS/74LS385
- 100% product assurance screening to MIL-STD-883 requirements

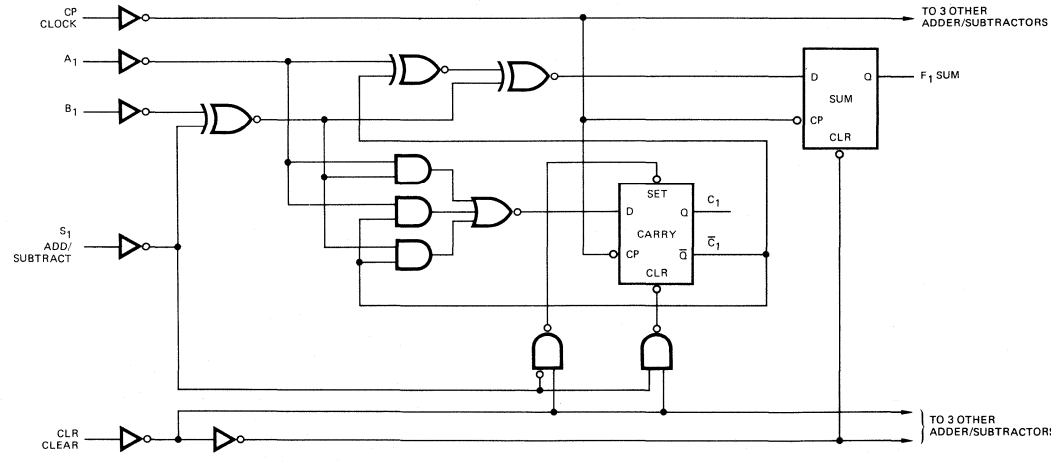
FUNCTIONAL DESCRIPTION

The Am25LS15 is a serial two's complement adder/subtractor designed for use in association with the Am25LS14 serial/parallel two's complement multiplier. This device can also be used for magnitude only or one's complement addition or subtraction.

Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic zero in the add mode and to logic one in subtract mode. This least significant carry is self propagating in the subtract mode as long as zeroes are applied to the A and B inputs at the LSB's. All internal flip-flops change state on the LOW-to-HIGH clock transition.

The Am25LS15 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in Fast Fourier Transforms.

LOGIC DIAGRAM
(One of Four Similar Functions)



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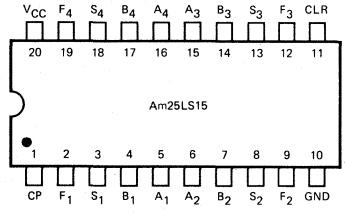
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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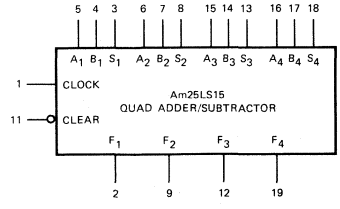
LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

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LECTRICAL CHARACTERISTICS

ıe Following Conditions Apply Unless Otherwise Specified:

)M'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	(MIN. = 4.75V MAX. = 5.25V)
IL	T_A = −55°C to +125°C	V_{CC} = 5.0V ± 10%	(MIN. = 4.50V MAX. = 5.50V)

C CHARACTERISTICS OVER OPERATING RANGE

ıarameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440μA V_{IN} = V_{IH} or V_{IL}	MIL	2.5			Volts
			COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			48	75	mA

otes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs HIGH, measured after a LOW-to-HIGH clock transition.

MAXIMUM RATINGS (Above which the useful life may be impaired)

;torage Temperature	−65°C to +150°C
'emperature (Ambient) Under Bias	−55°C to +125°C
;upply Voltage to Ground Potential Continuous	−0.5V to +7.0V
)C Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
)C Input Voltage	−0.5V to +7.0V
)C Output Current, Into Outputs	30mA
)C Input Current	−30mA to +5.0mA

;WITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

ıarameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Output			14	22	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}				14	22		
t_{PHL}	Clear to Output			20	30	ns	
t_s	A, B, S		10			ns	
t_h			0				
t_s	Clear Recovery		25			ns	
t_h	Clear Hold Time		0			ns	
t_{pw}	Clock	HIGH	17			ns	
		LOW	17				
t_{pw}	Clear LOW		20			ns	
f_{max} (Note 1)	Maximum Clock Frequency		30	40		MHz	

lote 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on the t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output			33		38	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				33		38		
t_{PHL}	Clear to Output			43		50	ns	
t_s	A, B, S		17		20		ns	
t_h			4		5			
t_s	Clear Recovery		37		42		ns	
t_h	Clear Hold Time		4		5		ns	
t_{pw}	Clock	HIGH	26		30		ns	
		LOW	26		30			
t_{pw}	Clear LOW		30		35		ns	
f_{max}(Note 1)	Maximum Clock Frequency		23		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

A_1, A_2, A_3, A_4 The "A" input into each adder/subtractor

B_1, B_2, B_3, B_4 The "B" input into each adder/subtractor

S_1, S_2, S_3, S_4 The add subtract control for each adder/subtractor. When S is LOW, the F function is A+B. When S is HIGH, the F function is A−B.

F_1, F_2, F_3, F_4 The four independent serial outputs of the adder/subtractor.

CP Clock The clock input for the device. All internal flip-flops change state on the LOW-to-HIGH transition.

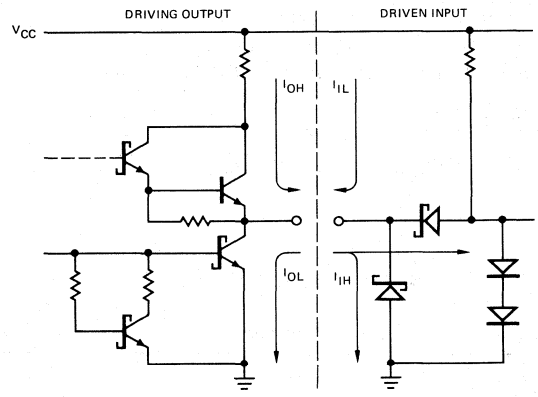
CLR Clear When the clear input is LOW, the four independent adder/subtractors are asynchronously reset. The sum flip-flop is always set to logic "0". The carry flip-flop is set to logic "0" in the add mode and logic "1" in the subtract mode.

FUNCTION TABLE

External Inputs					Internal Point		Output	
CP	CLR	S	A	B	C	C_1	F	Function
X	L	L	X	X	L	L	L	Clear
X	L	H	X	X	H	H	L	
L	H	X	X	X	NC	NC	NC	
H	H	X	X	X	NC	NC	NC	
↑	H	L	L	L	L	L	L	
↑	H	L	L	L	H	L	H	
↑	H	L	L	H	L	L	H	
↑	H	L	L	H	H	H	L	Add
↑	H	L	H	L	L	L	H	
↑	H	L	H	L	H	H	L	
↑	H	L	H	H	L	H	L	
↑	H	L	H	H	H	H	H	
↑	H	H	L	L	L	L	H	
↑	H	H	L	L	H	H	L	
↑	H	H	L	H	L	L	L	
↑	H	H	L	H	H	L	H	Subtract
↑	H	H	H	L	L	H	L	
↑	H	H	H	L	H	H	H	
↑	H	H	H	H	L	L	H	
↑	H	H	H	H	H	H	L	

C = Data In the Carry Flip-Flop Before the Clock Transition
C_1 = Data In the Carry Flip-Flop After the Clock
X = Don't Care
NC = No Change
H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATIONS

The normal butterfly network associated with the Cooley-Tukey Fast Fourier Transform (FFT) algorithm is shown below. Here we assume A, B, C, D and W are all complex numbers such that:

$A = A_R + jA_I$

$B = B_R + jB_I$

$W = W_R + jW_I$

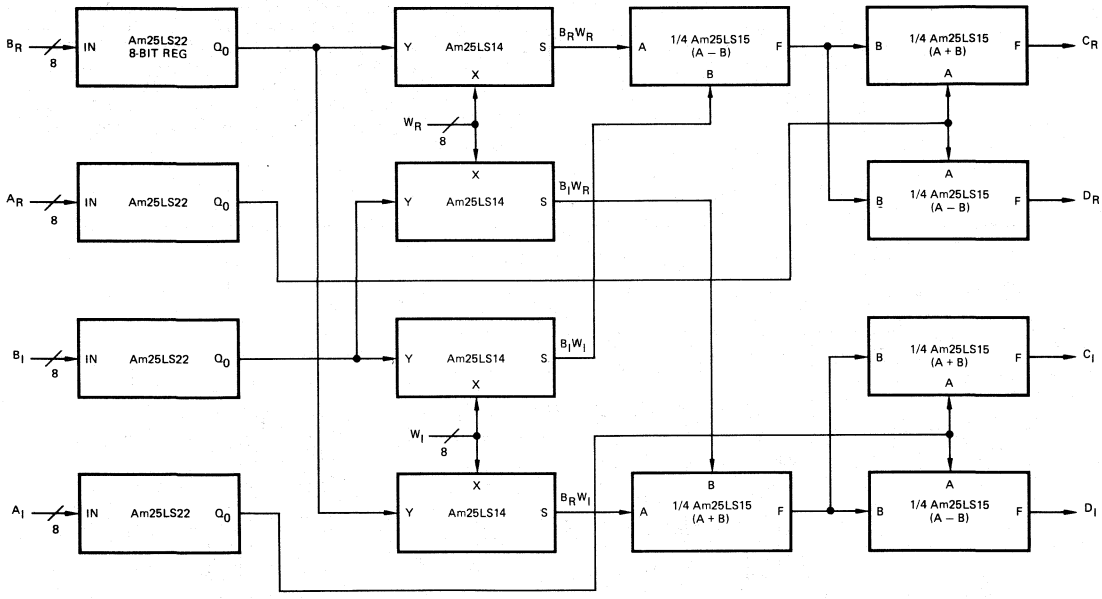
The outputs C and D are also complex numbers and are evaluated as:

$C = C_R + jC_I = (A_R + B_R W_R - B_I W_I) + j(A_I + B_R W_I + B_I W_R)$

$D = C_R + jD_I = (A_R - B_R W_R + B_I W_I) + j(A_I - B_R W_I - B_I W_R)$

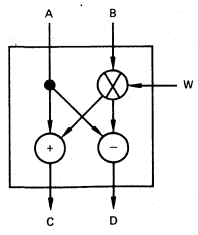
The four multiplications can be implemented using four Am25LS14 serial-parallel multipliers (the appropriate number of bits must, of course, be used). The additions and the subtractions are implemented using the Am25LS15 quad serial adder/subtractors. This diagram depicts only the basic data flow; binary weighting of the numbers, rounding, truncation, etc. must be handled as required by the individual design parameters.

FAST FOURIER TRANSFORM (FFT) BUTTERFLY

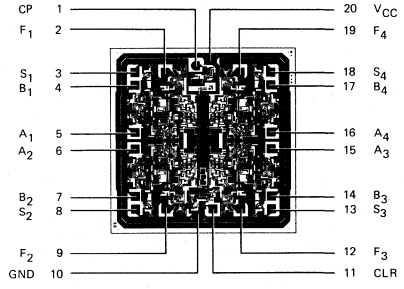


An FFT butterfly connection for complex arithmetic inputs and outputs.

Functional Diagram for FFT Butterfly Connection



Metallization and Pad Layout



DIE SIZE 0.095" X 0.095"

Am25LS22

8-Bit Serial/Parallel Register With Sign Extend

DISTINCTIVE CHARACTERISTICS

- Three-state outputs with multiplexed input
- Multiplexed serial data input
- Sign extend function
- Second sourced by T.I. as Am54LS/74LS322
- 100% product assurance screening to MIL-STD-883 requirements

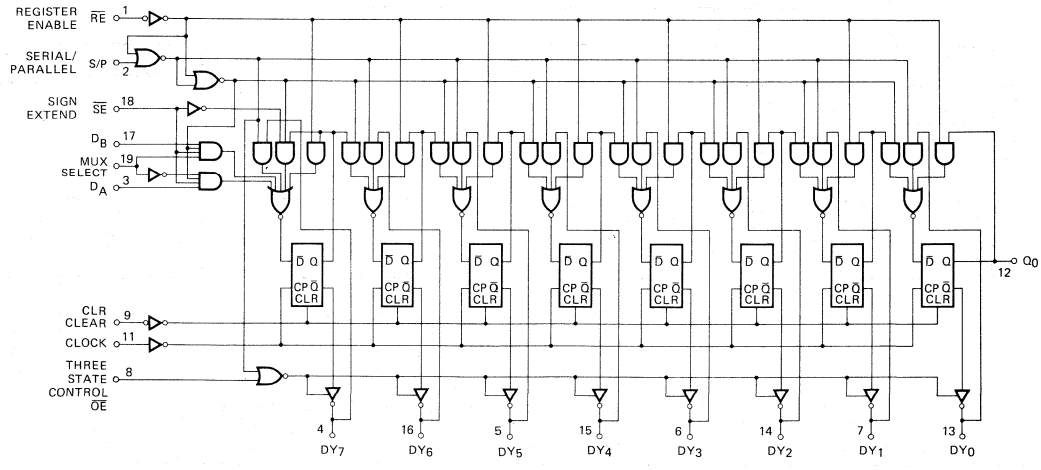
FUNCTIONAL DESCRIPTION

The Am25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input D_A or D_B. A serial output, Q_0, is also provided.

The Am25LS22 is specifically designed for operation with the Am25LS14 serial/parallel two's complement multiplier and provides the sign extend function required for this device.

When the Register Enable ($\overline{RE}$) input is HIGH, the register will retain its current contents. Synchronous parallel loading is accomplished by applying a LOW to $\overline{RE}$ and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of $\overline{OE}$ and allows data that is applied on the input/output lines (DY_i) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend ($\overline{SE}$) input is used to repeat the sign in the Q_7 flip-flop. This occurs whenever $\overline{SE}$ is LOW when the SHIFT mode is selected. When $\overline{SE}$ is high, the serial two-input multiplexer is enabled. Thus, either D_A or D_B can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

LOGIC DIAGRAM



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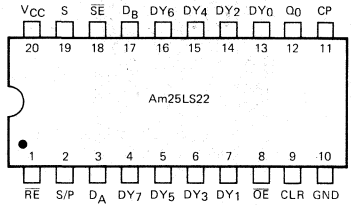
CONNECTION DIAGRAM

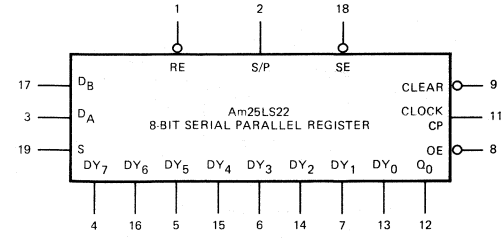
Top View



Note: Pin 1 is marked for orientation.

MPR-334

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-335

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q_0, $I_{OH} = -440\mu A$	MIL	2.5			Volts
				COM'L	2.7			
			DY_i, $I_{OH} = -1.0mA$	MIL	2.4			
			DY_i, $I_{OH} = -2.6mA$	COM'L	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$		$\overline{SE}$			−1.08	mA
				S			−0.72	
				Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$ (Except DY_i)		$\overline{SE}$			60	µA
				S			40	
				Others			20	
I_I	Input HIGH Current	V_{CC} = MAX., (Except DY_i)	$V_{IN} = 7.0V$	$\overline{OE}$, S/P, RE, CP, CLR			0.1	mA
			$V_{IN} = 5.5V$	$\overline{SE}$			0.3	
				S			0.2	
				Others			0.1	
I_{OZ}	Off State (High Impedance) Output Current (DY_i)	V_{CC} = MAX.	$V_O = 2.4V$				40	µA
			$V_O = 0.4V$				−100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.				40	65	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage ($\overline{OE}$, S/P, RE, CP, CLR)	−0.5V to +7.0V
DC Input Voltage (Others)	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to DY_i		16.5	24	ns	R_L = 2.0kΩ, C_L = 15pF
t_{PHL}			18	26		
t_{PHL}	Clear to DY_i		23	30	ns	
t_{PLH}	Clock to Q_0		16.5	24	ns	
t_{PHL}			18	26		
t_{PHL}	Clear to Q_0		23	30	ns	
t_{ZH}	$\overline{OE}$ to DY_i		13	21	ns	
t_{ZL}			18	26		
t_{HZ}			13	21		R_L = 2.0kΩ, C_L = 5pF
t_{LZ}			18	26		
t_{ZH}	SER/PAR to DY_i		18	26	ns	R_L = 2.0kΩ, C_L = 15pF
t_{ZL}			23	32		
t_{HZ}			18	26		R_L = 2.0kΩ, C_L = 5pF
t_{LZ}			23	32		
t_s	RE to Clock	20			ns	R_L = 2.0kΩ, C_L = 15pF
t_s	SE to Clock	10				
t_s	S to Clock	15				
t_s	D_A and D_B to Clock	15				
t_s	DY_i (Load) to Clock	15				
t_s	Clear Recovery to Clock	8.0				
t_s	S/P to Clock	15			ns	
t_h	Any Input	0				
t_h	Clear Hold	0			ns	
t_{pw}	Clock HIGH	8.0			ns	
	Clock LOW	8.0				
t_{pw}	Clear	20			ns	
f_{max} (Note 1)	Maximum Clock Frequency	35	50		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

FUNCTION TABLE

Mode	INPUTS							OUTPUTS								
	Clear	Register Enable	Serial/ Parallel	Sign Extend	Mux Select	$\overline{OE}$*	Clock	DY_7	DY_6	DY_5	DY_4	DY_3	DY_2	DY_1	DY_0	Q_0
Clear	L	H	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	L	H	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	L	L	X	X	L	X	Z	Z	Z	Z	Z	Z	Z	Z	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_0
Shift Right	H	L	H	H	L	L	↑	D_A	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
	H	L	H	H	H	L	↑	D_B	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Sign Extend	H	L	H	L	X	L	↑	Y_{7n}	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

L = LOW
H = HIGH
↑ = Clock LOW-to-HIGH Transition
NC = No Change
X = Don't Care
Z = High-Impedance Output State

*When the OE input is HIGH, all input/output terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

D_7, D_6. . . D_0 = the level of the steady-state input at the respective DY_n terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the DY_n terminal.

D_A, D_B = the level of the steady-state inputs to the serial multiplexer input.

Y_{7n}, Y_{6n}. . . Y_{0n} = the level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to DY_i			35		41	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				38		44		
t_{PHL}	Clear to DY_i			43		50	ns	
t_{PLH}	Clock to Q_0			35		41	ns	
t_{PHL}				38		44		
t_{PHL}	Clear to Q_0			43		50	ns	
t_{ZH}	OE to DY_i			32		36	ns	
t_{ZL}				38		44		
t_{HZ}				28		31		C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				34		39		
t_{ZH}	SER/PAR to DY_i			38		44	ns	C_L = 50pF, R_L = 2.0kΩ
t_{ZL}				46		53		
t_{HZ}				34		39		C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				42		48		
t_S	RE to Clock		30		35			C_L = 50pF, R_L = 2.0kΩ
t_S	SE to Clock		17		20			
t_S	S to Clock		24		27		ns	
t_S	D_A and D_B to Clock		24		27			
t_S	DY_i (Load) to Clock		24		27			
t_S	Clear Recovery to Clock		15		17			
t_S	S/P to Clock		24		27		ns	
t_h	Any Input		4		5			
t_h	Clear Hold		4		5		ns	
t_{pw}	Clock	HIGH	15		17		ns	
		LOW	15		17			
t_{pw}	Clear		30		35		ns	
f_{max} (Note 1)	Maximum Clock Frequency		26		23		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

DY_i The multiplexed parallel input/output port to the device. Data may be parallel loaded into the register or data can be read in parallel from the register on these pins. These outputs can be forced to the high-impedance state, i = 0 through 7.

Q_0 The continuous output from the Q_0 flip-flop of the register. This output is used for serial shifting.

$\overline{RE}$ Register Enable. When $\overline{RE}$ is LOW, the register functions are enabled. When $\overline{RE}$ is HIGH, the register functions (parallel load, shift right and sign extend) are inhibited.

S/P Serial/Parallel. When S/P is LOW, the register can be synchronously parallel loaded. This input forces the register output buffers to the high-impedance state independent of the $\overline{OE}$ input. When S/P is HIGH, the register contents are shifted right on the clock LOW-to-HIGH transition.

$\overline{SE}$ Sign Extend. When the $\overline{SE}$ input is LOW, the contents of the Q_7 flip-flop will be repeated in the Q_7 flip-flop as the register is shifted right. When $\overline{SE}$ is HIGH, the two-input multiplexer (D_A and D_B) is enabled to enter data during the serial shift right. The Q_7 flip-flop (DY_7) is normally considered the MSB of the register for arithmetic definitions.

D_A, D_B The serial inputs to the device.

S Multiplexer Select. When S is LOW, the D_A serial input is selected. When S is HIGH, the D_B serial input is selected.

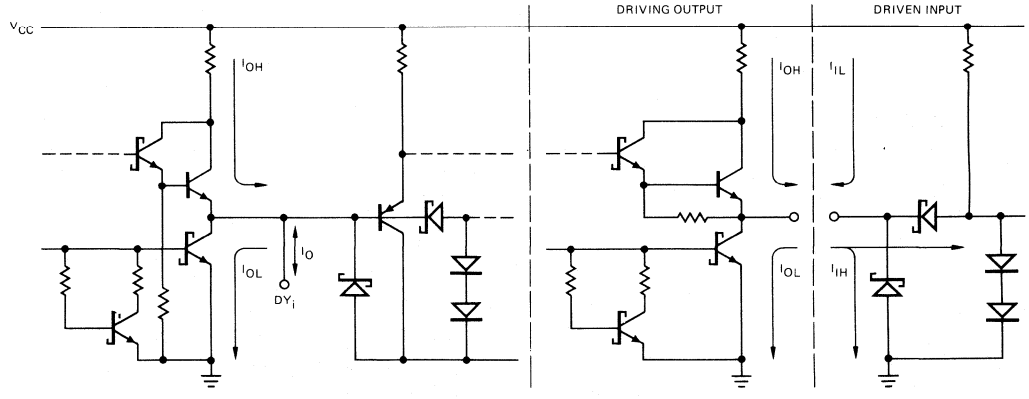
CLR Clear. The asynchronous clear to the register. When the clear is LOW, the outputs of the flip-flops are set LOW independent of all other inputs. When the clear is HIGH, the register will perform the selected function.

CP Clock. The clock pulse for the register. Register operations occur on the LOW-to-HIGH transition of the clock pulse.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the eight DY_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, data in the eight flip-flops will be present at the register parallel outputs unless S/P is LOW.

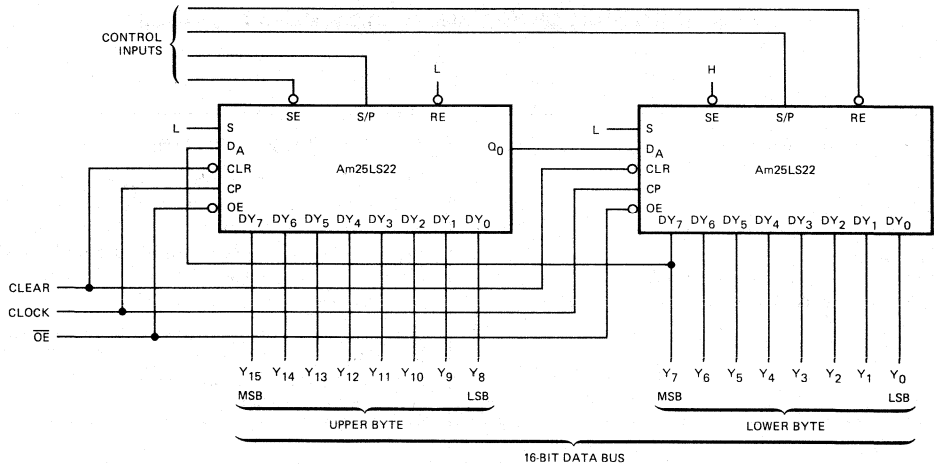
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

DY_i Only | **Other Pins**



Note: Actual current flow direction shown.

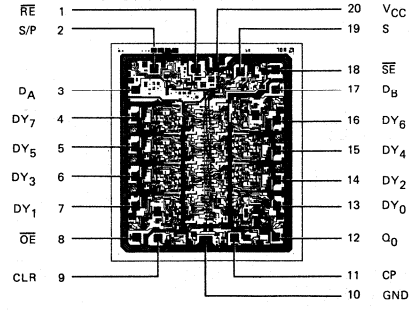
APPLICATION



SYSTEM OPERATION	Am25LS22 UPPER BYTE				Am25LS22 LOWER BYTE				FUNCTION
	$\overline{SE}$	S/P	$\overline{RE}$	$\overline{OE}$	$\overline{SE}$	S/P	$\overline{RE}$	$\overline{OE}$	Description
Load lower byte and extend lower byte sign to upper byte	H	H	L	X	X	L	L	X	Load from Bus
	L	H	L	H	X	X	H	H	7 clock cycles to extend sign
Load upper byte and extend upper byte sign while shifting value to lower byte position	X	L	L	X	X	X	X	X	Load from Bus
	H	H	L	H	H	H	L	H	8 clock cycles to extend upper byte sign and shift upper byte into lower byte position
Read 16-bit word to Bus	X	X	X	L	X	X	X	L	Unload

Two Am25LS22 8-bit registers can be used to perform the sign extend associated with two's complement 8-bit bytes for arithmetic operations in a 16-bit machine. If the upper byte value is to be used, it is shifted to the lower bit positions and its sign is extended. If the lower byte value is to be used, it is held in place while the sign is extended downward from the MSB position of the upper byte.

Metallization and Pad Layout



DIE SIZE 0.096" X 0.112"

Am25LS23

8-Bit Shift/Storage Register with Synchronous Clear

DISTINCTIVE CHARACTERISTICS

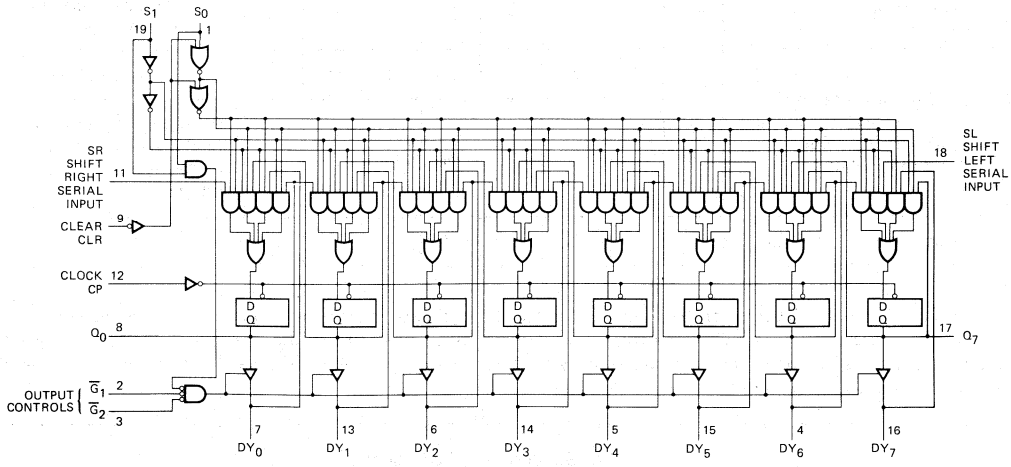
- Synchronous clear
- Three-state outputs
- Common input/output pins
- Cascadable shifting
- Second sourced by T.I. as 54LS/74LS323
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

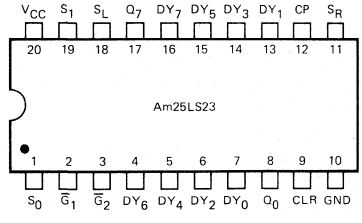
The Am25LS23 is an 8-bit universal shift/storage register with 3-state outputs. The function is similar to the Am25LS299 with the exception of a synchronous clear function. Parallel load inputs and register outputs are multiplexed to allow the use of a 20-pin package. Separate continuous outputs are also provided for flip-flops Q_0 and Q_7.

Four modes of operation are possible – Hold (store), Shift-left, Shift-right and Load Data. The Am25LS23 has a typical shift frequency of 50MHz. The Am25LS23 is packaged in a standard 20-pin package.

LOGIC DIAGRAM

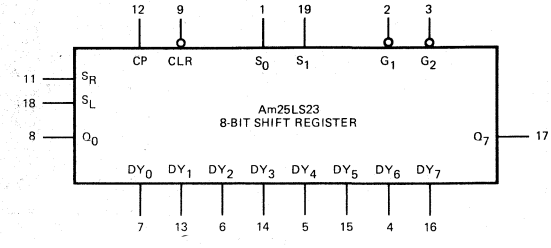


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LECTRICAL CHARACTERISTICS The following conditions apply unless otherwise specified:

OM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
IIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

)C CHARACTERISTICS OVER OPERATING RANGE

arameters	Description	Test Conditions (Note 1)				Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{OL}	Q_0, Q_7	$I_{OH} = -440\mu A$	MIL	2.5			Volts
					COM'L	2.7			
			$DY_0 - DY_7$	MIL, $I_{OH} = -1.0mA$		2.4			
				COM'L, $I_{OH} = -2.6mA$		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}		$I_{OL} = 4.0mA$			0.25	0.4	Volts
				$I_{OL} = 8.0mA$			0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$			S_0, S_1			−0.8	mA
					All others			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$ (Except DY_i)			S_0, S_1			40	μA
					All others			20	
I_I	Input HIGH Current	V_{CC} = MAX., (Except DY_i)	$V_{IN} = 7V$		S_0, S_1			0.2	mA
					$\overline{G}_1, \overline{G}_2$, CLR, CP			0.1	
			$V_{IN} = 5.5V$		Others			0.1	
I_{OZ}	Off-State (High Impedance) Output Current	V_{CC} = MAX.			$V_O = 0.4V$			−100	μA
					$V_O = 2.4V$			40	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.				−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)					38	60	mA

lotes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time.
4. I_{CC} – measured with clock input HIGH and output controls HIGH.

IAXIMUM RATINGS (Above which the useful life may be impaired)

torage Temperature	−65°C to +150°C
emperature (Ambient) Under Bias	−55°C to +125°C
upply Voltage to Ground Potential Continuous	−0.5V to +7.0V
C Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
C Input Voltage (S_0, S_1, $\overline{G}_1$, $\overline{G}_2$, CLR, CP)	−0.5V to +7.0V
C Input Voltage (Others)	−0.5V to +5.5V
C Output Current, Into Outputs	30mA
C Input Current	−30mA to +5.0mA

WITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

arameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q_0 or Q_7		18	26	ns	$C_L = 15pF$ $R_L = 2.0k\Omega$
t_{PHL}			23	28		
t_{PLH}	Clock to DY_i		18	26	ns	
t_{PHL}			21	28		
t_s	S_1, S_0 Set-up Prior to Clock	12			ns	
t_s	DY_i or S_R, S_L Set-up Prior to Clock	12			ns	
t_{PW}	Pulse Width (Clock)	15			ns	
t_s	Clear to Clock	15			ns	
t_{ZH}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i		18	30	ns	
t_{ZL}			20	30		
t_{LZ}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$, to DY_i		22	33	ns	$C_L = 5.0pF$ $R_L = 2.0k\Omega$
t_{HZ}			16	23		
f_{max}	Maximum Clock Frequency (Note 1)	35	50		MHz	

lote 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Q_0 or Q_7		38		44	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			40		47		
t_{PLH}	Clock to DY_i		38		44	ns	
t_{PHL}			40		47		
t_S	S_1, S_0 Set-up Prior to Clock	20		23		ns	
t_S	DY_i or S_R, S_L Set-up Prior to Clock	20		23		ns	
t_{pw}	Pulse Width (Clock)	24		27		ns	
t_S	Clear to Clock	24		27		ns	
t_{ZH}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i		43		50	ns	
t_{ZL}			43		50		
t_{LZ}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i		43		50	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			30		35		
f_{max}	Maximum Clock Frequency (Note 1)	26		23		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

S_R Shift right data input to Q_7

S_L Shift left data input to Q_0

Clear Active LOW synchronous input forcing the Q_0 through Q_7 register to see LOW conditions, visable only if outputs are enabled

Clock A LOW-to-HIGH transition will result in the register changing state to next state as described by mode and input data condition

S_0, S_1 Mode selection control lines used to control input (output during load) conditions

$\overline{G}_1$, $\overline{G}_2$ Active LOW input to control three-state output in active LOW AND configuration

Q_0, Q_7 The only two direct outputs; used to cascade shift operations

DY_0–DY_7 Input/Output line dependent on mode and output control. Input only with mode select LOAD. Output in all other modes but subject to output select ($\overline{G}_1$, $\overline{G}_2$).

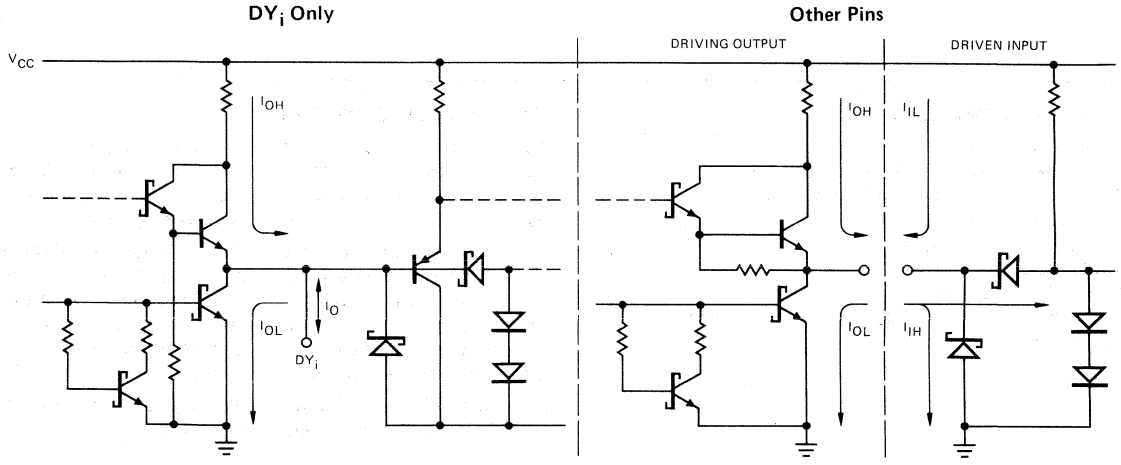
TRUTH TABLE

FUNCTION		INPUTS S_R	S_L	CLEAR	CLOCK	S_0	S_1	$\overline{G}_1$	$\overline{G}_2$	OUTPUTS Q_0	Q_7	INPUTS/OUTPUTS DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7
Clear		X	X	L	↑	(Note 1)		L	L	L	L	L	L	L	L	L	L	L	L
Output Control		X	X	X	X	X	X	H	L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	L	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	H	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
	Hold	X	X	H	X	L	L	L	L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
M	Load (Note 2)	X	X	H	↑	H	H	L	L	A	H	A	B	C	D	E	F	G	H
O	Shift Right	L	X	H	↑	H	L	L	L	L	DY_6	L	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
D	Shift Right	H	X	H	↑	H	L	L	L	H	DY_6	H	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
E	Shift Left	X	L	H	↑	L	H	L	L	DY_1	L	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	L
	Shift Left	X	H	H	↑	L	H	L	L	DY_1	H	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	H

L = LOW, H = HIGH, Z = High Impedance, X = Don't Care, ↑ = Transition LOW-to-HIGH, NC = No Change

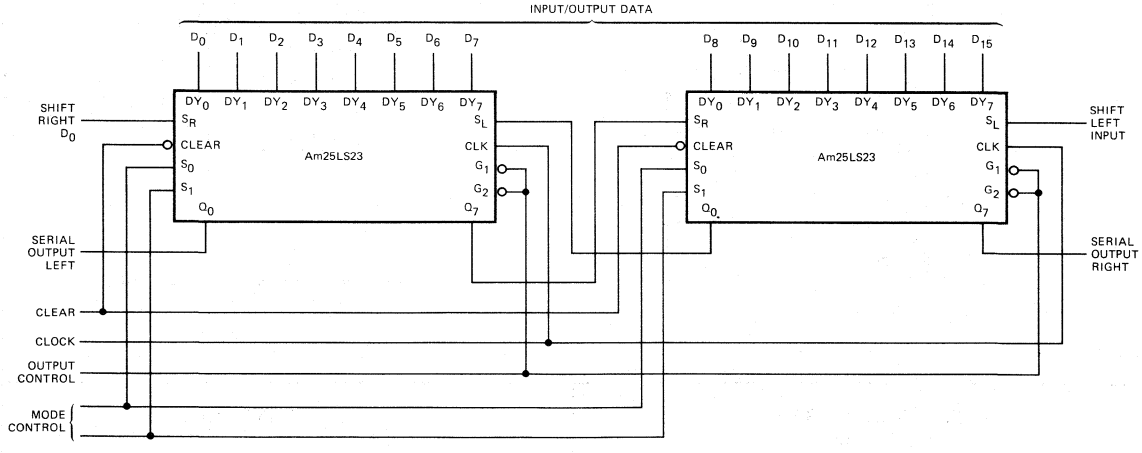
Notes: 1. Either LOW to observe outputs.
2. In this mode DY_i are inputs.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



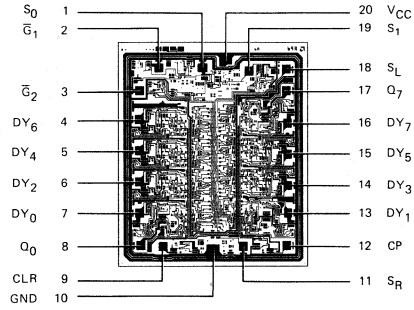
Note: Actual current flow direction shown.

APPLICATION



16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register.

Metallization and Pad Layout



DIE SIZE
0.096" X 0.112"

Am25LS240 • Am54LS/74LS240

Octal Three-State Inverting Drivers

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times – 18ns MAX.
- Enable-to-output – 30ns MAX.
- Am25LS240 specified at 48mA output current
- 20 pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

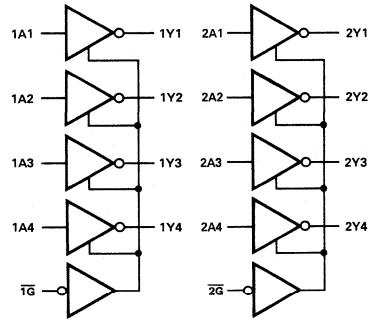
FUNCTIONAL DESCRIPTION

The 'LS240 is an octal inverting line driver fabricated using advanced low-power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

Three-state outputs are provided to drive bus lines directly. The Am25LS240 is specified at 48mA and 24mA output sink current, while the Am54/74LS240 is guaranteed at 12mA over the military range and 24mA over the commercial range. Four buffers are enabled from one common line and the other four from a second enable line.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

LOGIC DIAGRAM

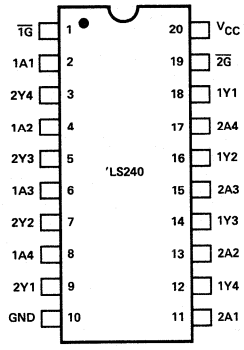


INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Note: All devices have input hysteresis.

LIC-331

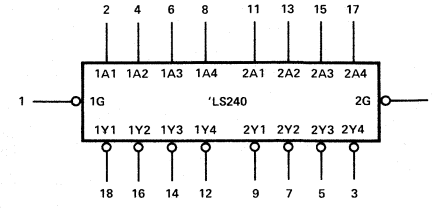
CONNECTION DIAGRAM
Top View



LIC-332

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LIC-333

Am25LS240
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage		V_{CC} = MIN., V_{IH} = 2.0V I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.		2.4	3.4		Volts
			V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
				COM'L, I_{OH}= −15mA	2.0			
V_{OL}	Low-Level Output Voltage		V_{CC} = MIN.	All I_{OL} = 12mA		0.25	0.4	Volts
				All I_{OL} = 24mA		0.35	0.5	
				COM'L I_{OL} = 48mA			0.55	
V_{IH}	High-Level Input Voltage		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Low-Level Input Voltage	COM'L					0.8	Volts
		MIL					0.7	
V_{IK}	Input Clamp Voltage		V_{CC} = MIN., I_I = −18mA				−1.5	Volts
	Hysteresis (V_{T+} − V_{T-})		V_{CC} = MIN.		0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = MAX. V_{IH} = 2.0V V_{IL} = V_{IL}MAX.	V_O = 2.7V			20	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied			V_O = 0.4V			−20	
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX., V_I = 7.0V				0.1	mA
I_{IH}	High-Level Input Current, Any Input		V_{CC} MAX., V_{IH} = 2.7V				20	μA
I_{IL}	Low-Level Input Current		V_{CC} = MAX., V_{IL} = 0.4V				−200	μA
I_{SC}	Short Circuit Output Current (Note 3)		V_{CC} = MAX.		−40		−225	mA
I_{CC}	Supply Current	V_{CC} = MAX. Outputs open	All Outputs HIGH			13	23	mA
			All Outputs LOW			26	44	
			Outputs at Hi-Z			29	50	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS240
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

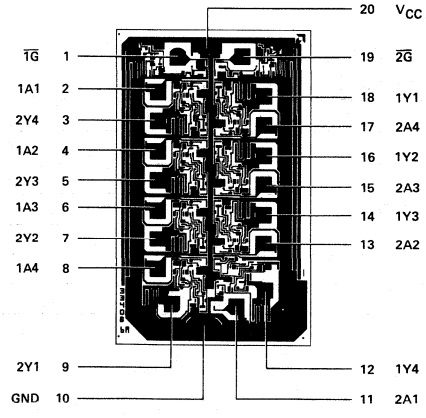
MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage		V_{CC} = MIN., V_{IH} = 2.0V, I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.		2.4	3.4		Volts
			V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
				COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage		V_{CC} = MIN.	All, I_{OL} = 12mA		0.25	0.4	Volts
				COM'L, I_{OL} = 24mA		0.35	0.5	
V_{IH}	High-Level Input Voltage		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Low-Level Input Voltage	COM'L					0.8	Volts
		MIL					0.7	
V_{IK}	Input Clamp Voltage		V_{CC} = MIN., I_I = −18mA				−1.5	Volts
	Hysteresis (V_{T+} − V_{T-})		V_{CC} = MIN.		0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.	V_O = 2.7V			20	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied			V_O = 0.4V			−20	
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX., V_I = 7.0V				0.1	mA
I_{IH}	High-Level Input Current, Any Input		V_{CC} MAX., V_{IH} = 2.7V				20	μA
I_{IL}	Low-Level Input Current		V_{CC} = MAX., V_{IL} = 0.4V				−200	μA
I_{SC}	Short Circuit Output Current (Note 3)		V_{CC} = MAX.		−40		−225	mA
I_{CC}	Supply Current	V_{CC} = MAX. Outputs open	All Outputs HIGH			13	23	mA
			All Outputs LOW			26	44	
			Outputs at Hi-Z			29	50	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Metallization and Pad Layout



DIE SIZE .056" X .089"

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

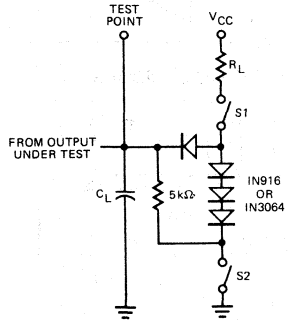
Parameters	Description	Am25LS240 Min.	Am25LS240 Typ.	Am25LS240 Max.	Am54LS/74LS240 Min.	Am54LS/74LS240 Typ.	Am54LS/74LS240 Max.	Units	Test Conditions (Notes 1–5)
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		8.0	12		9.0	14	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		12	16		12	18	ns	
t_{PZL}	Output Enable Time to Low Level		19	27		20	30	ns	
t_{PZH}	Output Enable Time to High Level		14	20		15	23	ns	
t_{PLZ}	Output Disable Time from Low Level		14	23		15	25	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		10	18		10	18	ns	

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%) Min.	Am25LS COM'L Max.	Am25LS MIL (T_A = −55°C to +125°C, V_{CC} = 5.0V ±10%) Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		16		19	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		22		25	ns	
t_{PZL}	Output Enable Time to Low Level		37		42	ns	
t_{PZH}	Output Enable Time to High Level		27		31	ns	
t_{PLZ}	Output Disable Time from Low Level		31		36	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		25		28	ns	

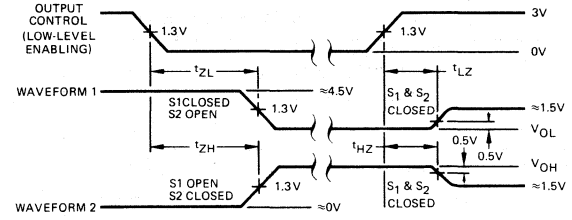
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



LIC-334

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



LIC-335

Notes:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, Z_{OUT} ≈ 50Ω and t_r ≤ 2.5ns, t_f ≤ 2.5ns.

Am25LS241 • Am54LS/74LS241
Am25LS244 • Am54LS/74LS244

Octal Three-State Buffers

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times – 18ns MAX.
- Enable-to-output – 30ns MAX.
- Am25LS241 and 244 specified at 48mA output current
- 20 pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The 'LS241 and 'LS244 are octal buffers fabricated using advanced low-power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

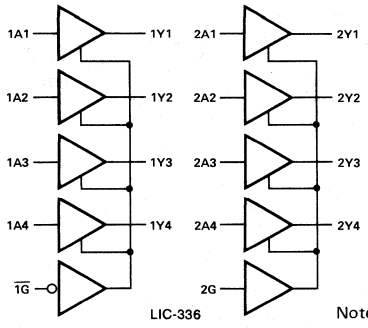
Three-state outputs are provided to drive bus lines directly. The Am25LS241 and Am25LS244 are specified at 48mA and 24mA output sink current, while the Am54LS/74LS241 and Am54LS/74LS244 are guaranteed at 12mA over the military range and 24mA over the commercial range. Four buffers are enabled from one common line and the other four from a second enable line.

The 'LS241 has enable inputs of opposite polarity to allow use as a transceiver without overlap. The 'LS244 enables are of similar polarity for use as a unidirectional buffer in which both halves are enabled simultaneously.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

LOGIC DIAGRAMS

'LS241

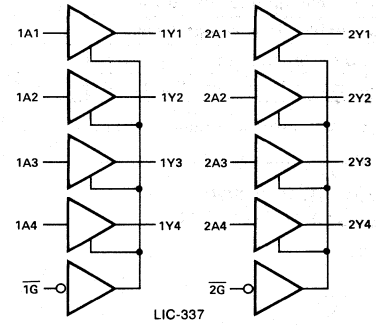


LIC-336

'LS241

INPUTS			OUTPUTS
$\overline{1G}$	2G	A	Y
H	L	X	Z
L	H	H	H
L	H	L	L

'LS244



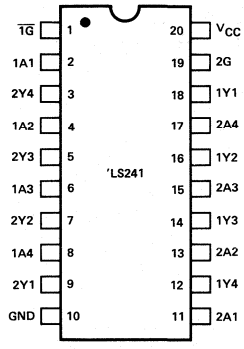
LIC-337

'LS244

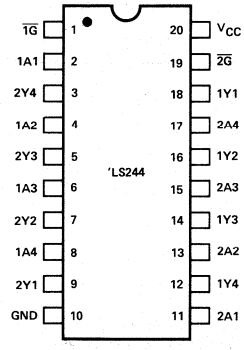
INPUTS		OUTPUT
$\overline{G}$	A	
H	X	Z
L	H	H
L	L	L

Note: All devices have input hysteresis.

CONNECTION DIAGRAMS
Top Views



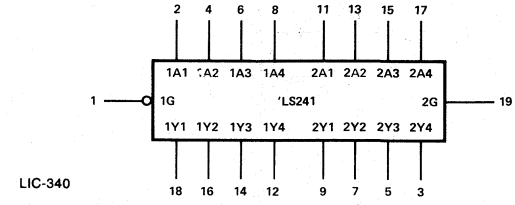
LIC-338



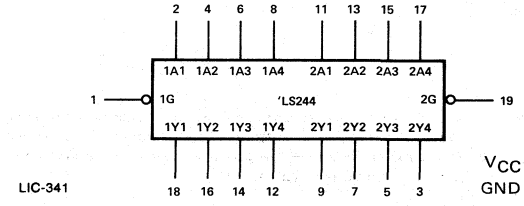
LIC-339

Note: Pin 1 is marked for orientation.

LOGIC SYMBOLS



LIC-340



LIC-341

V_{CC} = Pin 20
GND = Pin 10

Am25LS241•Am25LS244
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage		V_{CC} = MIN., V_{IH} = 2.0V I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.		2.4	3.4		Volts
			V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
				COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage		V_{CC} = MIN.	All I_{OL} = 12mA		0.25	0.4	Volts
				All I_{OL} = 24mA		0.35	0.5	
				COM'L, I_{OL} = 48mA			0.55	
V_{IH}	High-Level Input Voltage		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Low-Level Input Voltage	COM'L					0.8	Volts
		MIL					0.7	
V_{IK}	Input Clamp Voltage		V_{CC} = MIN., I_I = −18mA				−1.5	Volts
	Hysteresis (V_{T+} − V_{T-})		V_{CC} = MIN.		0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.	V_O = 2.7V			20	µA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied			V_O = 0.4V			−20	
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX., V_I = 7.0V				0.1	mA
I_{IH}	High-Level Input Current, Any Input		V_{CC} = MAX., V_{IH} = 2.7V				20	µA
I_{IL}	Low-Level Input Current		V_{CC} = MAX., V_{IL} = 0.4V				−200	µA
I_{SC}	Short Circuit Output Current (Note 3)		V_{CC} = MAX.		−40		−225	mA
I_{CC}	Supply Current	V_{CC} = MAX. Outputs open	All Outputs HIGH			13	23	mA
			All Outputs LOW			27	46	
			Outputs at Hi-Z			32	54	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS241•Am54LS/74LS244
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

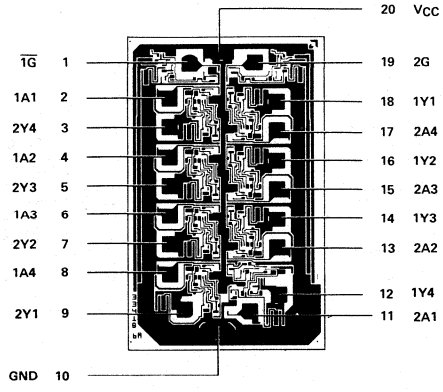
DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage		V_{CC} = MIN., V_{IH} = 2.0V I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.		2.4	3.4		Volts
			V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
				COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage		V_{CC} = MIN.	All, I_{OL} = 12mA		0.25	0.4	Volts
				COM'L, I_{OL} = 24mA		0.35	0.5	
V_{IH}	High-Level Input Voltage		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Low-Level Input Voltage	COM'L					0.8	Volts
		MIL					0.7	
V_{IK}	Input Clamp Voltage		V_{CC} = MIN., I_I = −18mA				−1.5	Volts
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN.		0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = MAX. V_{IH} = 2.0V V_{IL} = V_{IL}MAX.	V_O = 2.7V			20	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied			V_O = 0.4V			−20	
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX., V_I = 7.0V				0.1	mA
I_{IH}	High-Level Input Current, Any Input		V_{CC} = MAX., V_{IH} = 2.7V				20	μA
I_{IL}	Low-Level Input Current		V_{CC} = MAX., V_{IL} = 0.4V				−200	μA
I_{SC}	Short Circuit Output Current (Note 3)		V_{CC} = MAX.		−40		−225	mA
I_{CC}	Supply Current	V_{CC} = MAX. Outputs open	All Outputs HIGH			13	23	mA
			All Outputs LOW			27	46	
			Outputs at Hi-Z			32	54	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

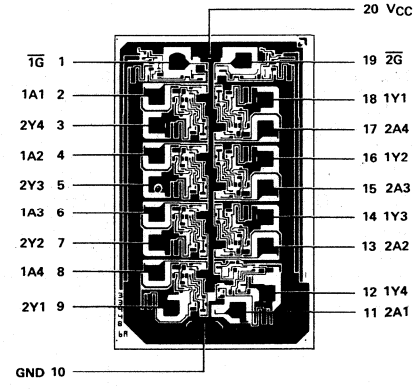
Metallization and Pad Layouts

'LS241



DIE SIZE .056" X .089"

'LS244



DIE SIZE .056" X .089"

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

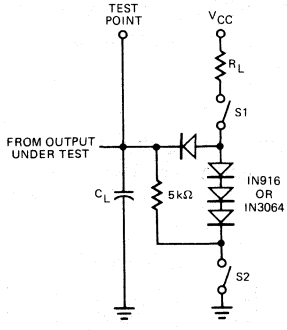
Parameters	Description	Am25LS241 Am25LS244 Min.	Typ.	Max.	Am54LS/74LS241 Am54LS/74LS244 Min.	Typ.	Max.	Units	Test Conditions (Notes 1–5)
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		10	15		12	18	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		12	18		12	18	ns	
t_{PZL}	Output Enable Time to Low Level		20	30		20	30	ns	
t_{PZH}	Output Enable Time to High Level		15	23		15	23	ns	
t_{PLZ}	Output Disable Time from Low Level		15	25		15	25	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		10	18		10	18	ns	

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		21		24	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		25		28	ns	
t_{PZL}	Output Enable Time to Low Level		41		47	ns	
t_{PZH}	Output Enable Time to High Level		31		47	ns	
t_{PLZ}	Output Disable Time from Low Level		34		36	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		25		28	ns	

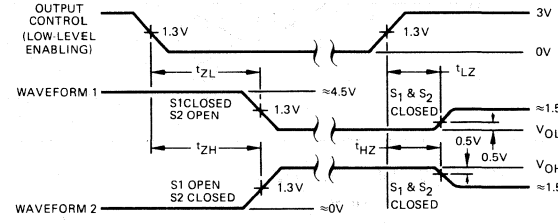
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



LIC-342

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



LIC-343

Notes:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR ≤ 1.0MHz, Z_{OUT} ≈ 50Ω, t_r ≤ 15ns, t_f ≤ 6ns.
5. When measuring t_{PLH} and t_{PHL}, switches S_1 and S_2 are closed.

Am25LS242 • Am54LS/74LS242
Am25LS243 • Am54LS/74LS243

Quad Bus Transceivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data to output propagation delay times – 18ns MAX.
- Enable to output – 30ns MAX.
- Am25LS242 and Am25LS243 are specified at 48mA output current
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The 'LS242 and 'LS243 are quad bus transceivers designed for asynchronous two-way communications between data buses.

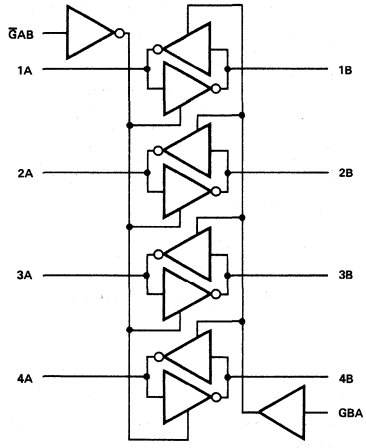
The 'LS242 and 'LS243 have the two 4-line data paths connected input-to-output on both sides to form an asynchronous transceiver/buffer with complementing enable inputs. The 'LS242 is inverting, while the 'LS243 presents non-inverting data at the outputs.

Three-state outputs are provided to drive bus lines directly. The Am25LS242 and Am25LS243 are specified at 48mA and 24mA output sink current, while the Am54/74LS242 and 243 are guaranteed at 12mA over the military range and 24mA over the commercial range.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

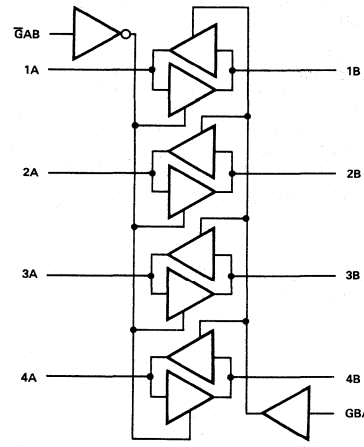
LOGIC DIAGRAMS

Am54LS/74LS242



LIC-344

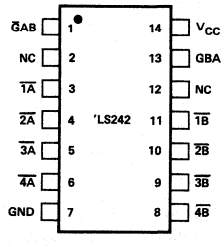
Am54LS/74LS243



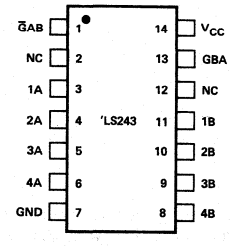
LIC-345

Note: All devices have input hysteresis.

CONNECTION DIAGRAMS
Top Views



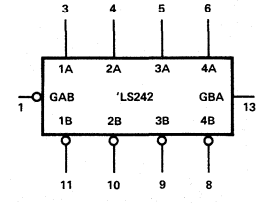
LIC-346



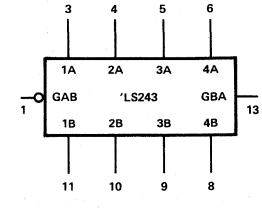
LIC-347

Note: Pin 1 is marked for orientation

LOGIC SYMBOLS



LIC-348



LIC-349

V_{CC} = Pin 14
GND = Pin 7

Am25LS242 • Am25LS243

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage		V_{CC} = MIN., V_{IH} = 2.0V I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.		2.4	3.4		Volts
			V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
				COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage		V_{CC} = MIN.	All I_{OL} = 12mA		0.25	0.4	Volts
				All I_{OL} = 24mA		0.35	0.5	
				COM'L, I_{OL} = 48mA			0.55	
V_{IH}	High-Level Input Voltage		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Low-Level Input Voltage	COM'L					0.8	Volts
		MIL					0.7	
V_{IK}	Input Clamp Voltage		V_{CC} = MIN., I_I = −18mA				−1.5	Volts
	Hysteresis (V_{T+} − V_{T-})		V_{CC} = MIN.		0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = MAX. V_{IH} = 2.0V V_{IL} = V_{IL}MAX.	V_O = 2.7V			40	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied			V_O = 0.4V			−200	
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX.	V_I = 7.0V, $\overline{G}$AB or GBA			0.1	mA
				V_I = 5.5V, A or B			0.1	mA
I_{IH}	High-Level Input Current, Any Input		V_{CC} = MAX., V_{IH} = 2.7V				20	μA
I_{IL}	Low-Level Input Current		V_{CC} = MAX., V_{IL} = 0.4V				−200	μA
I_{SC}	Short Circuit Output Current (Note 3)		V_{CC} = MAX.		−40		−225	mA
I_{CC}	Supply Current	V_{CC} = MAX. Outputs open (Note 4)	All Outputs HIGH	'LS242, 'LS243		22	38	mA
			All Outputs LOW	'LS242, 'LS243		29	50	
			Outputs at Hi-Z	'LS242		29	50	
				'LS243		32	54	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.

2. All typical values are V_{CC} = 5.0V, T_A = 25°C.

3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

4. For 'LS242 and 'LS243 I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS242 • Am54LS/74LS243
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage		V_{CC} = MIN., V_{IH} = 2.0V I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.		2.4	3.4		Volts
			V_{CC} = MIN.,	MIL, I_{OH} = −12mA	2.0			
			V_{IL} = 0.5V	COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage		V_{CC} = MIN.	All, I_{OL} = 12mA		0.25	0.4	Volts
				COM'L, I_{OL} = 24mA		0.35	0.5	
V_{IH}	High-Level Input Voltage		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Low-Level Input Voltage	COM'L					0.8	Volts
		MIL					0.7	
V_{IK}	Input Clamp Voltage		V_{CC} = MIN., I_I = −18mA				−1.5	Volts
	Hysteresis (V_{T+} − V_{T-})		V_{CC} = MIN.		0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = MAX. V_{IH} = 2.0V V_{IL} = V_{IL}MAX.	V_O = 2.7V			40	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied			V_O = 0.4V			−200	
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX.	V_I = 7.0V, $\overline{G}$AB or GBA			0.1	mA
				V_I = 5.5V, A or B			0.1	mA
I_{IH}	High-Level Input Current, Any Input		V_{CC} MAX., V_{IH} = 2.7V				20	μA
I_{IL}	Low-Level Input Current		V_{CC} = MAX., V_{IL} = 0.4V				−200	μA
I_{SC}	Short Circuit Output Current (Note 3)		V_{CC} = MAX.		−40		−225	mA
I_{CC}	Supply Current	V_{CC} = MAX. Outputs open (Note 4)	All Outputs HIGH	'LS242, 'LS243		22	38	mA
			All Outputs LOW	'LS242, 'LS243		29	50	
			Outputs at Hi-Z	'LS242		29	50	
				'LS243		32	54	

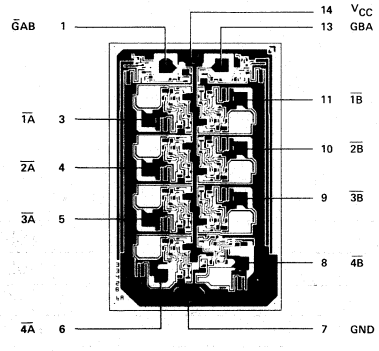
Notes: 1. For conditions shown as MIN' or MAX., use the appropriate value specified under recommended operating conditions.

2. All typical values are V_{CC} = 5.0V, T_A = 25°C.

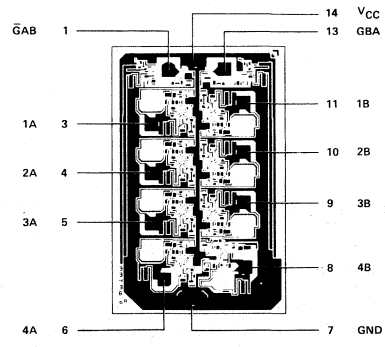
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

4. For 'LS242 and 'LS243 I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

Metallization and Pad Layouts



DIE SIZE .056" X .089"



DIE SIZE .056" X .089"

Am25LS242•Am54LS/74LS242 SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25LS242 Min.	Am25LS242 Typ.	Am25LS242 Max.	Am54LS/74LS242 Min.	Am54LS/74LS242 Typ.	Am54LS/74LS242 Max.	Units	Test Conditions (Notes 1–5)
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		8.0	12		9.0	14	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		12	16		12	18	ns	C_L = 45pF, R_L = 667Ω
t_{PZL}	Output Enable Time to Low Level		20	30		20	30	ns	C_L = 45pF, R_L = 667Ω
t_{PZH}	Output Enable Time to High Level		15	23		15	23	ns	C_L = 45pF, R_L = 667Ω
t_{PLZ}	Output Disable Time from Low Level		15	25		15	25	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		10	18		10	18	ns	C_L = 5.0pF, R_L = 667Ω

Am25LS242 ONLY SWITCHING CHARACTERISTICS OVER OPERATION RANGE*

Parameters	Description	Am25LS COM'L: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL: T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		16		19	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		22		25	ns	C_L = 45pF, R_L = 667Ω
t_{PZL}	Output Enable Time to Low Level		37		42	ns	C_L = 45pF, R_L = 667Ω
t_{PZH}	Output Enable Time to High Level		29		33	ns	C_L = 45pF, R_L = 667Ω
t_{PLZ}	Output Disable Time from Low Level		33		38	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		25		28	ns	C_L = 5.0pF, R_L = 667Ω

Am25LS243•Am54LS/74LS243 SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

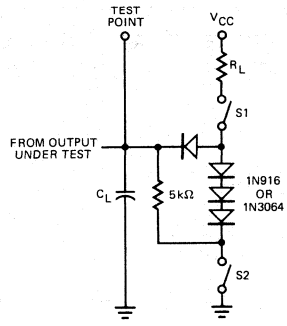
Parameters	Description	Am25LS243 Min.	Am25LS243 Typ.	Am25LS243 Max.	Am54LS/74LS243 Min.	Am54LS/74LS243 Typ.	Am54LS/74LS243 Max.	Units	Test Conditions (Notes 1–5)
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		10	15		12	18	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		12	18		12	18	ns	C_L = 45pF, R_L = 667Ω
t_{PZL}	Output Enable Time to Low Level		20	30		20	30	ns	C_L = 45pF, R_L = 667Ω
t_{PZH}	Output Enable Time to High Level		15	23		15	23	ns	C_L = 45pF, R_L = 667Ω
t_{PLZ}	Output Disable Time from Low Level		15	25		15	25	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		10	18		10	18	ns	C_L = 5.0pF, R_L = 667Ω

Am25LS243 ONLY SWITCHING CHARACTERISTICS OVER OPERATION RANGE*

Parameters	Description	Am25LS COM'L: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL: T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		21		24	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		25		28	ns	C_L = 45pF, R_L = 667Ω
t_{PZL}	Output Enable Time to Low Level		41		47	ns	C_L = 45pF, R_L = 667Ω
t_{PZH}	Output Enable Time to High Level		33		49	ns	C_L = 45pF, R_L = 667Ω
t_{PLZ}	Output Disable Time from Low Level		36		38	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		25		28	ns	C_L = 5.0pF, R_L = 667Ω

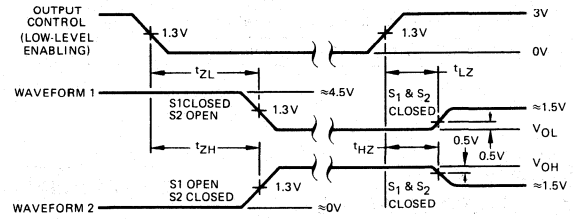
SWITCHING CHARACTERISTICS TEST CONDITIONS

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



LIC-350

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



LIC-351

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR ≤ 1MHz, $Z_{OUT} \approx 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6$ns.
5. When measuring t_{PLH} and t_{PHL}, switches S_1 and S_2 are closed.

FUNCTION TABLES

Am54LS/74LS242

CONTROL INPUTS		DATA OUTPUTS	
$\overline{G}AB$	GBA	A	B
H	H	$\overline{O}$	I
L	H	*	*
H	L	ISOLATED	
L	L	I	$\overline{O}$

I = Input
O = Output
$\overline{O}$ = Inverting Output
H = HIGH
L = LOW

Am54LS/74LS243

CONTROL INPUTS		DATA OUTPUTS	
$\overline{G}AB$	GBA	A	B
H	H	O	I
L	H	*	*
H	L	ISOLATED	
L	L	I	O

*Possible destructive oscillation may occur if the transceivers are enable in both directions at once.

Am25LS273 • Am25LS273B
Am54LS/74LS273

8-Bit Register with Clear
8-Bit Register with Clear and Buffered Outputs

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high-speed parallel registers
- Clock to output delay – 15ns (typ) on Am25LS273
- Buffered outputs to eliminate output commutation on Am25LS273B
- Positive edge-triggered D-type flip-flops
- Common clock and common clear
- Am25LS devices offer the following improvements over Am54/74LS
  - 50mV lower V_{OL} at I_{OL} = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

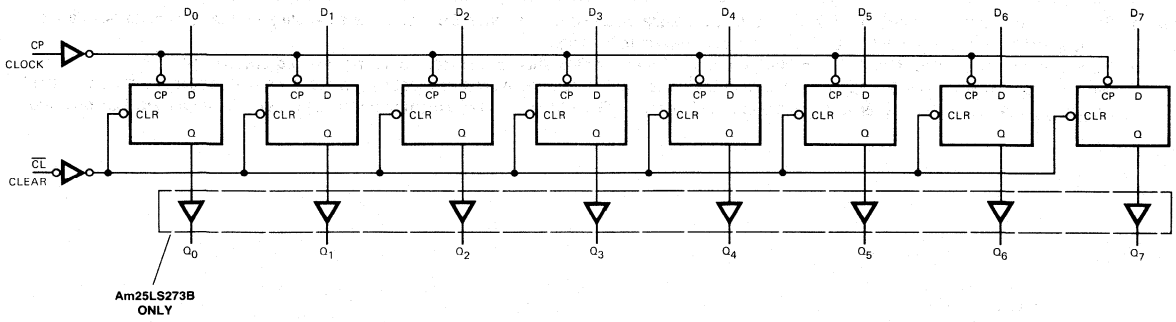
FUNCTIONAL DESCRIPTION

The Am25LS273, Am25LS273B and the Am54LS/74LS273 are eight-bit registers built using Advanced Low-Power Schottky Technology. These registers consist of D-type flip-flops with a buffer common clock and an asynchronous active LOW buffered common clear.

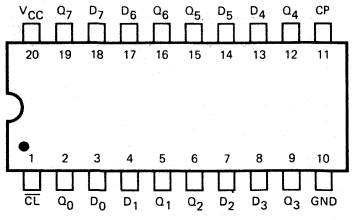
When the clear input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input. These devices are supplied in the 20-pin space saving package featuring 0.3-inch centers between rows of leads.

The Am25LS273 and Am54LS/74LS273 are designed for maximum speed. The Am25LS273B has an additional output buffer to eliminate output commutation.

LOGIC DIAGRAM

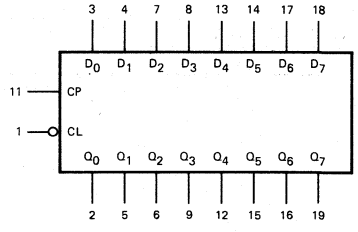


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Am25LS273 • Am25LS273B
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440μA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−20		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			17	27	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. (a) All outputs open and 4.5 V applied to the data and clear input. Measured after a momentary ground, then 4.5V applied to the clock input.
(b) All outputs open, 4.5V applied to the clear input, all D_i inputs = GND. Measure after a momentary ground, then 4.5V applied to the clock input.

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS273

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	All, I_{OL} = 4.0 mA			0.4	Volts
			74LS only, I_{OL} = 8.0 mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18 mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0 V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−20		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			17	27	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. (a) All outputs open and 4.5 V applied to the data and clear input. Measured after a momentary ground, then 4.5V applied to the clock input.
(b) All outputs open, 4.5V applied to the clear input, all D_i inputs = GND. Measure after a momentary ground, then 4.5V applied to the clock input.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{CL}$ Clear. When the clear is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear is HIGH, data can be entered in the register.

CP Clock pulse for the register. Enters data on the positive transition.

Q_i The TRUE register outputs.

FUNCTION TABLE

INPUTS			OUTPUT
Clear	Clock	D_i	Q_i
L	X	X	L
H	L	X	NC
H	H	X	NC
H	↑	L	L
H	↑	H	H

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
X = Don't Care
NC = No Change

Am25LS273 • Am54LS/74LS273 SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	Clock to Output			15	23		17	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}	Clock to Output			15	23		18	27	ns	
t_{PHL}	Clear to Output			18	27		18	27	ns	
t_{pw}	Clock Pulse Width	HIGH	15			20			ns	
		LOW	15			20				
t_{pw}	Clear Pulse Width		15			20			ns	
t_s	Data Set-up		20			20			ns	
t_h	Data Hold		5			5			ns	
t_s	Set-up, Clear Recovery (In-Active) to Clock		25			25			ns	
f_{max} (Note 1)	Maximum Clock Frequency		30	40		30	40		MHz	

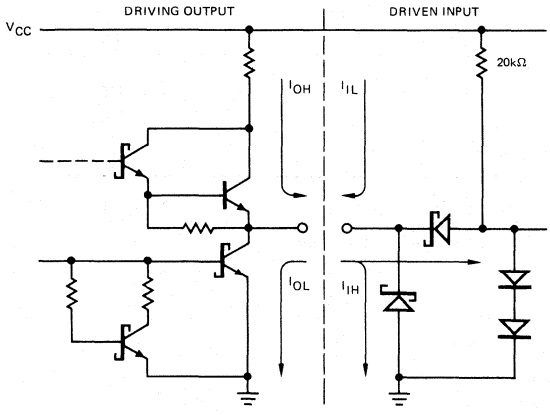
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constaints on t_r, t_f, pulse width or duty cycle.

Am25LS273 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output			28		30	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}	Clock to Output			31		37		
t_{PHL}	Clear to Output			37		45	ns	
t_{pw}	Clock Pulse Width	HIGH	17		20		ns	
		LOW	20		27			
t_{pw}	Clear Pulse Width		17		20		ns	
t_s	Data Set-up		22		25		ns	
t_h	Data Hold		0		0		ns	
t_s	Set-up, Clear Recovery (In-Active) to Clock		30		33		ns	
f_{max} (Note 1)	Maximum Clock Frequency		25		20		MHz	

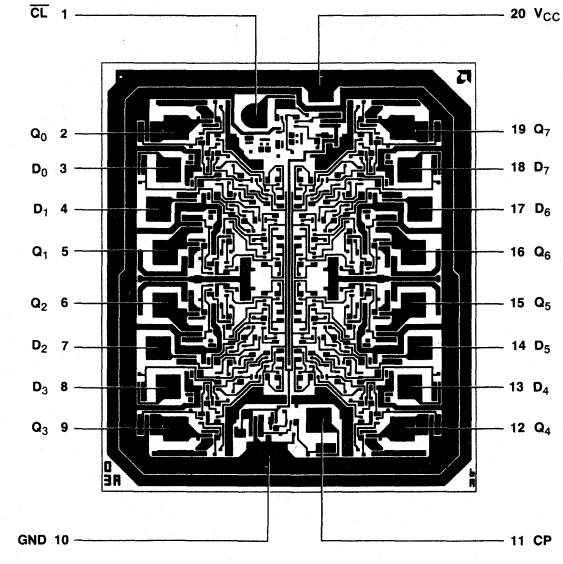
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Metallization and Pad Layout Am25LS/54LS/74LS273



DIE SIZE .072" X .083"

Am25LS273B
SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Am25LS273B Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Output			21	32	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}				26	38		
t_{PHL}	Clear to Output			28	39	ns	
t_{pw}	Clock Pulse Width	HIGH	20			ns	
		LOW	25				
t_{pw}	Clear Pulse Width		25			ns	
t_S	Data Set-up		20			ns	
t_h	Data Hold		10			ns	
t_S	Set-up, Clear Recovery (In-Active) to Clock		25			ns	
f_{max} (Note 1)	Maximum Clock Frequency		30	40		MHz	

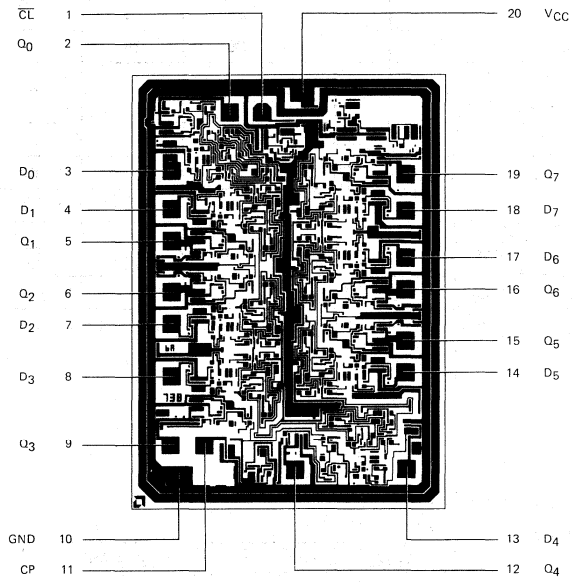
Note: 1.Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS273B
SWITCHING CHARACTERISTICS
OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	Clock to Output			36		40	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}				49		60		
t_{PHL}	Clear to Output			50		60	ns	
t_{pw}	Clock Pulse Width	HIGH	25		30		ns	
		LOW	30		35			
t_{pw}	Clear Pulse Width		25		25		ns	
t_s	Data Set-up		20		20		ns	
t_h	Data Hold		12		15		ns	
t_s	Set-up, Clear Recovery (In-Active) to Clock		25		25		ns	
f_{max} (Note 1)	Maximum Clock Frequency		25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Metallization and Pad Layout
Am25LS273B

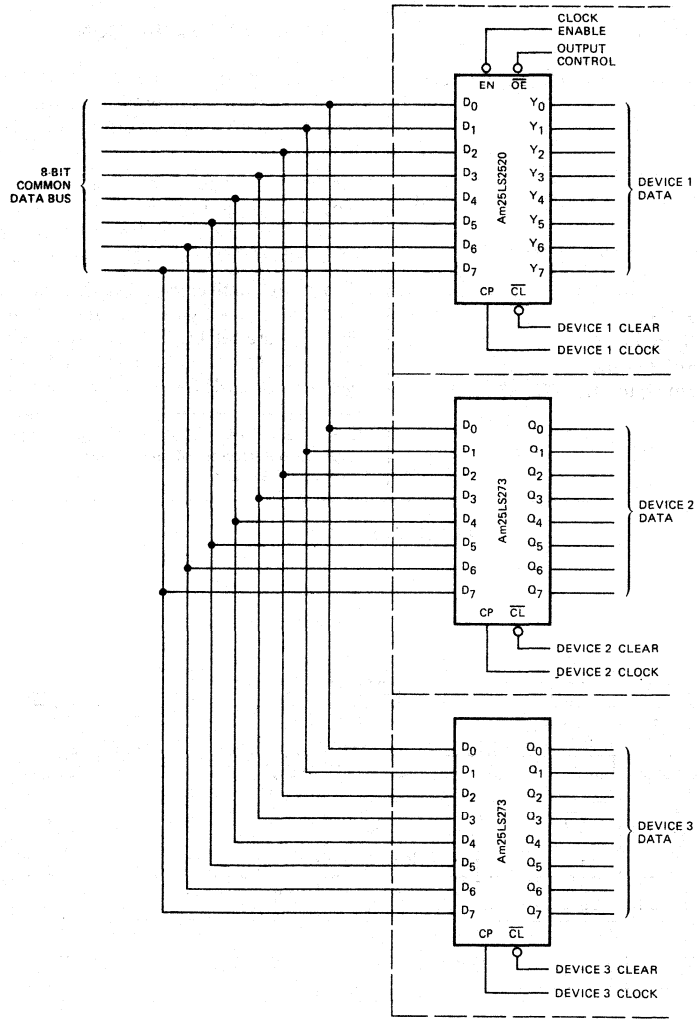


DIE SIZE 0.080" X 0.111"

ORDERING INFORMATION

Package Type	Temperature Range	Am25LS273 Order Number	Am25LS273B Order Number	Am54LS/ 74LS273 Order Number
Molded DIP	0°C to +70°C	AM25LS273PC	AM25LS273BPC	SN74LS273N
Hermetic DIP	0°C to +70°C	AM25LS273DC	AM25LS273BDC	SN74LS273J
Dice	0°C to +70°C	AM25LS273XC	AM25LS273BXC	SN74LS273X
Hermetic DIP	−55°C to +125°C	AM25LS273DM	AM25LS273BDM	SN54LS273J
Hermetic Flat Pak	−55°C to +125°C	AM25LS273FM	AM25LS273BFM	SN54LS273W
Dice	−55°C to +125°C	AM25LS273XM	AM25LS273BXM	SN54LS273X

APPLICATION



Am25LS273 8-bit registers are shown used as device data input registers on a common 8-bit data bus.

Am25LS299 • Am54LS/74LS299

8-Bit Universal Shift/Storage Register

DISTINCTIVE CHARACTERISTICS

- Four operational modes: shift left, shift right, parallel load, hold
- Common input/output pins
- Three-state outputs
- Buffered asynchronous master clear
- Separate shift right serial input and shift left serial input for easy cascadability
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL} at I_{OL} = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

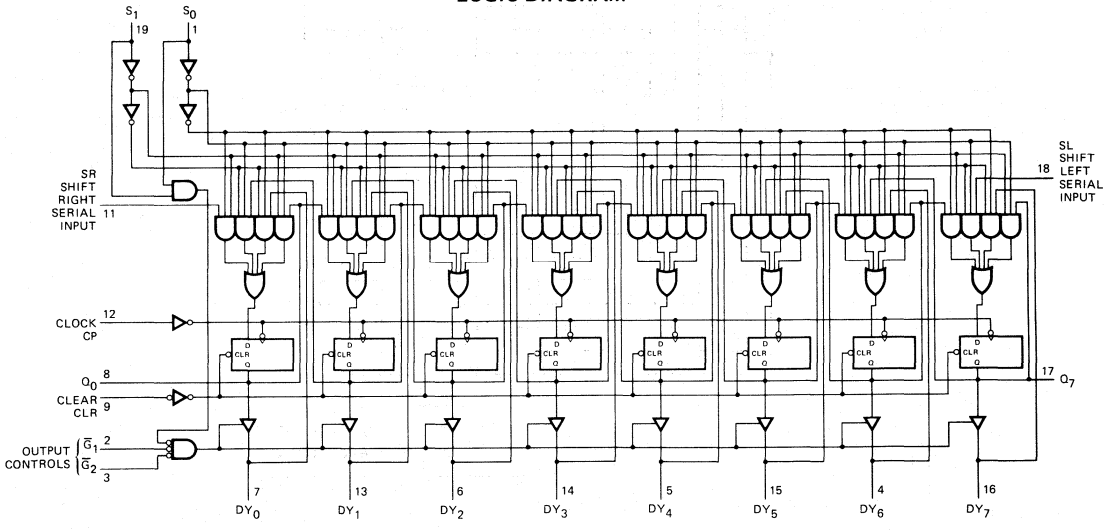
The Am25LS299 and Am54LS/74LS299 are eight-bit universal shift/storage registers with three-state outputs. Four modes of operation are possible: hold (store), shift left, shift right, and load data.

Parallel load inputs and register outputs are multiplexed to reduce the total number of package pins. Separate continuous outputs are also provided for flip-flop A and H. These devices can be cascaded to N-bit words easily.

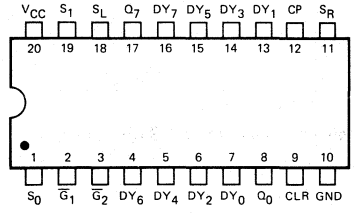
A separate active low asynchronous clear input is used to reset the register. Whenever the clear input is LOW, all internal flip-flops are set LOW independent of all other inputs. See the Am25LS23 for the identical logic function to the Am25LS299 and Am54LS/74LS299, but with synchronous clear capability.

Note: The Advanced Micro Devices' LS299 products were designed prior to publication of data sheets by T.I. Review specifications for possible differences.

LOGIC DIAGRAM

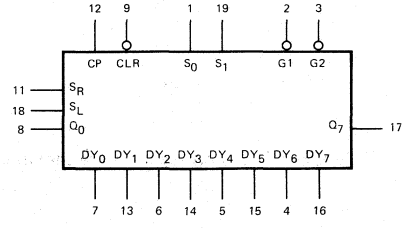


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Am25LS299

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)				Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q_0, Q_7	I_{OH} = −440μA	MIL	2.5			Volts
					COM'L	2.7			
			DY_0–DY_7	MIL, $I_{OH} = -1.0mA$		2.4			
				COM'L, $I_{OH} = -2.6mA$		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}			$I_{OL} = 4.0mA$		0.25	0.4	Volts
					$I_{OL} = 8.0mA$		0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$			S_0, S_1			−0.8	mA
					All Others			−0.4	
I_{IH}	Input HIGH Current (Except DY_i)	V_{CC} = MAX., $V_{IN} = 2.7V$			S_0, S_1			40	μA
					All Others			20	
I_I	Input HIGH Current (Except DY_i)	V_{CC} = MAX.,	$V_{IN} = 7.0V$	S_0, S_1				0.2	mA
				$\overline{G}_1, \overline{G}_2$, CLR, CP				0.1	
			$V_{IN} = 5.5V$	All Others				0.1	
I_{OZ}	Off-State (High-Impedance) Output Current at DY_i	V_{CC} = MAX.			$V_O = 0.4V$			−100	μA
					$V_O = 2.4V$			40	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.				−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.					38	60	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} measured with clock input HIGH and output controls HIGH.

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage ($\overline{G}_1, \overline{G}_2$, CLR, CP, S_0, S_1)	−0.5V to +7.0V
DC Input Voltage (Others)	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

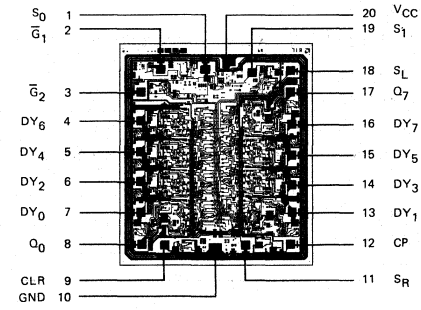
Parameters	Description	Test Conditions (Note 1)				Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q_0, Q_7	I_{OH} = −400μA	MIL	2.5			Volts
					COM'L	2.7			
			DY_0-DY_7	MIL, I_{OH} = −1.0mA		2.4			
				COM'L, I_{OH} = −2.6mA		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}		I_{OL} = 4.0mA			0.25	0.4	Volts
				I_{OL} = 8.0mA 74LS only			0.35	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			S_0, S_1			−0.8	mA
					All Others			−0.4	
I_{IH}	Input HIGH Current (Except DY_i)	V_{CC} = MAX., V_{IN} = 2.7 V			S_0, S_1			40	μA
					All Others			20	
I_I	Input HIGH Current (Except DY_i)	V_{CC} = MAX., V_{IN} = 5.5 V			S_0, S_1			0.2	mA
					All Others			0.1	
I_{OZ}	Off-State (High-Impedance) Output Current at DY_i	V_{CC} = MAX.			V_O = 0.4 V			−100	μA
					V_O = 2.4 V			40	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.				−15		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.					35	60	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} measured with clock input HIGH and output controls HIGH.

DEFINITION OF FUNCTIONAL TERMS

S_R	Shift right data input to Q_0
S_L	Shift left data input to Q_7
Clear	Active LOW synchronous input forcing the Q_0 through Q_7 register to see LOW conditions, visable only if outputs are enabled
Clock	A LOW-to-HIGH transition will result in the register changing state to next state as described by mode and input data condition
S_0, S_1	Mode selection control lines used to control input (output during load) conditions
$\overline{G}_1, \overline{G}_2$	Active LOW input to control three-state output in active LOW AND configuration
Q_0, Q_7	The only two direct outputs; used to cascade shift operations
DY_0-DY_7	Input/Output line dependent on mode and output control. Input only with mode select LOAD. Output in all other modes but subject to output select (G_1, G_2).

Metallization and Pad Layout



DIE SIZE 0.096" X 0.112"

SWITCHING CHARACTERISTICS

T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i		18	26			30	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			22	28			34		
t_{PLH}	Clock to DY_i		18	26			30	ns	
t_{PHL}			22	28			34		
t_{PHL}	Clear to DY_0 - DY_7		25	35			35	ns	
t_{PHL}	Clear to Q_0 or Q_7		25	35			35	ns	
t_{pw}	Pulse Width (Clock)	15			20			ns	
t_s	S_1, S_0 Set-up Time	12			15			ns	
t_s	DY_i or S_R, S_L Data Set-up Time	12			15			ns	
t_h	Hold Time	3.0			3.0			ns	
t_{ZH}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i		20	30			40	ns	
t_{ZL}			20	30			40		
t_{LZ}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i		22	33			40	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			15	23			30		
f_{max}	Maximum Clock Frequency (Note 1)	30	45		25			MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i		38		44	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			41		47		
t_{PLH}	Clock to DY_i		38		44	ns	
t_{PHL}			41		47		
t_{PHL}	Clear to DY_0 - DY_7		50		57	ns	
t_{PHL}	Clear to Q_0 - Q_7		50		57	ns	
t_{pw}	Pulse Width (Clock)	24		27		ns	
t_s	S_1, S_0 Set-up Time	20		23		ns	
t_s	DY_i or S_R, S_L Data Set-up Time	20		23		ns	
t_h	Hold Time	8		9		ns	
t_{ZH}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i		43		50	ns	
t_{ZL}			43		50		
t_{LZ}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i		43		50	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			34		39		
f_{max}	Maximum Clock Frequency (Note 1)	23		20		MHz	

AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

TRUTH TABLE

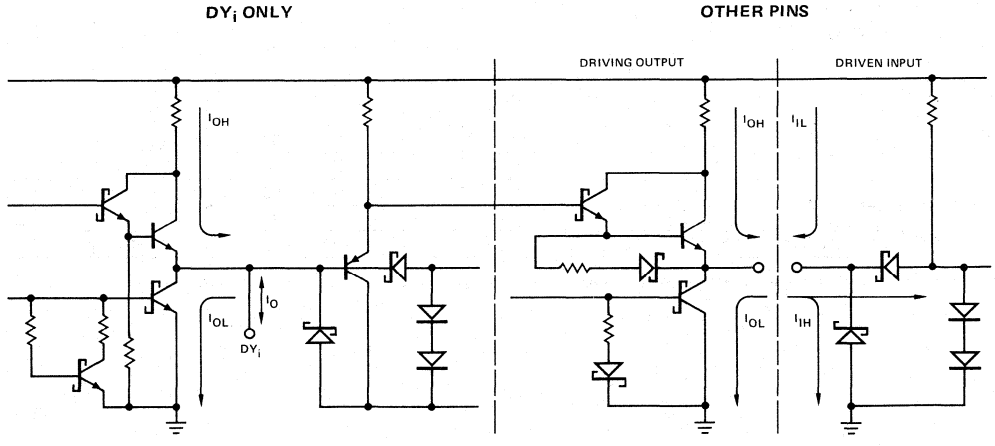
FUNCTION		INPUTS								OUTPUTS		INPUTS/OUTPUTS							
		S_R	S_L	CLEAR	CLOCK	S_0	S_1	$\overline{G}_1$	$\overline{G}_2$	Q_0	Q_7	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7
Clear		X	X	L	X	(Note 1)		L	L	L	L	L	L	L	L	L	L	L	L
Output Control		X	X	X	X	X	X	H	L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	L	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	H	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
	Hold	X	X	H	X	L	L	L	L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
M	Load (Note 2)	X	X	H	↑	H	H	X	X	A	H	A	B	C	D	E	F	G	H
O	Shift Right	L	X	H	↑	H	L	L	L	L	DY_6	L	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
D	Shift Right	H	X	H	↑	H	L	L	L	H	DY_6	H	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
E	Shift Left	X	L	H	↑	L	H	L	L	DY_1	L	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	L
	Shift Left	X	H	H	↑	L	H	L	L	DY_1	H	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	H

L = LOW Z = High Impedance ↑ = Transition LOW-to-HIGH
H = HIGH X = Don't Care NC = No Change

Notes: 1. Either LOW to observe outputs.
2. In this mode DY_i are inputs.

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Am25LS • Am54LS/74LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS

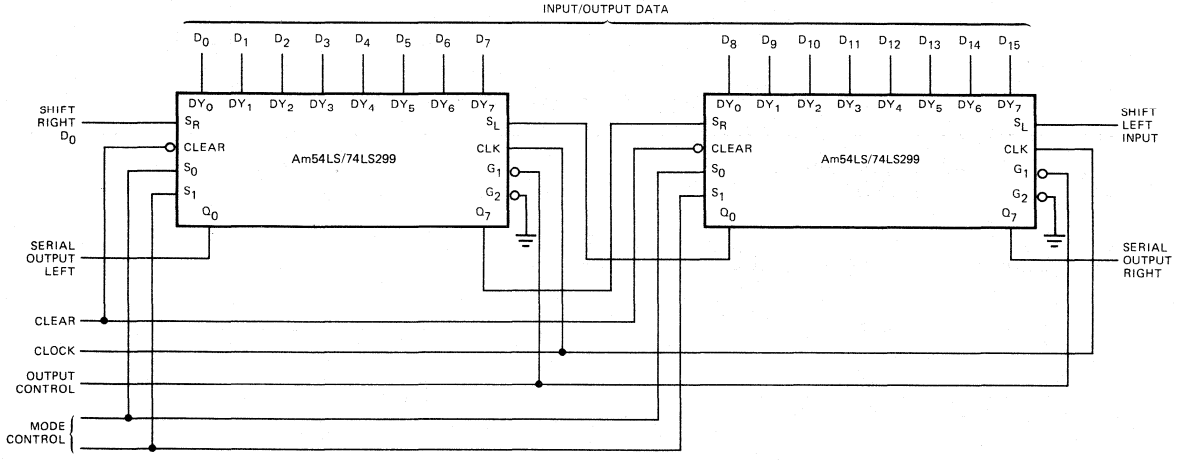


Note: Actual current flow direction shown.

ORDERING INFORMATION

Package Type	Temperature Range	Am25LS299 Order Number	Am54LS/ 74LS299 Order Number
Molded DIP	0°C to +75°C	AM25LS299PC	SN74LS299N
Hermetic DIP	0°C to +75°C	AM25LS299DC	SN74LS299J
Dice	0°C to +75°C	AM25LS299XC	SN74LS299X
Hermetic DIP	−55°C to +125°C	AM25LS299DM	SN54LS299J
Hermetic Flat Pak	−55°C to +125°C	AM25LS299FM	SN54LS299W
Dice	−55°C to +125°C	AM25LS299XM	SN54LS299X

APPLICATION



16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register.

Am25LS373 • Am54LS/74LS373
Am25LS533 • Am54LS/74LS533

Octal Latches with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

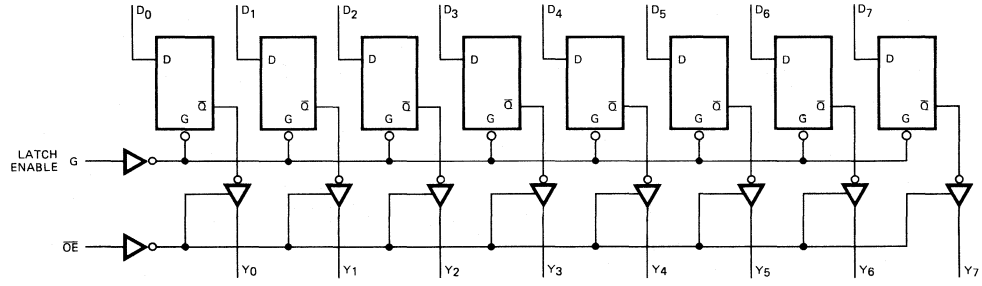
- 8 latches in a single package
- Non-inverting 'LS373, inverting 'LS533
- Three-state outputs interface directly with bus organized systems
- Hysteresis on latch enable input for improved noise margin
- Am25LS devices offer the following improvements over Am54LS/74LS
  - Higher speed
  - Twice the fan-out over military range
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am25LS/54LS/74LS373 and Am25LS/54LS/74LS533 are octal latches with three-state outputs for bus organized system applications. The latches appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

The 'LS373 presents non-inverted data at the outputs while the 'LS533 is inverting.

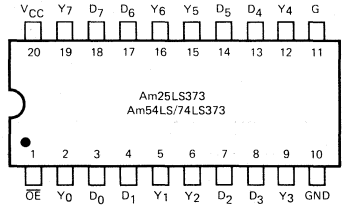
LOGIC DIAGRAM
Am25LS/54LS/74LS373

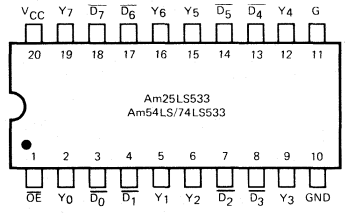


Inputs D_0 through D_7 are inverted on the Am25LS/54LS/74LS533.

BLI-041

CONNECTION DIAGRAMS
Top Views

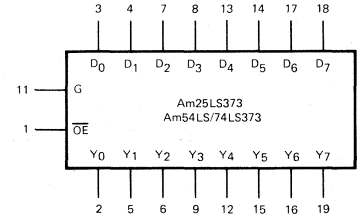




Note: Pin 1 is marked for orientation.

BLI-042

LOGIC SYMBOL



BLI-043

V_{CC} = Pin 20
GND = Pin 10

Inputs D_0 through D_7 are inverted on the Am25LS/54LS/74LS533.

Am25LS373, Am25LS533

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -1.0mA$	MIL	2.4	3.4		Volts
			$I_{OH} = -2.6mA$	COM'L	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 12mA$				0.4	Volts
			$I_{OL} = 24mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				24	40	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS373, Am54LS/74LS533

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -1.0$ mA	MIL	2.4	3.4		Volts
			$I_{OH} = -2.6$mA	COM'L	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	All, I_{OL} = 12mA			0.25	0.4	Volts
			74LS only, I_{OL} = 24mA			0.35	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18$mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0 V					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	V_O = 0.4 V				−20	μA
			V_O = 2.4 V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−130	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				24	40	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

FUNCTION TABLES

Am25LS/54LS/74LS373

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	D_i	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	L	Transparent
L	H	H	L	H	
L	L	X	NC	NC	Latched

Am25LS/54LS/74LS533

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	$\overline{D_i}$	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	H	Transparent
L	H	H	L	L	
L	L	X	NC	NC	Latched

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

Am25LS/54LS/74LS373

D_i The latch data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i The three-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

Am25LS/54LS/74LS533

$\overline{D_i}$ The latch inverting data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i The three-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the inverted outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

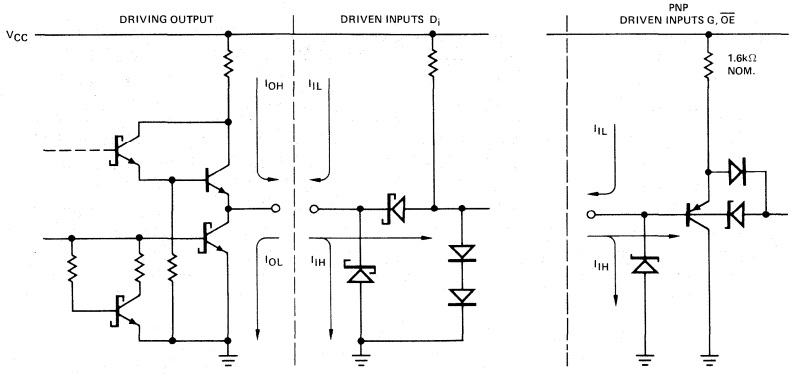
Am25LS/54LS/74LS373
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	Enable to Output		20	30		20	30	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}			18	30		18	30		
t_{PLH}	Data Input to Output		10	18		12	18	ns	
t_{PHL}			12	18		12	18		
t_s(H)	HIGH Data to Enable	0			0			ns	
t_s(L)	LOW Data to Enable	0			0				
t_h(H)	HIGH Data to Enable	10			10			ns	
t_h(L)	LOW Data to Enable	10			10				
t_{pw}	Enable Pulse Width	15			15			ns	
t_{ZH}	$\overline{OE}$ to Y_i			28			28	ns	
t_{ZL}				36			36		
t_{HZ}	$\overline{OE}$ to Y_i			20			20	ns	C_L = 5pF, R_L = 667Ω
t_{LZ}				25			25		

Am25LS373 ONLY
SWITCHING CHARACTERISTICS
OVER OPERATING RANGE

Parameters	Description	Am25LS COM'L Min. (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)	Am25LS COM'L Max.	Am25LS MIL Min. (T_A = −55°C to +125°C, V_{CC} = 5.0V ±10%)	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Enable to Output		35		40	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}			35		40		
t_{PLH}	Data Input to Output		19		20	ns	
t_{PHL}			20		25		
t_s(H)	HIGH Data to Enable	0		0		ns	
t_s(L)	LOW Data to Enable	0		0			
t_h(H)	HIGH Data to Enable	11		12		ns	
t_h(L)	LOW Data to Enable	15		17			
t_{pw}	Enable Pulse Width	17		20		ns	
t_{ZH}	$\overline{OE}$ to Y_i		28		28	ns	
t_{ZL}			36		36		
t_{HZ}	$\overline{OE}$ to Y_i		33		36	ns	C_L = 5pF, R_L = 667Ω
t_{LZ}			33		36		

Am25LS • Am54LS/74LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI-044

Am25LS/54LS/74LS533
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25LS/54LS/74LS Min	Typ	Max	Units	Test Conditions
t_{PLH}	Enable to Output		20	30	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}			18	30		
t_{PLH}	Data Input to Output		13	20	ns	
t_{PHL}			15	23		
$t_s(H)$	HIGH Data to Enable	3			ns	
$t_s(L)$	LOW Data to Enable	0				
$t_h(H)$	HIGH Data to Enable	13			ns	
$t_h(L)$	LOW Data to Enable	7				
t_{pw}	Enable Pulse Width	15			ns	
t_{ZH}	$\overline{OE}$ to Y_i			28	ns	
t_{ZL}				36		
t_{HZ}	$\overline{OE}$ to Y_i			20	ns	C_L = 5pF, R_L = 667Ω
t_{LZ}				25		

Am25LS533 ONLY
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

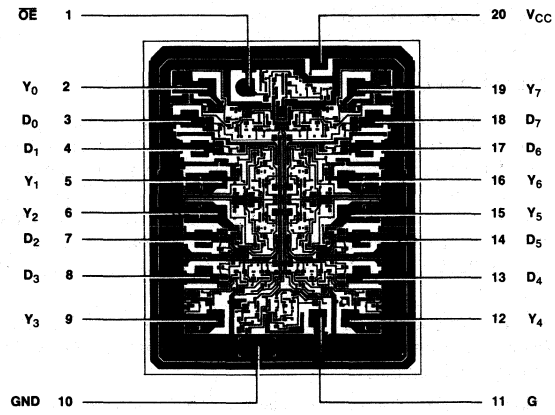
Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	Enable to Output		35		40	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}			35		40		
t_{PLH}	Data Input to Output		20		21	ns	
t_{PHL}			25		30		
$t_s(H)$	HIGH Data to Enable	5		5		ns	
$t_s(L)$	LOW Data to Enable	0		0			
$t_h(H)$	HIGH Data to Enable	14		15		ns	
$t_h(L)$	LOW Data to Enable	9		10			
t_{pw}	Enable Pulse Width	17		20		ns	
t_{ZH}	$\overline{OE}$ to Y_i		28		28	ns	
t_{ZL}			36		36		
t_{HZ}	$\overline{OE}$ to Y_i		33		36	ns	C_L = 5pF, R_L = 667Ω
t_{LZ}			33		36		

ORDERING INFORMATION

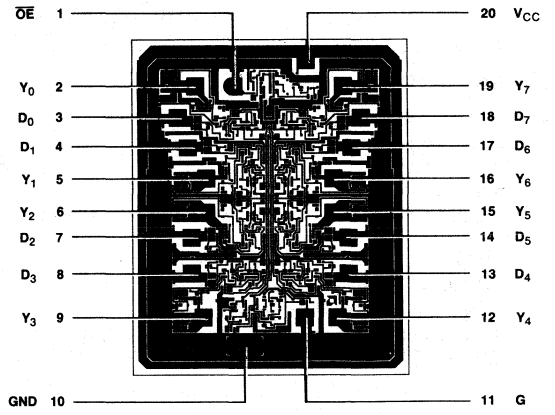
Package Type	Temperature Range	Am25LS373 Order Number	Am54LS/74LS373 Order Number	Am25LS533 Order Number	Am54LS/74LS533 Order Number
Molded DIP	0°C to +70°C	AM25LS373PC	SN74LS373N	AM25LS533PC	SN74LS533N
Hermetic DIP	0°C to +70°C	AM25LS373DC	SN74LS373J	AM25LS533DC	SN74LS533J
Dice	0°C to +70°C	AM25LS373XC	SN74LS373X	AM25LS533XC	SN74LS533X
Hermetic DIP	−55°C to +125°C	AM25LS373DM	SN54LS373J	AM25LS533DM	SN54LS533J
Hermetic Flat Pak	−55°C to +125°C	AM25LS373FM	SN54LS373W	AM25LS533FM	SN54LS533W
Dice	−55°C to +125°C	AM25LS373XM	SN54LS373X	AM25LS533XM	SN54LS533X

Metallization and Pad Layouts

Am25LS/54LS/74LS373

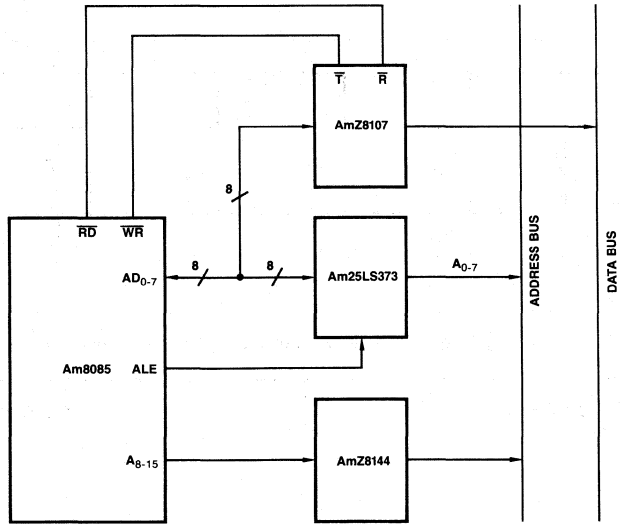


Am25LS/54LS/74LS533



DIE SIZE 0.073" X 0.089"

APPLICATION



BLI-056

Am25LS374A • Am54LS/74LS374A
Am25LS534 • Am54LS/74LS534

8-Bit Registers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 8-bit, high-speed parallel registers
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- Am25LS/54LS have I_{OL} = 24mA over full military temperature range
- Am25LS devices offer the following improvements over Am54/74LS
  - Twice the fan-out over military range
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

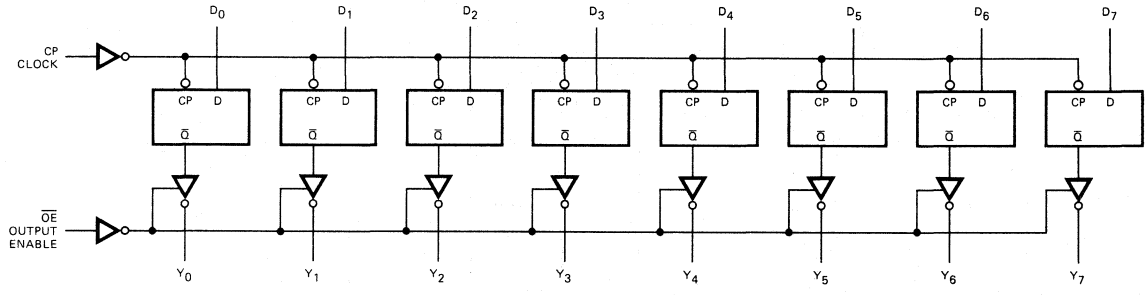
The Am25LS374A and Am54LS/74LS374A are 8-bit registers built using advanced Low-Power Schottky technology. These registers consist of eight D-type flip-flops with a buffered common clock and a buffered three-state output control. When the output enable (OE) input is LOW, the eight outputs are enabled. When the OE input is HIGH, the outputs are in the three-state condition. The Am25LS/54LS/74LS534 provide the inverting version of the same function.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y ouputs on the LOW-to-HIGH transition of the clock input.

The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

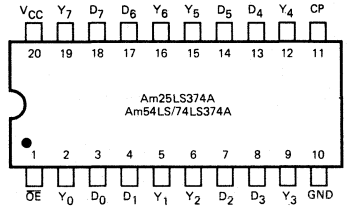
LOGIC DIAGRAM

Am25LS/54LS/74LS374A



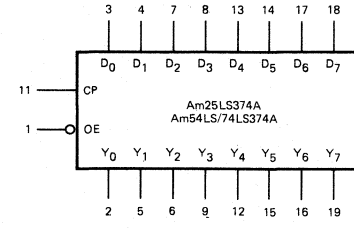
Ouputs Y_0 through Y_7 are inverted on the Am25LS/54LS/74LS534

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
Ouputs Y_0 through Y_7 are inverted on the Am25LS/54LS/74LS534

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10
Outputs Y_0 through Y_7 are inverted on the Am25LS/54LS/74LS534

Am25LS374A/534

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -1.0mA$, MIL		2.4	3.4		Volts
			$I_{OH} = -2.6mA$, COM'L		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 12mA$				0.4	Volts
			$I_{OL} = 24mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.7V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				27	40	mA

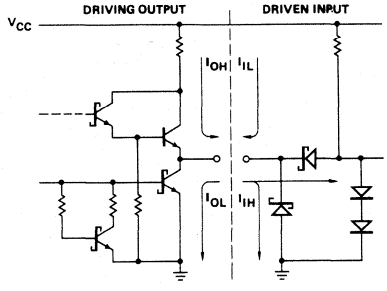
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open; all D_i inputs and $\overline{OE} = 4.5V$. Apply momentary ground, then 4.5V to clock input.

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am25LS • Am54LS/74LS
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am54LS/74LS374A/LS534

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -1.0mA$	MIL	2.4	3.4		Volts
			$I_{OH} = -2.6mA$	COM'L	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	All, $I_{OL} = 12mA$				0.4	Volts
			74LS only, $I_{OL} = 24mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.5V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−130	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				27	40	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open; all D_i inputs and $\overline{OE} = 4.5V$. Apply momentary ground, then 4.5V to clock input.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Y_i The register three-state outputs.

$\overline{OE}$ Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

FUNCTION TABLE

FUNCTION	INPUTS			INTERNAL	OUTPUTS
	$\overline{OE}$	Clock	D_i	Q_i	Y_i
Hi-Z	H	L	X	NC	Z
	H	H	X	NC	Z
LOAD REGISTER	L	↑	L	L	L
	L	↑	H	H	H
	H	↑	L	L	Z
	H	↑	H	H	Z

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance
↑ = LOW-to-HIGH transition

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Am25LS Min	Am25LS Typ	Am25LS Max	Am54LS/74LS Min	Am54LS/74LS Typ	Am54LS/74LS Max	Units	Test Conditions
t_{PLH}	Clock to Y_i				28			28	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}					28			28		
t_{PW}	Clock Pulse Width	LOW	15			15			ns	
		HIGH	15			15				
t_s	Data		20			20			ns	
t_h	Data		0			0			ns	
t_{ZH}	$\overline{OE}$ to Y_i				20			20	ns	
t_{ZL}					20			20		
t_{HZ}	$\overline{OE}$ to Y_i (Note 2)				20			20	ns	C_L = 5.0pF, R_L = 667Ω
t_{LZ}					25			25		
f_{max}	Maximum Clock Frequency (Note 1)		35	50		35	50		MHz	

Notes: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

2. Because of interlead capacitance the rising edge of $\overline{OE}$ is coupled Y_o, thereby, increasing the apparent t_{HZ} for Y_o by 5ns for plastic package device and 10ns for Cerdip. The die geometry for Y_o is the same as other outputs and no spec difference is required for users of dice.

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Am25LS COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Min	Am25LS COM'L Max	Am25LS MIL T_C = −55 to +125°C, V_{CC} = 5.0V ±10% Min	Am25LS MIL Max	Units	Test Conditions
t_{PLH}	Clock to Y_i			30		38	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}				30		38		
t_{PW}	Clock Pulse Width	LOW	10		10		ns	
		HIGH	19		28			
t_s	Data		20		20		ns	
t_h	Data		0		0		ns	
t_{ZH}	$\overline{OE}$ to Y_i			25		30	ns	
t_{ZL}				25		30		
t_{HZ}	$\overline{OE}$ to Y_i (Note 2)			25		30	ns	C_L = 5.0pF, R_L = 667Ω
t_{LZ}				25		28		
f_{max}	Maximum Clock Frequency (Note 1)		35		30		MHz	

*AC performance over the operating temperatuare range is guaranteed by testing defined in Group A, Subgroup 9.

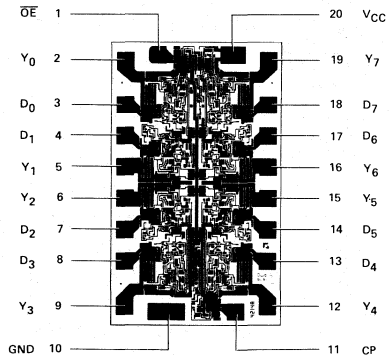
Note 2. Because of interlead capacitance the rising edge of $\overline{OE}$ is coupled into Y_o, thereby, increasing the apparent t_{HZ} for Y_o by 5ns for plastic package device and 10ns for cerdip. The die geometry for Y_o is the same as other outputs and no spec difference is required for users of dice.

ORDERING INFORMATION

Package Type	Temperature Range	Am25LS374A Order Number	Am54LS/74LS374A Order Number	Am25LS534 Order Number	Am54LS/74LS534 Order Number
Molded DIP	0 to +70°C	AM25LS374APC	SN74LS374AN	AM25LS534PC	SN74LS534N
Hermetic DIP	0 to +70°C	AM25LS374ADC	SN74LS374AJ	AM25LS534DC	SN74LS534J
Dice	0 to +70°C	AM25LS374AXC	SN74LS374AX	AM25LS534XC	SN74LS534X
Hermetic DIP	−55°C to +125°C	AM25LS374ADM	SN54LS374AJ	AM25LS534DM	SN54LS534J
Hermetic Flat Pak	−55°C to +125°C	AM25LS374AFM	SN54LS374AW	AM25LS534FM	SN54LS534W
Dice	−55°C to +125°C	AM25LS374AXM	SN54LS374AX	AM25LS534XM	SN54LS534X

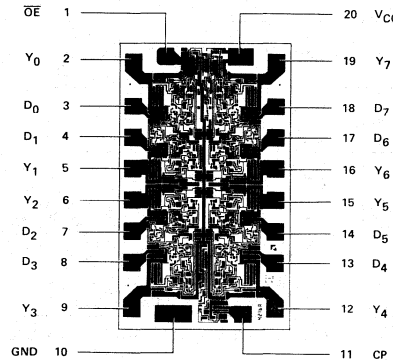
METALLIZATION AND PAD LAYOUTS

Am25LS/54LS/74LS374A



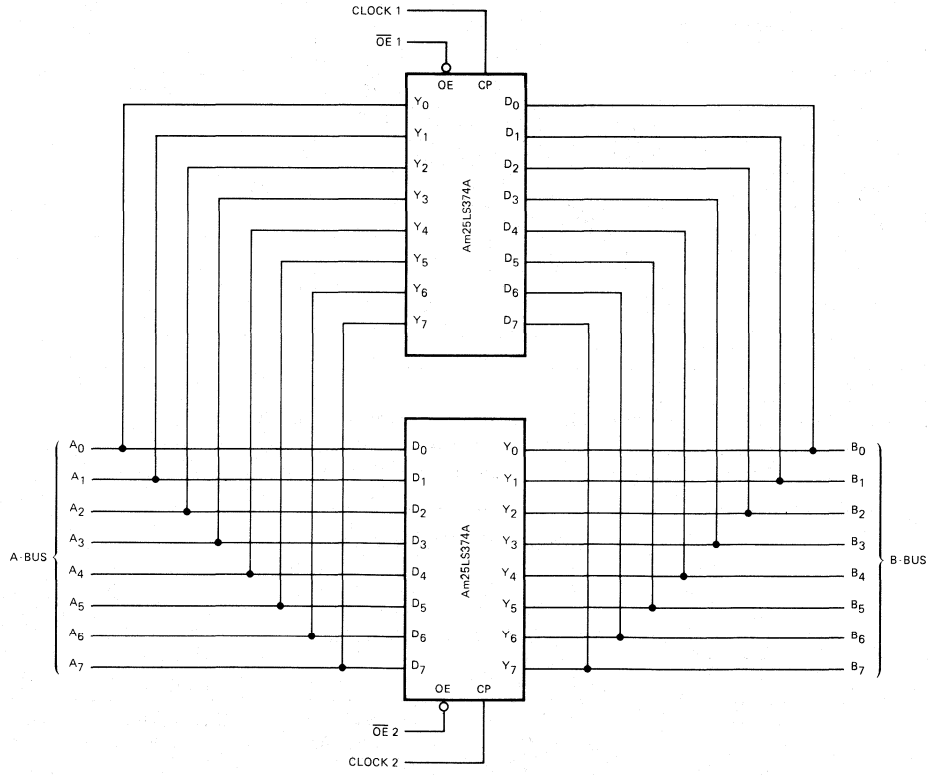
DIE SIZE 0.077" X 0.047"

Am25LS/54LS/74LS534



DIE SIZE 0.077" X 0.047"

APPLICATIONS



Two Am25LS374s can be used as a bidirectional bus driver/register. The above connetion shows separate clocks and three-state controls.

Am25LS377 • Am25LS377B
Am54LS/74LS377

8-Bit Register with Register Enable
8-Bit Register with Register Enable and Buffered Outputs

2

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high speed parallel registers
- Clock to output delay – 14ns (typ) on Am25LS377
- Buffered outputs to eliminate output commutation on Am25LS377B
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common clock enable
- Am25LS devices offer the following improvements over Am54/74LS
  - 50mV lower V_{OL} at I_{OL} = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am25LS377, Am25LS377B and the Am54LS/74LS377 are eight-bit registers built using advanced Low-Power Schottky technology. These registers consist of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

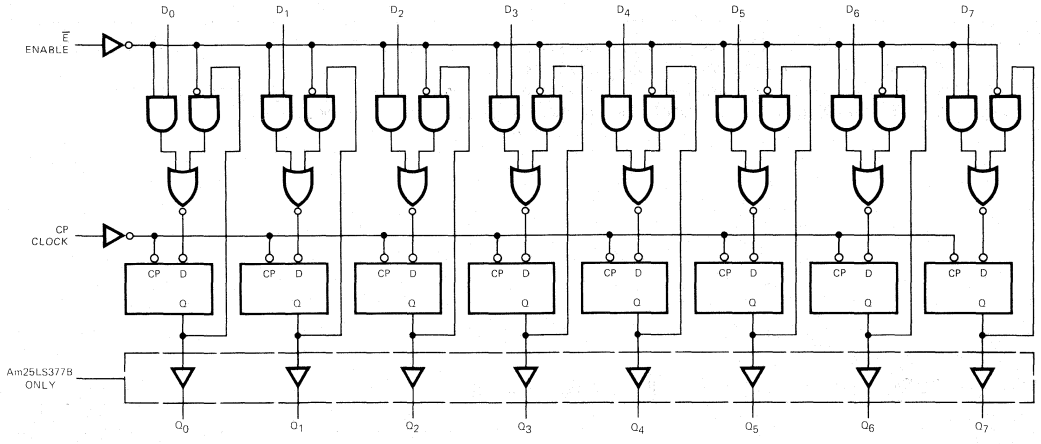
When the clock enable ($\overline{E}$) input is LOW, new data is entered into the flip-flop register on the LOW-to-HIGH transition of the clock input. When the ($\overline{E}$) input is HIGH, the register will retain the present data independent of the clock inputs.

The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

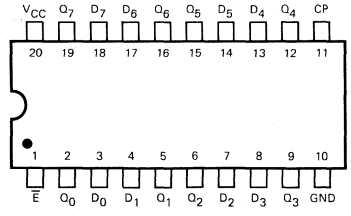
The Am25LS377and Am54LS/74LS377 are designed for maximum speed.

The Am25LS377B has an additional output buffer to eliminate output commutation.

LOGIC DIAGRAM

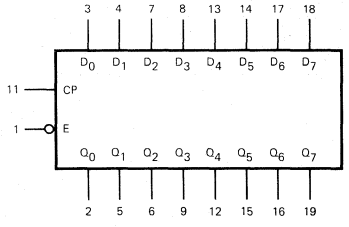


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Am25LS377 • Am25LS377B
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440μA $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5			Volts
				COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V					0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−20		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				17	28	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, E = GND, all Di inputs = GND. Apply momentary ground, then 4.5V to clock input.

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS377
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5			Volts
			COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	All, I_{OL} = 4mA			0.4	Volts
			74LS only, I_{OL} = 8mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0 V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−20		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			17	28	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, E = GND, all Di inputs = GND. Apply momentary ground, then 4.5V to clock input.

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{E}$	D_i	CP	Q_i
H	X	X	NC
L	X	H	NC
L	X	L	NC
L	L	↑	L
L	H	↑	H

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
NC = No Change
X = Don't Care

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{E}$ Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Q_i The TRUE register outputs.

Am25LS377 • Am54LS/74LS377 SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	Clock to Output			13	20		17	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				14	21		18	27		
t_{pw}	Clock Pulse Width	HIGH	15			20			ns	
		LOW	15			20				
t_s	Data		20			20			ns	
t_h	Data		0			5			ns	
t_s	Clock Enable	Active State	15			25			ns	
		Inactive State	10			10				
t_h	Clock Enable		5			5			ns	
f_{max}	Maximum Clock Frequency (Note 1)		30	40		30	40		MHz	

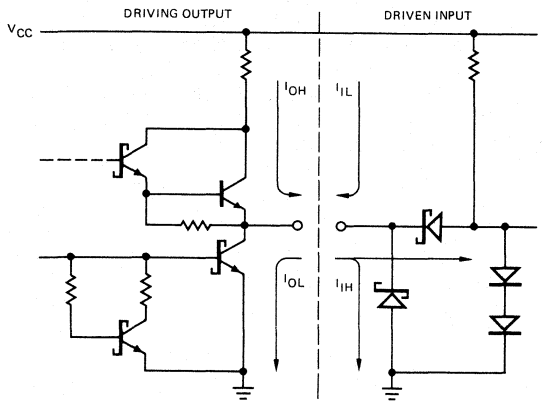
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS377 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output			25		27	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				29		34		
t_{pw}	Clock Pulse Width	HIGH	15		15		ns	
		LOW	15		15			
t_s	Data		24		26		ns	
t_h	Data		0		0		ns	
t_s	Clock Enable	Active	18		20		ns	
		Inactive	13		15			
t_h	Clock Enable		5		5		ns	
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

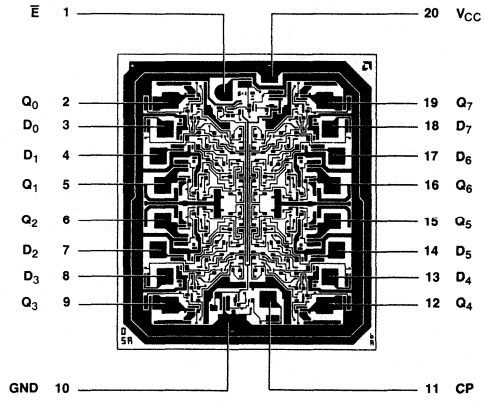
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Metallization and Pad Layout Am25LS/54LS/74LS377



DIE SIZE..072" X .083"

Am25LS377B SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Am25LS Min.	Am25LS Typ.	Am25LS Max.	Units	Test Conditions
t_{PLH}	Clock to Output			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				23	35		
t_{pw}	Clock Pluse Width	HIGH	20			ns	
		LOW	25				
t_s	Data		20			ns	
t_h	Data		10			ns	
t_s	Clock Enable	Active State	25			ns	
		Inactive State	20				
t_h	Clock Enable		5			ns	
f_{max}	Maximum Clock Frequency (Note 1)		30	40		MHz	

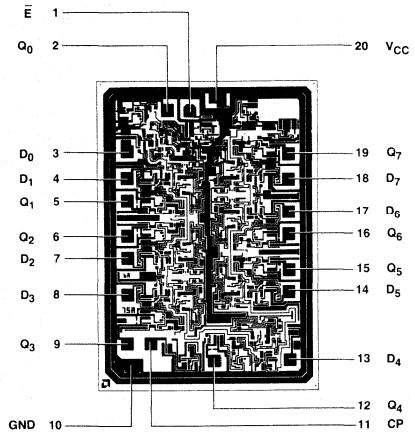
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS377B SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output			32		37	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				45		54		
t_{pw}	Clock Pulse Width	HIGH	25		25		ns	
		LOW	25		30			
t_s	Data		20		20		ns	
t_h	Data		12		15		ns	
t_s	Clock Enable	Active	27		30		ns	
		Inactive	22		25			
t_h	Clock Enable		5		5		ns	
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Metallization and Pad Layout Am25LS377B

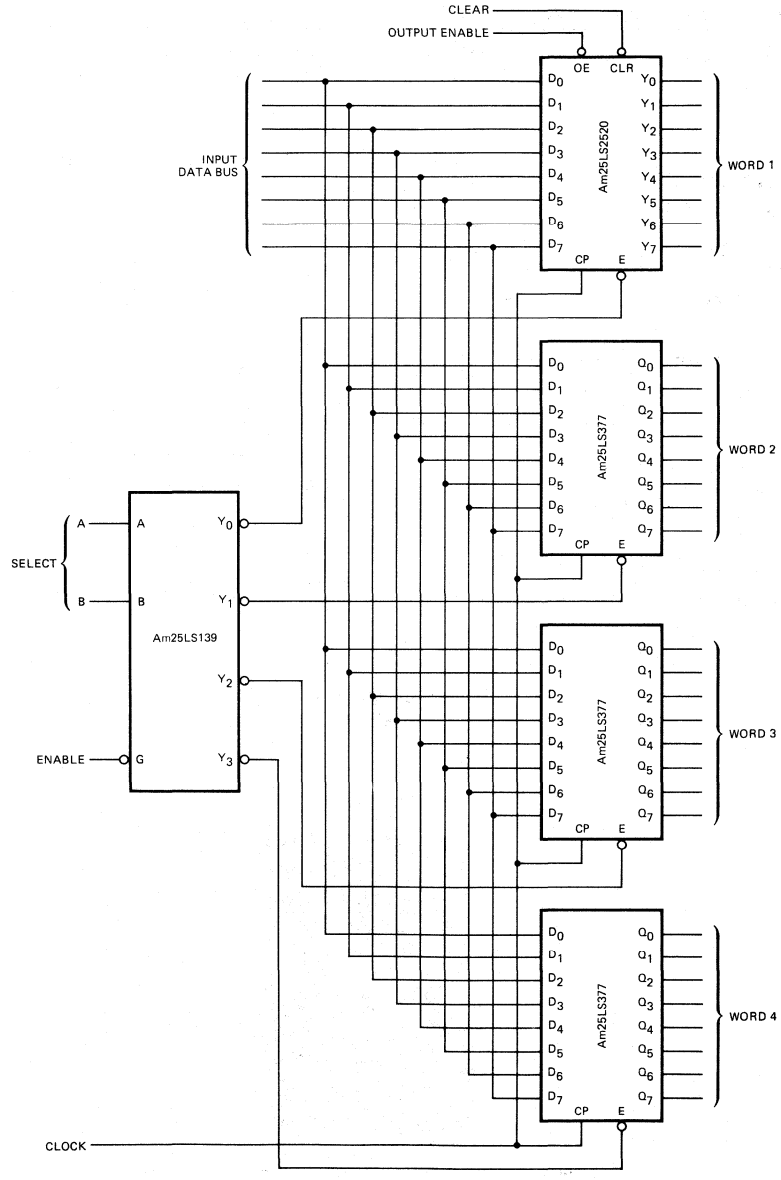


DIE SIZE 0.080" X 0.111"

ORDERING INFORMATION

Package Type	Temperature Range	Am25LS377 Order Number	Am25LS377B Order Number	Am54LS/ 74LS377 Order Number
Molded DIP	0°C to 70°C	Am25LS377PC	Am25LS377BPC	SN74LS377N
Hermetic DIP	0°C to 70°C	Am25LS377DC	Am25LS377BDC	SN74LS377J
Dice	0°C to 70°C	Am25LS377XC	Am25LS377BXC	SN74LS377X
Hermetic DIP	−55°C to +125°C	Am25LS377DM	Am25LS377BDM	SN54LS377J
Hermetic Flat Pak	−55°C to +125°C	Am25LS377FM	Am25LS377BFM	SN54LS377W
Dice	−55°C to +125°C	Am25LS377XM	Am25LS377BXM	SN54LS377X

APPLICATION



Selective Register Loading of Data on Synchronous Clock.

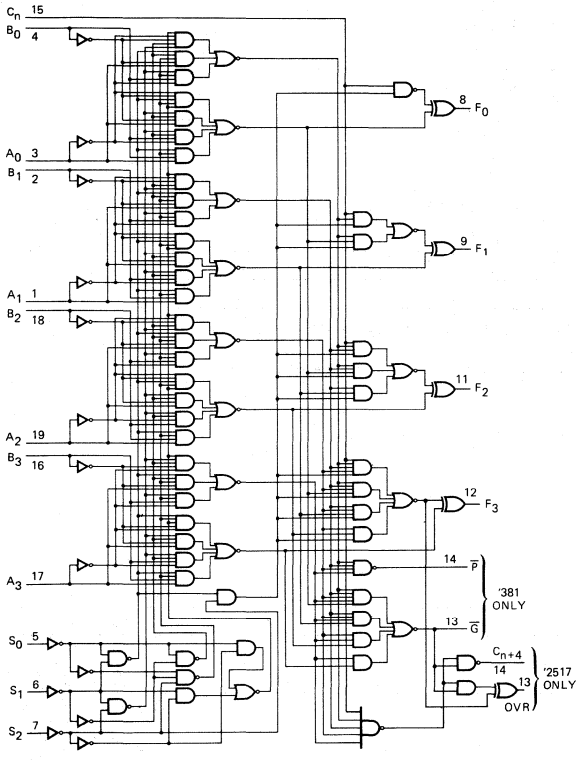
Am25LS381 • Am54LS/74LS381
Am25LS2517

Arithmetic Logic Unit/Function Generator

DISTINCTIVE CHARACTERISTICS

- Three arithmetic functions
- Three logic functions
- Preset and clear functions
- Space-saving 20-pin package
- Carry output (C_{n+4}) and overflow (OVR) outputs on Am25LS2517
- Generate and propagate outputs for full lookahead carry on Am25LS381
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL} at I_{OL} = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance testing to MIL-STD-883 requirements

LOGIC DIAGRAM



Note: The Advanced Micro Devices' LS381 products were designed prior to publication of data sheets by T.I. Review specifications for possible differences. Am25LS2517 has been second sourced as the 54/74LS382.

FUNCTIONAL DESCRIPTION

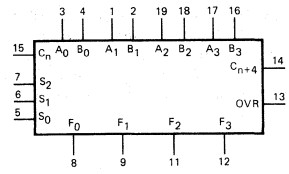
The Am25LS381 and Am54LS/74LS381 are arithmetic logic units (ALU)/function generators that perform three arithmetic operations and three logic operations on two 4-bit words. The device can also output forced 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs S_0, S_1 and S_2 as shown in the function table. Full carry look ahead is used over the four-bit field within the device. When devices are cascaded, multi-level full carry look-ahead is implemented using a '182 carry look ahead generator and the $\overline{G}$ and $\overline{P}$ outputs on the Am25LS381 or Am54LS/74LS381. The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package. If the C_{n+4} carry output function is required, the Am25LS2517 should be used.

The Am25LS381 is a high-performance version of the Am54LS/74LS381. Improvements include faster a. c. specifications, higher noise margin and twice the fan-out over the military temperature range.

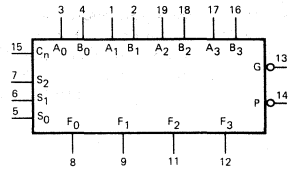
The Am25LS2517 is an arithmetic logic unit (ALU)/function generator that performs three arithmetic operations and three logic operations on two 4-bit words. The device can also force output 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs S_0, S_1 and S_2 as shown in the function table. Full carry look-ahead is used over the four-bit field within the device. When devices are cascaded, the carry output (C_{n+4}) is connected to the carry input (C_n) of the next device. The Am25LS2517 can also detect two's complement overflow. The overflow output (OVR) is defined logically as $C_{n+3} \oplus C_{n+4}$.

LOGIC SYMBOLS

Am25LS2517



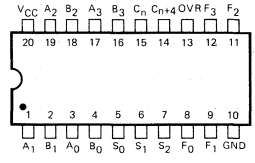
Am25LS381
Am54LS/74LS381



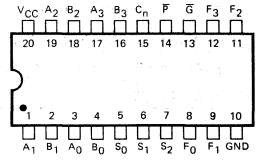
V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAMS
Top Views

Am25LS2517



Am25LS381
Am54LS/74LS381



Note: Pin 1 is marked for orientation.

Am25LS381•Am25LS2517

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$\overline{G}$, $I_{OL} = 16mA$				0.55	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	Any S				−0.36	mA
			Any A or B				−1.44	
			'LS381, C_n				−1.08	
			'LS2517, C_n				−1.44	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	Any S				20	μA
			Any A or B				80	
			'LS381, C_n				60	
			'LS2517, C_n				80	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$	Any S				0.1	mA
			Any A or B				0.4	
			'LS381, C_n				0.3	
		V_{CC} = MAX., $V_{IN} = 5.5V$	'LS2517, C_n				0.4	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.	MIL	Am25LS381			40	mA
				Am25LS2517			43	
			COM'L	Am25LS381		25	43	
				Am25LS2517		27	47	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: LS381: $S_0 = S_1 = S_2$ = GND, all other inputs open.
LS2517: $S_0 = C_n$ = open, all other inputs = GND.

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage (Except Am25LS2517, C_n input = 5.5V)	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

.m54LS/74LS381

LECTRICAL CHARACTERISTICS

he Following Conditions Apply Unless Otherwise Specified:

OM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

IIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

)C CHARACTERISTICS OVER OPERATING RANGE

arameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA			0.4	Volts
			74LS only, I_{OL} = 8mA			0.5	
			$\overline{P}$, I_{OL} = 8.0mA			0.5	
			$\overline{G}$, I_{OL} = 16mA			0.65	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current (Note 5)	V_{CC} = MAX., V_{IN} = 0.4 V	Any S			−0.4	mA
			Others			−1.6	
I_{IH}	Input HIGH Current (Note 5)	V_{CC} = MAX., V_{IN} = 2.7 V	Any S			20	μA
			Others			80	
I_I	Input HIGH Current (Note 5)	V_{CC} = MAX., V_{IN} = 7.0 V	Any S			0.1	mA
			Others			0.4	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			25	43	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: LS381: $S_0 = S_1 = S_2$ = GND, all other inputs open.
LS2517: $S_0 = C_n$ = open, all other inputs = GND.
5. Limits chosen by AMD based on SN54S/74S381, T.I. LS data unavailable.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3	The A data inputs.
B_0, B_1, B_2, B_3	The B data inputs.
S_0, S_1, S_2, S_3	The control inputs used to determine the arithmetic or logic function performed.
F_0, F_1, F_2, F_3	The data outputs of the ALU.
C_n	The carry-in input of the ALU.
C_{n+4}	The carry-look-ahead output of the four-bit input field.
$\overline{G}$	The carry-generate output for use in multi-level look-ahead schemes.
$\overline{P}$	The carry-propagate output for use in multi-level look-ahead schemes.
OVR	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

FUNCTION TABLE

Selection			Arithmetic/Logic Operation
S_2	S_1	S_0	
L	L	L	Clear
L	L	H	B Minus A
L	H	L	A Minus B
L	H	H	A Plus B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	Preset

H = High Level, L = Low Level

See Truth Table for full description.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	C_n to F_i		14	19			26	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			16	23			30		
t_{PLH}	A_i or B_i to F_i		16	24			30	ns	
t_{PHL}			23	35			40		
t_{PLH}	S_i to F_i		20	30			35	ns	
t_{PHL}			25	37			40		
t_{PLH}	A_i or B_i to $\overline{G}$ ('LS381 Only)		20	27			35	ns	
t_{PHL}			15	22			30		
t_{PLH}	A_i or B_i to $\overline{P}$ ('LS381 Only)		17	24			34	ns	
t_{PHL}			15	23			30		
t_{PLH}	S_i to $\overline{G}$ or $\overline{P}$ ('LS381 Only)		32	48			55	ns	
t_{PHL}			23	35			42		
t_{PLH}	A_i or B_i to OVR ('LS2517 Only)		23	34			—	ns	
t_{PHL}			24	36			—		
t_{PLH}	A_i or B_i to C_{n+4} ('LS2517 Only)		21	32			—	ns	
t_{PHL}			24	36			—		
t_{PLH}	S_i to OVR or C_{n+4} ('LS2517 Only)		27	41			—	ns	
t_{PHL}			37	55			—		
t_{PLH}	C_n to C_{n+4} ('LS2517 Only)		14	21			—	ns	
t_{PHL}			15	22			—		
t_{PLH}	C_n to OVR ('LS2517 Only)		15	22			—	ns	
t_{PHL}			15	22			—		

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L (T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5%) Min.	Am25LS COM'L Max.	Am25LS MIL (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%) Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	C_n to F_i		27		30	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			35		42		
t_{PLH}	A_i or B_i to F_i		32		36	ns	
t_{PHL}			44		50		
t_{PLH}	S_i to F_i		38		42	ns	
t_{PHL}			48		55		
t_{PLH}	A_i or B_i to $\overline{G}$ ('LS381 Only)		37		40	ns	
t_{PHL}			31		36		
t_{PLH}	A_i or B_i to $\overline{P}$ ('LS381 Only)		34		39	ns	
t_{PHL}			34		42		
t_{PLH}	S_i to $\overline{G}$ or $\overline{P}$ ('LS381 Only)		57		63	ns	
t_{PHL}			47		55		
t_{PLH}	A_i or B_i to OVR ('LS2517 Only)		41		45	ns	
t_{PHL}			47		55		
t_{PLH}	A_i or B_i to C_{n+4} ('LS2517 Only)		38		40	ns	
t_{PHL}			46		52		
t_{PLH}	S_i to OVR or C_{n+4} ('LS2517 Only)		52		60	ns	
t_{PHL}			66		75		
t_{PLH}	C_n to C_{n+4} ('LS2517 Only)		28		32	ns	
t_{PHL}			28		30		
t_{PLH}	C_n to OVR ('LS2517 Only)		30		35	ns	
t_{PHL}			28		30		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS/54LS/74LS381
TEST TABLE

Path						Same Bit		Other Data Bits		Output
In	Out	S_0	S_1	S_2	C_n	4.5 V	GND	4.5 V	GND	Waveform
C_n	Any F	1	0	0	–	–	–	All A's & B's	–	out-of-phase
C_n	F_i	1	0	0	–	B_i	Ai	All A's & B's	–	in-phase
A_i	$\overline{G}$	1	1	0	X	B_i	–	All B's	All A's	out-of-phase
B_i	$\overline{G}$	1	1	0	X	A_i	–	All B's	All A's	out-of-phase
A_i	$\overline{P}$	X	X	1	X	B_i	–	All A's & B's	–	out-of-phase
B_i	$\overline{P}$	1	1	0	X	A_i	–	All B's	All A's	out-of-phase
A_i	F_i	0	1	0	0	–	B_i	–	A's & B's	out-of-phase
A_i	F_i	0	1	0	1	–	B_i	–	A's & B's	in-phase
B_i	F_i	0	1	0	0	–	A_i	–	A's & B's	out-of-phase
B_i	F_i	0	1	0	1	–	A_i	–	A's & B's	in-phase
A_i	F_{i+1}	0	1	0	1	B_i	–	A's & B's	–	out-of-phase
B_i	F_{i+1}	1	0	0	1	A_i	–	A's & B's	–	out-of-phase
S_0	F_i	–	0	0	1	B_i	A_i	All B's	All A's	in-phase
S_0	$\overline{G}$	–	1	0	X	–	–	A's & B's	–	out-of-phase
S_0	$\overline{P}$	–	1	0	X	–	–	All B's	All A's	out-of-phase
S_1	F_i	0	–	0	1	A_i	B_i	All A's	All B's	in-phase
S_1	$\overline{G}$	1	–	0	X	–	–	A's & B's	–	out-of-phase
S_1	$\overline{P}$	1	–	0	X	–	–	All A's	All B's	out-of-phase
S_2	F_i	0	1	–	1	A_i	B_i	All A's	All B's	in-phase
S_2	$\overline{G}$	1	1	–	X	–	–	A's & B's	–	in-phase
S_2	$\overline{P}$	1	1	–	X	–	–	All A's	All B's	out-of-phase

X = Don't care

TRUTH TABLE

	INPUTS						OUTPUTS					
FUNCTION	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
CLEAR	0	0	0	X	X	X	0	0	0	0	0	0
B MINUS A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A MINUS B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A PLUS B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A ⊕ B	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
PRESET	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

Am25LS2517
TEST TABLE

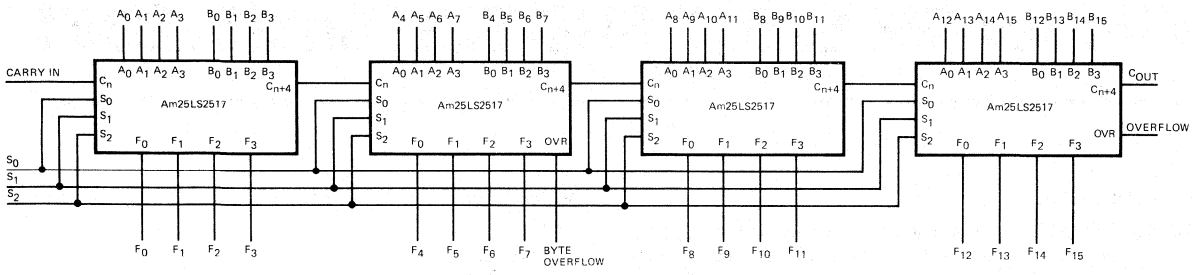
Path						Same Bit		Other Data Bits		Output
In	Out	S_0	S_1	S_2	C_n	4.5 V	GND	4.5 V	GND	Waveform
C_n	Any F	1	0	0	–	–	–	A's & B's	None	out-of-phase
C_n	F_i	1	0	0	–	B_i	A_i	A's & B's	None	in-phase
A_i	F_i	0	1	0	0	–	B_i	None	A's & B's	out-of-phase
A_i	F_i	0	1	0	1	–	B_i	None	A's & B's	in-phase
A_i	OVRF	0	1	1	1	B_i	–	A's & B's	None	in-phase
A_i	C_{n+4}	0	1	1	1	B_i	–	A's & B's	None	in-phase
B_i	F_i	0	1	0	0	–	A_i	None	A's & B's	out-of-phase
B_i	F_i	0	1	0	1	–	A_i	–	A's & B's	in-phase
B_i	OVRF	0	1	1	0	A_i	–	A's & B's	None	out-of-phase
B_i	C_{n+4}	0	1	1	0	A_i	–	A's & B's	None	out-of-phase
A_i	F_{i+1}	0	1	0	1	B_i	–	A's & B's	None	out-of-phase
B_i	F_{i+1}	1	0	0	1	A_i	–	A's & B's	None	out-of-phase
S_0	F_i	–	0	0	1	B_i	A_i	All B's	All A's	in-phase
S_0	OVRF	–	1	1	0	–	–	A's & B's	None	out-of-phase
S_0	C_{n+4}	–	1	1	0	–	–	None	A's & B's	out-of-phase
S_1	F_i	0	–	0	1	A_i	B_i	All A's	All B's	in-phase
S_1	OVRF	0	–	1	X	–	–	None	A's & B's	in-phase
S_1	C_{n+4}	0	–	1	X	–	–	None	A's & B's	in-phase
S_2	F_i	0	1	–	1	A_i	B_i	All A's	All B's	in-phase
S_2	OVRF	0	1	–	0	–	–	None	A's & B's	in-phase
S_2	C_{n+4}	0	1	–	0	–	–	None	A's & B's	in-phase

X = Don't care

TRUTH TABLE

	INPUTS						OUTPUTS					
FUNCTION	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	OVR	C_{n+4}
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1
				1	X	X	0	0	0	0	1	1
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	1	1	1	0	1
				0	1	0	0	0	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	1	0	1
				1	1	0	1	0	0	0	0	0
				1	1	1	0	0	0	0	0	1
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	0
				0	1	0	0	1	1	1	0	1
				0	1	1	1	1	1	1	0	0
				1	0	0	1	0	0	0	0	1
				1	0	1	0	0	0	0	0	0
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	0	1
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	1	1	1	0	1
				1	0	0	1	0	0	0	0	0
				1	0	1	0	0	0	0	0	1
				1	1	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	0	1
A ⊕ B	0	0	1	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	0	0	0	1	1
				1	0	0	0	0	0	0	0	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	1	1
A + B	1	0	1	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
AB	0	1	1	0	0	0	0	0	0	0	1	1
				0	0	1	0	0	0	0	0	1
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	0	1
				1	0	0	0	0	0	0	1	1
				1	0	1	0	0	0	0	0	1
				1	1	0	0	0	0	0	1	1
				1	1	1	1	1	1	1	1	1
PRESET	1	1	1	0	0	0	1	1	1	1	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	1	1	1	1	0	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	1	1	1	0	0
				1	1	1	1	1	1	1	0	1

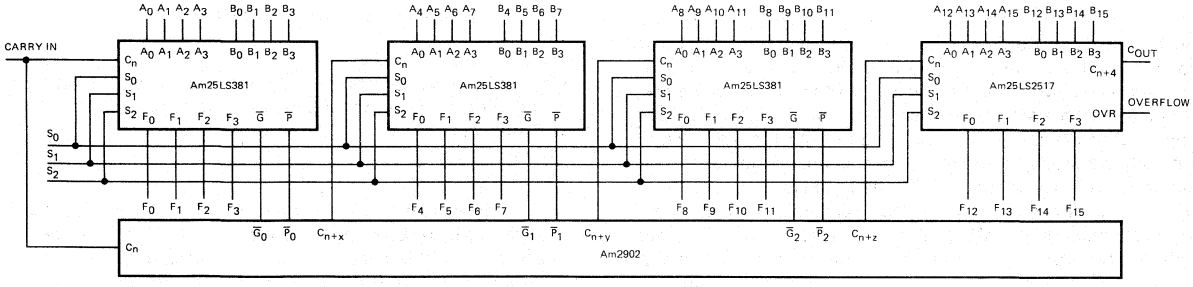
APPLICATIONS



TYPICAL SPEED CALCULATIONS

	Output	
Path	**F**	**C_{n+4}, OVR**
A_i or B_i to C_{n+4}	24 ns	24 ns
C_n to C_{n+4}	15 ns	15 ns
C_n to C_{n+4}	15 ns	15 ns
C_n to F_i	16 ns	–
C_n to C_{n+4}, OVR	–	15 ns
16-Bit Speed	70 ns	69 ns

The Am25LS2517 in a 16-Bit Ripple Carry ALU Connection.



TYPICAL SPEED CALCULATIONS

	Output	
Path	**F**	**C_{n+4}, OVR**
A_i or B_i to $\overline{G}$ or $\overline{P}$	20 ns*	20 ns*
$\overline{G}_i$ or $\overline{P}_i$ to C_{i+j} (Am 2902)	8 ns	8 ns
C_n to F	16 ns	–
C_n to C_{n+4}, OVR	–	15 ns
16-Bit Speed	44 ns	43 ns

* Note that S_i to G or P may be longer path.

The Am25LS2517 and Am25LS381 in a 16-Bit Carry Lookahead ALU Connection.

UNDERSTANDING THE Am25LS2517 AND THE Am25LS381

By John R. Mick

INTRODUCTION

The heart of most digital arighmetic processors is the arithmetic logic unit (ALU). The ALU can be thought of as a digital subsystem that performs various arithmetic and logic operations on two digital input variables. The Am25LS2517 and the Am25LS381 are Schottky TTL arithmetic logic units/function generators that perform eight arithmetic/logic operations on two four-bit input variables. In most ALU's, speed is generally a key ingredient. Therefore, as much parallelism in the operation of the arithmetic logic unit as possible is desired.

The Am25LS381 ALU is designed to operate with a '182 carry lookahead generator to perform multi-level full carry lookahead over any number of bits. Therefore, the Am25LS381 has both the carry generate and carry propagate outputs required by the '182 carry lookahead generator. The Am25LS2517, on the other hand, does not have the carry generate and carry propagate functions, but rather has the carry output (C_{n+4}) and a two's complement overflow detection signal (OVR) available at the output. The net result is that a very high-speed 16-bit arithmetic logic unit/function generator can be designed and assembled using three Am25LS381's, one Am25LS2517, and one Am2902 (the Am2902 is a high-speed version of the '182 carry lookahead generator).

UNDERSTANDING THE FULL ADDER

The results of an arithmetic operation in any position in a word depends not only on the two-input operand bits at that position, but also on all the lesser significant operand bits of the two input variables. The final result for any bit, therefore, is not available until the carries of all the previous bits have rippled through the logic array starting from the least significant bit and propagating through to the most significant bit. A full adder is a device that accepts two individual operand bits at the same binary weight, and also accepts a carry input bit from the next lesser significant weight full adder. The full adder then produces the sum bit for this bit position and also produces a carry bit to be used in the next more significant weight full adder carry input. The truth table for a full adder is shown in Figure 1. From this truth table, the equations for the full adder:

$$S = A \oplus B \oplus C$$
$$C_0 = AB + BC + AC,$$

where A and B are the input operands to the full adder and C is the carry input into the adder.

The sum output, S, represents the sum of the A and B operand inputs and the carry input. The carry output, C_0, represents the carry out of this cell and can be used in the next more significant cell of the adder. Full adder cells can be cascaded as depicted in Figure 2 to form a four-bit ripple carry parallel adder.

Inputs			Outputs	
A	B	C	S	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 1. Full Adder Truth Table.

Note that once we have cascaded devices as shown in Figure 2, we may wish to discuss the equations for the i-th bit of the adder. In so doing, we might describe the equations of the full adder as follows:

$$S_i = A_i \oplus B_i \oplus C_i$$
$$C_{i+1} = A_iB_i + B_iC_i + A_iC_i$$

where the A_i and B_i are the input operands at the i-th bit, and the C_i is the carry input to the i-th bit. (Note that the equations for this adder are iterative in nature and each depends on the result of the previous lesser significant bits of the adder array.)

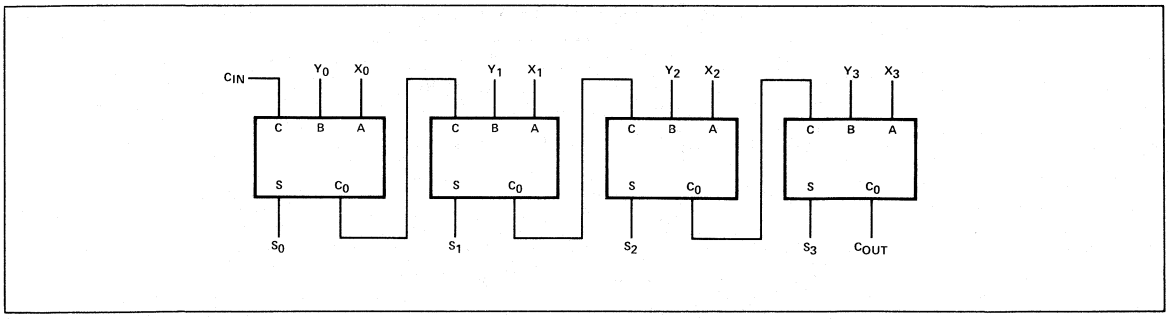


Figure 2. Cascaded Full Adder Cells Connected as a Four-Bit Ripple-Carry Full Adder.

The connection scheme shown in Figure 2 requires a ripple propagation time through each full adder cell. If a 16-bit adder is to be assembled, the carry will have to propagate through all 16 full adder cells. What is desired is some technique for anticipating the carry such that we will not have to wait for a ripple carry to progagate through the entire network. By using some additional logic, such an adder array can be constructed. This type of adder is usually called a carry lookahead adder.

A FOUR-BIT CARRY LOOKAHEAD ADDER

Looking back to the equations developed for i-th bit of an adder, let us now rewrite the carry equation in a slightly different form. When we factor the C_i in this equation, the new equation becomes:

$$C_{i+1} = A_iB_i + C_i (A_i + B_i)$$

From the above equation, let us now define two additional equations. These are:

$$G_i = A_iB_i$$

$$P_i = A_i + B_i$$

With these two new auxiliary equations, we can now rewrite the carry equation for the i-th bit as follows:

$$C_{i+1} = G_i + P_iC_i$$

Note that we have now developed two terms: the P_i term is known as carry propagate and the G_i term is known as carry generate. An anticipated carry can be generated at any stage of the adder by implementing the above equations and using the auxiliary functions P_i and G_i as required.

It is interesting to note that the sum equation can also be written in terms of these two auxiliary equations, P_i and G_i. For this case, the equation is:

$$S_i = (A_i + B_i) (A_iB_i) \oplus C_i$$

The auxiliary function G_i is called carry generate, because if it is true, then a carry is immediately produced for the next adder stage. The function P_i is called carry propagate because it implies there will be a carry into the next stage of the adder if there is a carry into this stage of the adder. That is, G_i causes a carry signal at the i-th stage of the adder to be generated and presented to the next stage of the adder while P_i causes an existing carry at the input to the i-th stage of the adder to propagate to the next stage of the adder.

Let us now write all of the sum and carry equations required for a full four-bit lookahead carry adder.

$$S_0 = A_0 \oplus B_0 \oplus C_0$$

$$S_1 = A_1 \oplus B_1 \oplus [G_0 + P_0C_0]$$

$$S_2 = A_2 \oplus B_2 \oplus [G_1 + P_1G_0 + P_1P_0C_0]$$

$$S_3 = A_3 \oplus B_2 \oplus [G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0]$$

$$C_{i+4} = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$$

An important point to note is that all of the sum equations and the final carry output equation, C_{i+4}, can be written in terms of the A_i, B_i, and C_0 inputs to the four-bit adder. The configuration as described above is shown in Figure 3. This figure is divided into two parts — the upper blocks show the auxiliary function generator circuitry required to implement the P_i and G_i equations while the lower block implements the logic required to generate the sum output at each bit position.

A serious drawback to the lookahead carry adder is that as the word length is increased, the carry functions become more and more complex, eventually becoming impractical due to the large number of interconnections and heavy loading of the G_i and P_i functions. The auxiliary function concept can be extended, however, by dividing the word length into fairly small increments and defining blocks of auxiliary functions G and P.

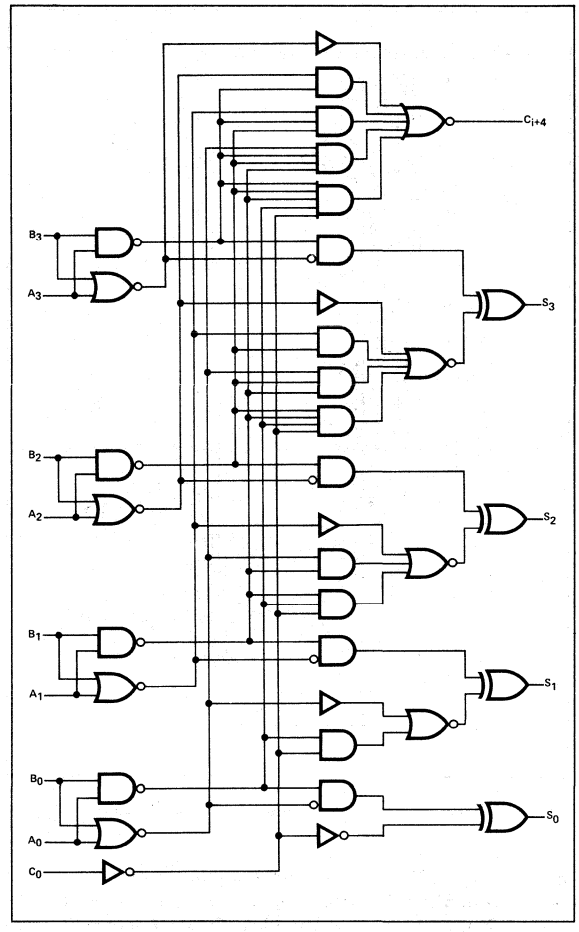


Figure 3. Full Four-Bit Carry-Lookahead Adder.

It is possible for a given block, to define a function G as the carry out generated with the block; and P can be defined as the carry propagate over the block. If the block size is set at four bits, then the functions for G and P for this block can be defined as follows:

$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$

$$P = P_3P_2P_1P_0$$

It is important to note that neither of these terms involves a carry-in (C_0) to the block, so no matter how many blocks are tied in an adder, all the blocks have stable G and P functions available in a minimum number of gate delays.

The G and P functions can be gated to produce a carry-in to each four-bit block, as a function of the lesser significant blocks. The carry-in to a block in is therefore:

$$C_n = G_{n-1} + P_{n-1}G_{n-2} + P_{n-1}P_{n-2}G_{n-3} + \ldots + P_{n-1}P_{n-2}P_{n-3} \ldots P_2P_1P_0C_0$$

Finally, the carry-in to each of the bits in a four-bit block must include a term for the actual least significant carry-in; note, therefore, that the equations for the four-bit full adder presented above include a term for carry-in at each bit position. Figure 4 shows the logic diagram for the Am25LS381 arithmetic logic unit/function generator while Figure 5 shows the logic diagram for the Am25LS2517 arithmetic logic unit/function generator. Note the generate and propagate outputs

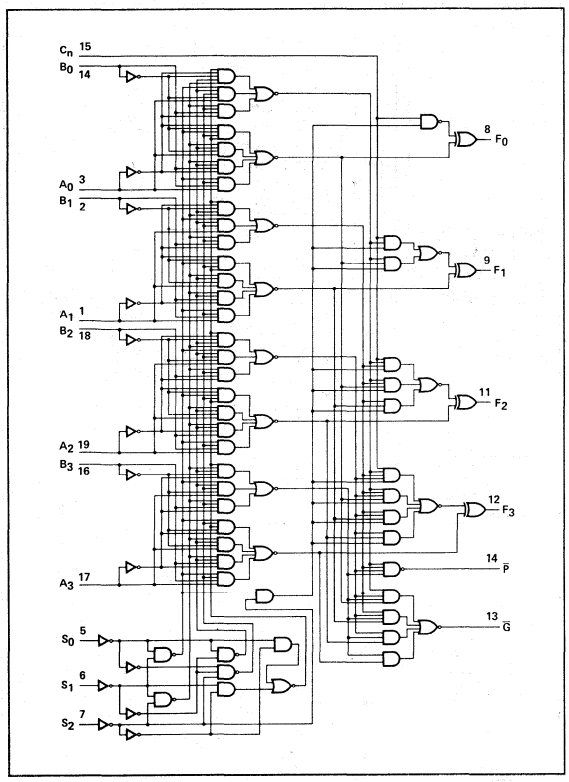


Figure 4. Logic Diagram of The Am25LS381.

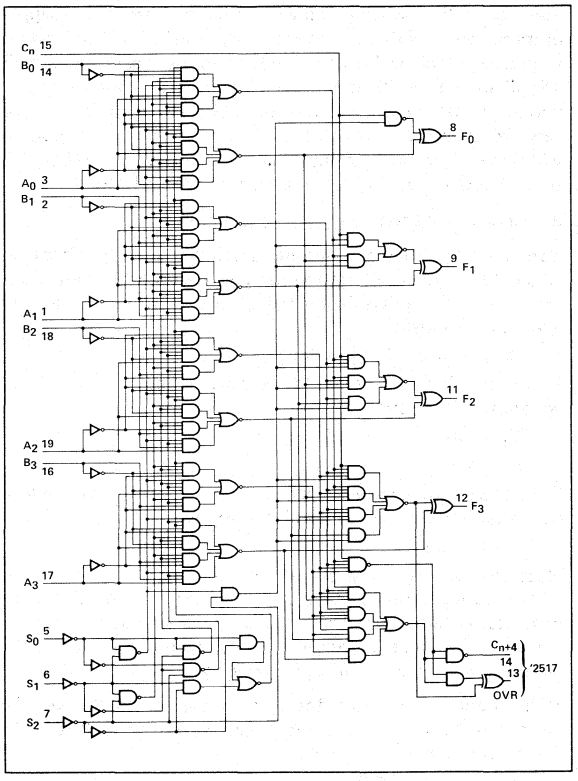


Figure 5. Logic Diagram of the Am25LS2517.

on the Am25LS381, and the carry output and overflow output on the Am25LS2517. Figure 6 gives the function table for both the Am25LS2517 and Am25LS381. Figure 7 shows the technique for cascading three Am25LS381's, one Am25LS2517, and one Am2902 in a full 16-bit high-speed carry lookahead connection. Figure 8 shows a connection scheme using only four Am25LS2517's in a 16-bit arithmetic logic unit connection where the carries are rippled between the devices. Each Am25LS2517 does use internal carry lookahead over the four-bit block.

In summary, the ripple carry method can be used in conjunction with the lookahead technique in several ways.

1. Lookahead carry over sections of the adder and ripple carry between these sections of the adder can be used. This method is often the most efficient in terms of hardware for

Selection			Arithmetic/Logic Operation
S_2	S_1	S_0	
L	L	L	Clear
L	L	H	B Minus A
L	H	L	A Minus B
L	H	H	A Plus B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	Preset

H = High Level, L = Low Level

Figure 6. Function Table for the Am25LS2517 and Am25LS381.

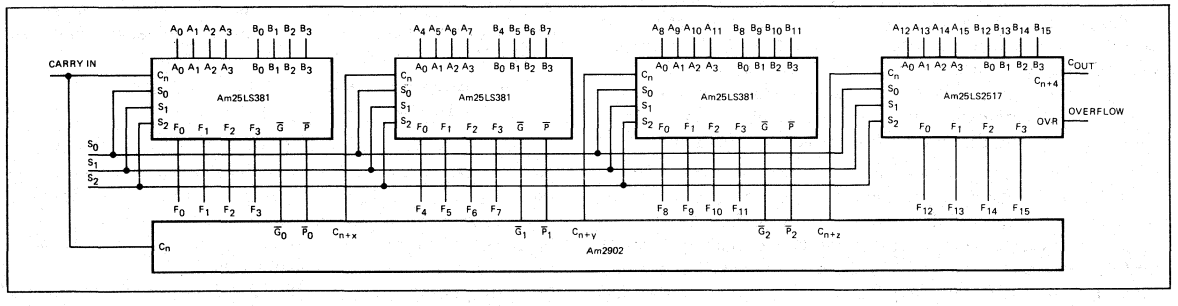


Figure 7. Full Lookahead Carry 16-Bit Adder.

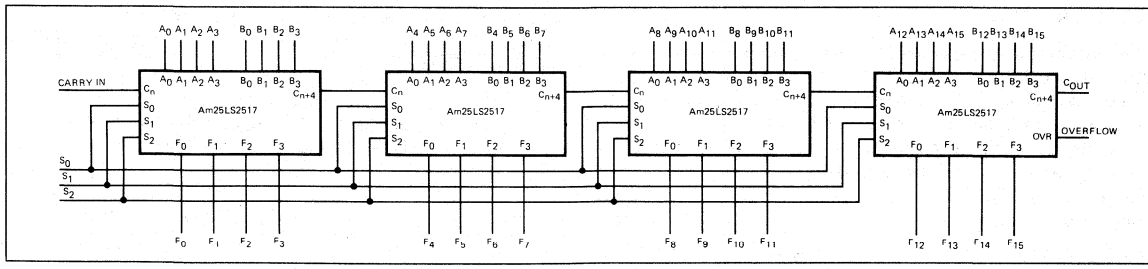


Figure 8. Connection of 16-Bit ALU Using Ripple Carry.

a given speed requirement. It does not require the use of a lookahead carry generator such as the Am2902.

2. Lookahead carry across 16-bit blocks with a ripple carry between 16-bit blocks can be used. This technique is usually called two-level carry lookahead addition. This technique results in very high-speed arithmetic function generation and makes a reasonable tradeoff between the speed and hardware for word lengths greater than 16 bits.
3. Full lookahead carry across all levels and all block sizes can be used. This is the highest speed arithmetic logic unit connection scheme. For word sizes up to 64 bits, it is referred to as three-level lookahead carry addition. Such a 64-bit ALU requires the use of five Am2902 carry lookahead generator units in addition to the 15 Am25LS381 devices and one Am25LS2517 as shown in Figure 9.

OVERFLOW

When two's complement numbers are added or subtracted, the result must lie within the range of the numbers that can be handled by the operand word length. Numbers are normally represented either as fractions with a binary point between the sign bit and the rest of the word, or as integers where the binary point is after the least significant bit. The actual choice for the location of the binary point is really up to the design engineer, as the hardware configuration required for either technique is identical. It is also possible to use number notations that include both integer and fractional representations in the same numbering scheme. Overflow is defined as the situation where the result of an arithmetic operation lies outside of the number range that can be represented by the number of bits in the word. For example, if two eight-bit numbers are added and the result does not lie within the number range that can be represented by an eight-bit word, we say that an overflow has occured. This can happen at either the positive end of the number range or at the negative end of the number range. The logic function that indicates that the result of an operation is outside of the representable number range is:

$$OVR = C_S \oplus C_{S+1}$$

where C_S is the carry-in to the sign bit and C_{S+1} is the carry-out of the sign bit.

Thus, for a four-bit ALU with the sign bit in the most significant bit position, the overflow can be defined as the C_{n+4} term exclusive OR'ed with the C_{n+3} term.

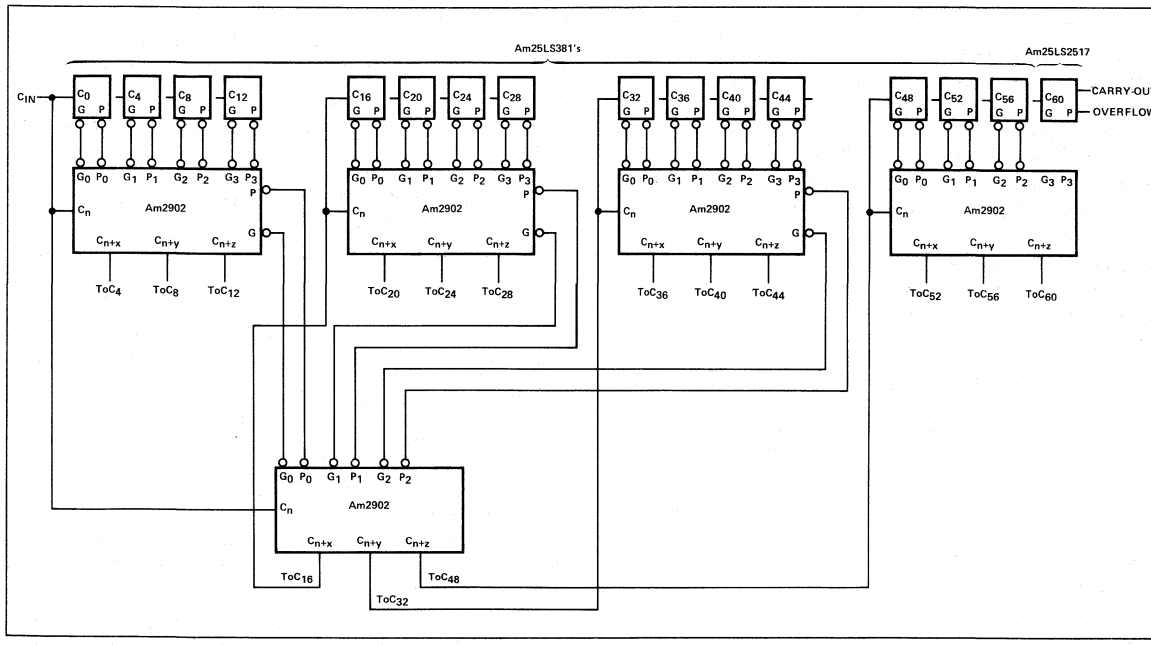


Figure 9. 64-Bit ALU with Full Carry Lookahead Using 5 Am2902's, 15 Am25LS381's and 1 Am25LS2517.

SPEED OR DELAY

Usually, the most important parameter in the design of any arithmetic logic unit is speed. How fast can two numbers be added? Is ripple carry sufficient or should carry lookahead over the entire adder array be used? In order to answer these questions, the design engineer must first evaluate the speed of the ALU required in his system. Then he can evaluate the various alternatives based on the number of bits in the word being used in the design.

The calculation of the speed (add or subtract time) of a 16-bit adder is straightforward and will be discussed in detail. It should be mentioned that the speed of the adder while in the logic mode is simply the propagation delay from the A_i or B_i inputs to the F_i outputs (35ns maximum at 25°C and 5V for the Am25LS2517).

LOOKAHEAD CARRY

The typical method for building 16-bit ALU's is to employ a carry lookahead generator such as the Am2902. Such a 16-bit design would incorporate three Am25LS381's, one Am25LS 2517, and one Am2902. For the 16-bit full carry lookahead adder in the add or subtract mode as shown in Figure 7, the maximum propagation delay for data-in to data-out is calculated as follows:

DATA PATH DELAY
16-BIT LOOKAHEAD ADDER/SUBTRACTOR
(+5V and 25°C Maximum Delays)

Path	Output			Units
	F_i	C_{n+4}	OVR	
A_i or B_i to $\overline{G}$ or $\overline{P}$	27	27	27	ns
G_i or P_i to C_{i+j} (Am2902)	10	10	10	ns
C_n to F_i	23	–	–	ns
C_n to C_{n+4} or OVR	–	22	22	ns
TOTAL 16-bit delay	60	59	59	ns

The data path for this computation begins at the least significant 4-bit device, propagates through the Am2902, and then ends at the most significant 4-bit device. Actually, the delay to the outputs of the most significant device (MSD), then second MSD, or third MSD is identical.

Thus, the above speed is identical if a 12-bit ALU is fabricated. This results because the same types of combinatorial propagation delays are involved.

We should also investigate the delay of this adder with regard to the select inputs as shown in Figure 7. Again, we may calculate the 16-bit full carry lookahead add/subtract delay as follows:

16-BIT LOOKAHEAD ADDER DELAY
FOR SELECT INPUTS
(+5V and 25°C Maximum Delays)

Path	Output			Units
	F_i	C_{n+4}	OVR	
S_i to $\overline{G}$ or $\overline{P}$	48	48	48	ns
G_i or P_i to C_{i+j} (Am2902)	10	10	10	ns
C_n to F_i	23	–	–	ns
C_n to C_{n+4} or OVR	–	22	22	ns
TOTAL 16-bit delay	81	80	80	ns

Let us examine the speed of a 64-bit arithmetic logic unit fabricated as shown in Figure 9. The worst case path for this design is as follows:

DATA PATH DELAY
64-BIT LOOKAHEAD ADDER/SUBTRACTOR
(+5V and 25°C Maximum Delays)

Path	Output			Units
	F_i	C_{n+4}	OVR	
A_i or B_i to $\overline{G}$ or $\overline{P}$	27	27	27	ns
G_i or P_i to G_i or P_i (Am2902)	14	14	14	ns
G_i or P_i to C_{i+j} (Am2902)	10	10	10	ns
C_n to C_{i+j} (Am2902)	14	14	14	ns
C_n to F_i	23	–	–	ns
C_n to C_{n+4} or OVR	–	22	22	ns
TOTAL 16-bit delay	88	87	87	ns

The above example demonstrates the speed improvement when using carry lookahead over the entire array. When this 64-bit example is compared with the previous 16-bit example, it will be found that the only difference is the addition of two Am2902 delays.

RIPPLE CARRY

The slowest speed ALU design employs the ripple carry technique. When four-bit devices such as the Am25LS2517 are employed in such an ALU, the speed is usually computed using the combinatorial delay terms in the following manner.

1. Select the longest combinatorial delay in the least significant device from any input to the carry output, C_{n+4}. This is usually from the A or B inputs to the carry output.
2. Add the carry input to carry output propagation delay as many times as required to represent each of the intermediate four-bit ALU's.
3. Finally, take the propagation delay from the carry input to the ALU adder outputs.

When the above rules are followed, the total worst case propagation delay over the entire ALU bit width is derived.

If we consider the ripple carry adder/subtractor configuration as shown in Figure 8, the propagation delay for the data input to data output path is computed as follows:

DATA PATH DELAY
16-BIT RIPPLE CARRY ADDER/SUBTRACTOR
(+5V and +25°C Maximum Delays)

Path	Output			Units
	F_i	C_{n+4}	OVR	
A_i or B_i to C_{n+4}	36	36	36	ns
C_n to C_{n+4}	22	22	22	ns
C_n to C_{n+4}	22	22	22	ns
C_n to F_i	23	–	–	ns
C_n to C_{n+4} or OVR	–	22	22	ns
TOTAL 16-bit delay	103	102	102	ns

In this connection, the maximum delay begins at the least significant device and propagates through the most significant device via the ripple carry path.

The select to output delay is computed in a similar manner using S_i to C_{n+4} as the first term and is found to be:

S_i to F_i = 122ns; S_i to C_{n+4} = 12ns; S_i to OVR = 121ns

The ripple carry computational examples show the speed of a 16-bit ALU function/generator built using four Am25LS 2517's.

COMPARING THE '2517/'381 WITH THE '181

To compare the performance of the Am25LS2517 and LS381, we should evaluate the various '181 ALU's connected in a 16-bit configuration with the Am2902 carry lookahead generator used in all configurations as shown in Figure 7. The comparison for the A_i or B_i to F_i add/subtract time is as follows:

COMPARISON OF 16-BIT ADDER/SUBTRACTOR DATA DELAY USING 4 ALU's AND 1 Am2902

ALU Device	Maximum Add/Subtract Delay +5V and 25°C	Maximum Power* V_{CC} = +5.25V
Am74S181	37ns	914mA
Am74181	64ns	694mA
Am74LS181	69ns	242mA
Am25LS181	55ns	242mA
Am25LS381/Am25LS2517	60ns	266mA

*Note: Of this power, 94mA is the Am2902

Even more important is the comparison of "System Speed" normally associated with the ALU function. If we assume the system configuration as shown in Figure 10, then a reasonable comparison of speed for A_i or B_i to OVERFLOW can be made as follows:

SPEED AND POWER FOR ALU SYSTEMS OF FIGURE 10

Path	All "S"	All 25LS	All 74LS	All Gold Doped	'LS381 'LS2517	Units
A_i or B_i to G or P	15	26	33	25	27	ns
G or P to C_{i+j} (Am2902)	10	10	10	10	10	ns
C_n to OVR	–	–	–	–	22	ns
C_n to F_3	12	19	26	19	–	ns
C_{out} to OVR	21	–	60	60	–	ns
TOTAL	58	55	129	114	59	ns
POWER	998		253	748	266	mA

*no 25LS

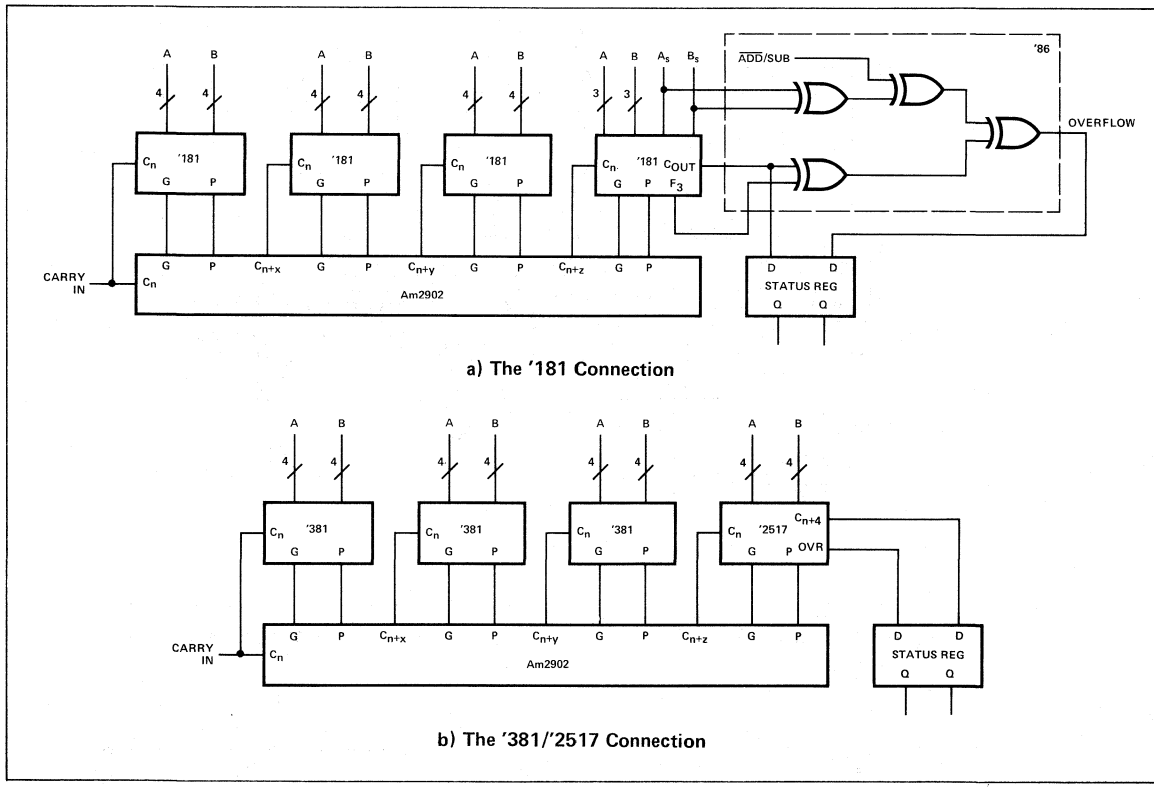


Figure 10. The Normal ALU System.

SUMMARY

The Am25LS381 and Am25LS2517 offer superior performance utilizing the space saving 20-pin package. The data add/subtract time compares very favorably with the 74181 and 74S181 with a considerable reduction (1/3 to 1/4) in dissipated power. The Am25LS381 and Am25LS2517 combination provide the OVR function not currently available or easily to implement on any '181 configuration. The 20-pin package configuration offers at least a 2:1 saving in PC board area compared to the '181 24-pin package approach.

Am25LS2513

Three-State Priority Encoder

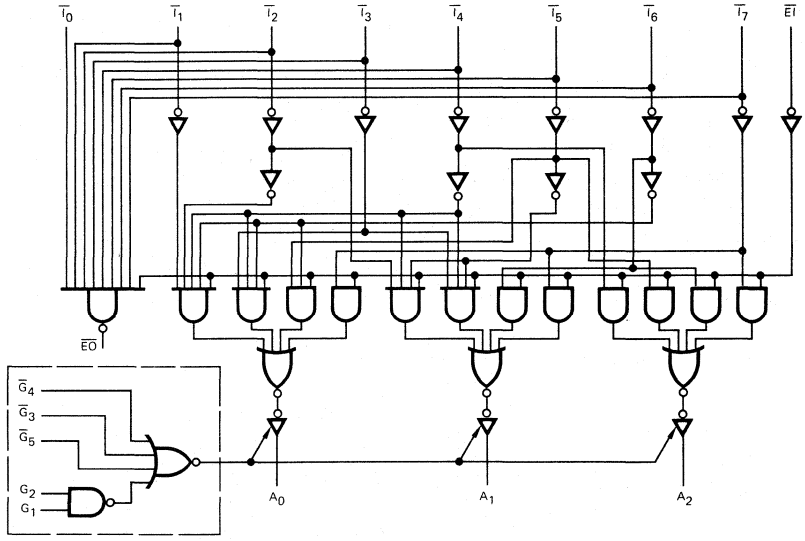
DISTINCTIVE CHARACTERISTICS

- Encodes eight lines to three-line binary
- Expandable
- Cascadable
- Three State inverted output version of Am54LS/74LS/25LS148
- Gated three-state output
- Advanced Low-Power Schottky processing
- 100% product assurance screening to MIL-STD-883 requirements

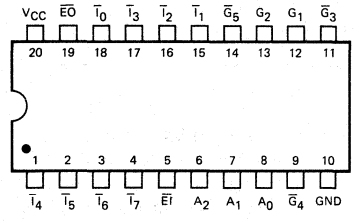
FUNCTIONAL DESCRIPTION

The Am25LS2513 Low-Power Schottky Priority Encoder performs priority encoding of 8 inputs to provide a binary-weighted code of the priority order of the 3 tri-state active HIGH outputs A_0, A_1, A_2. Three active LOW and two active HIGH inputs in AND-OR configuration allow control of the tri-state outputs. The use of the input enable ($\overline{EI}$) combined with the enable output ($\overline{EO}$) permits cascading without additional circuitry. Enable input ($\overline{EI}$) HIGH will force all outputs LOW subject to the tri-state control. The enable output is LOW when all inputs $\overline{I_0}$ through $\overline{I_7}$ are HIGH and the enable input is LOW.

LOGIC DIAGRAM

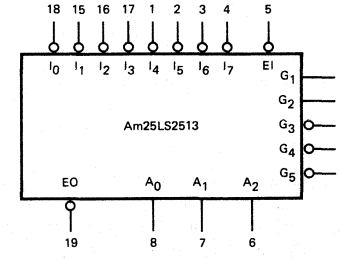


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



Am25LS2513

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75V	MAX. = 5.25V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50V	MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	A_i	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
				COM'L, $I_{OH} = -2.6mA$	2.4	3.2		
			$\overline{EO}$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA (A_n$ Outputs)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{EI}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				−0.4	mA
			All others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{EI}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				20	μA
			All others				40	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$	$\overline{EI}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				0.1	mA
			All others				0.2	
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				15	24	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs and outputs open.

Am25LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	$\overline{I_i}$ to A_n (In-phase)		17	25	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	$\overline{I_i}$ to A_n (Out-phase)		11	17	ns	
t_{PHL}			12	18		
t_{PLH}	$\overline{I_i}$ to $\overline{EO}$		7.0	11	ns	
t_{PHL}			24	36		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		11	17	ns	
t_{PHL}			23	34		
t_{PLH}	$\overline{EI}$ to A_n		12	18	ns	
t_{PHL}			14	21		
t_{ZH}	G_1 or G_2 to A_n		23	40	ns	
t_{ZL}			20	37		
t_{ZH}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		20	30	ns	
t_{ZL}			18	27		
t_{HZ}	G_1 or G_2 to A_n		17	27	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			19	28		
t_{HZ}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		16	24	ns	
t_{LZ}			18	27		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	$\overline{I_i}$ to A_n (In-phase)		31		37	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			30		34		
t_{PLH}	$\overline{I_i}$ to A_n (Out-phase)		22		27	ns	
t_{PHL}			22		25		
t_{PLH}	$\overline{I_i}$ to $\overline{EO}$		15		18	ns	
t_{PHL}			48		60		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		19		21	ns	
t_{PHL}			46		57		
t_{PLH}	$\overline{EI}$ to A_n		22		25	ns	
t_{PHL}			27		32		
t_{ZH}	G_1 or G_2 to A_n		42		49	ns	
t_{ZL}			43		49		
t_{ZH}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		36		43	ns	
t_{ZL}			35		43		
t_{HZ}	G_1 or G_2 to A_n		34		40	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			34		40		
t_{HZ}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		30		35	ns	
t_{LZ}			31		35		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Note: i = 0 to 7
n = 0 to 2

DEFINITIONS OF FUNCTIONAL TERMS

A0, A1, A2	Three-state, active high encoder outputs
$\overline{EI}$	Enable input provided to allow cascaded operation
$\overline{EO}$	Enable output provided to enable the next lower order priority chip
G_1, G_2	Active high three-state output controls
$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$	Active low three-state output controls
$\overline{I}_{0\text{-}7}$	Active low encoder inputs

TRUTH TABLE

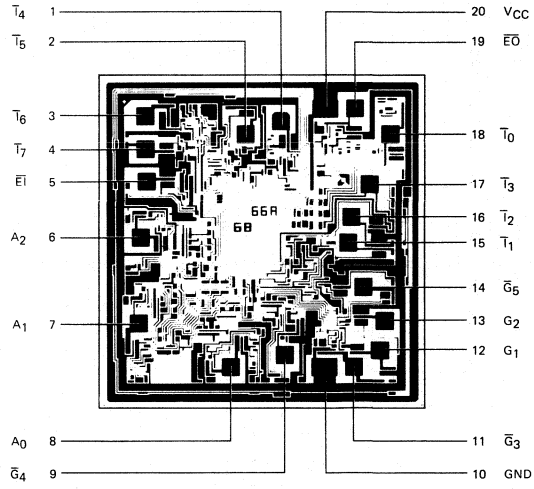
Inputs									Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G_1 = H, G_2 = H, G_3 = L, G_4 = L, G_5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

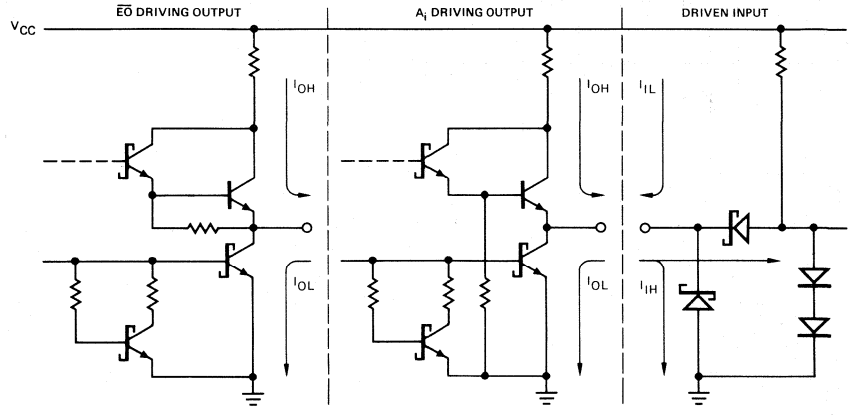
Z = HIGH Impedance

Metallization and Pad Layout



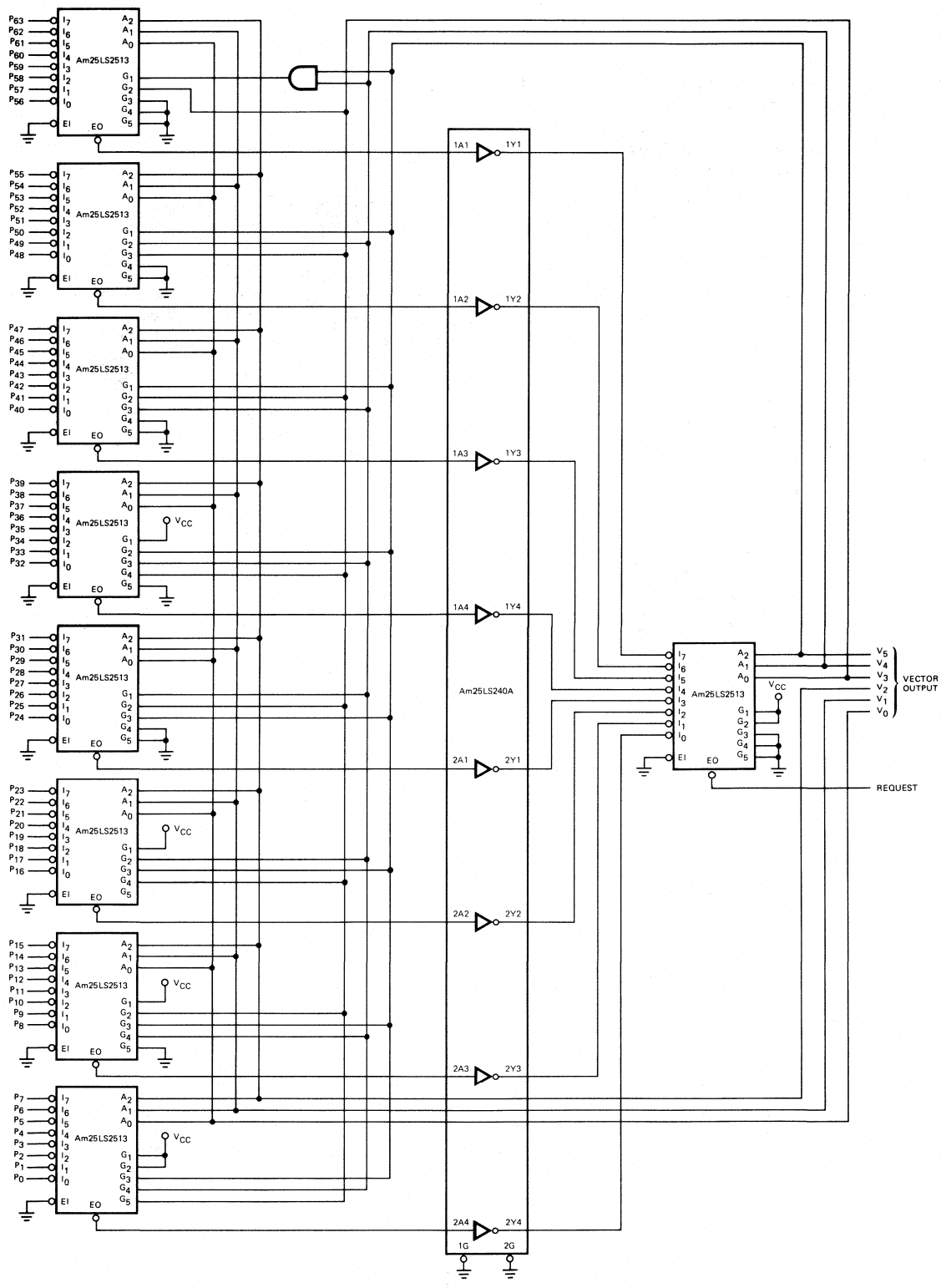
DIE SIZE 0.082 X 0.085

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATION

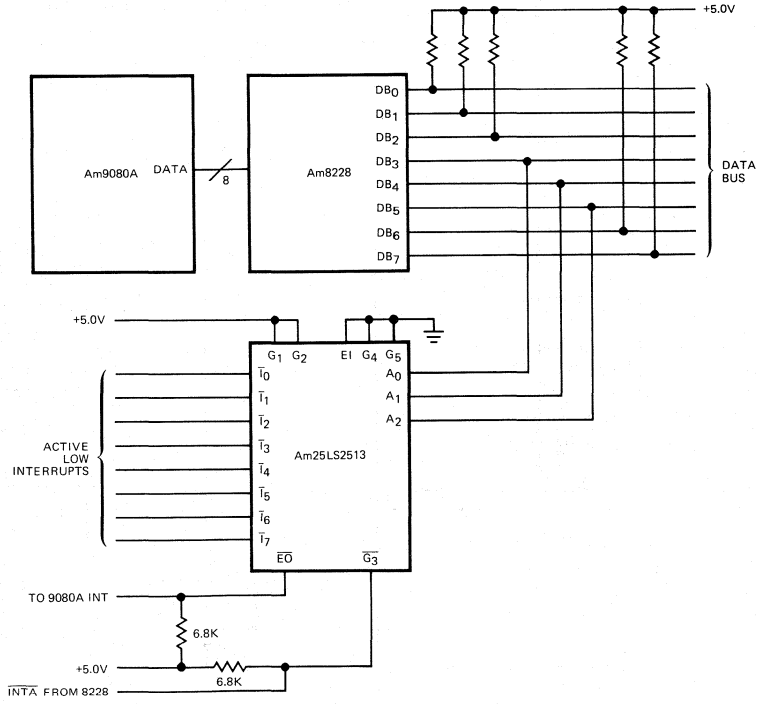


64 Input Priority Encoder Connected for Parallel Enable

ORDERING INFORMATION

Package Type	Temperature Range	Am25LS2513 Order Number
Molded DIP	0°C to +70°C	AM25LS2513PC
Hermetic DIP	0°C to +70°C	AM25LS2513DC
Dice	0°C to +70°C	AM25LS2513XC
Hermetic DIP	−55°C to +125°C	AM25LS2513DM
Hermetic Flat Pak	−55°C to +125°C	AM25LS2513FM
Dice	−55°C to +125°C	AM25LS2513XM

PRIORITY ENCODED RST INTERRUPT INSTRUCTION FOR THE Am9080A



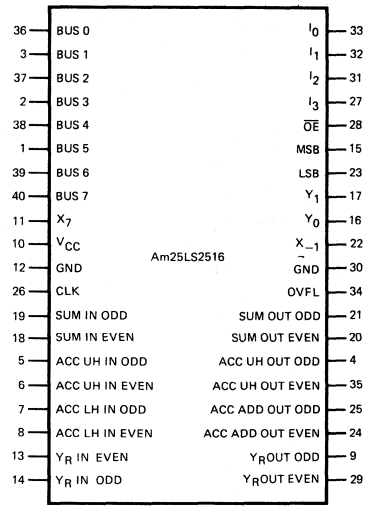
Am25LS2516

Eight-Bit by Eight-Bit Serial/Parallel Multiplier with Accumulator

DISTINCTIVE CHARACTERISTICS

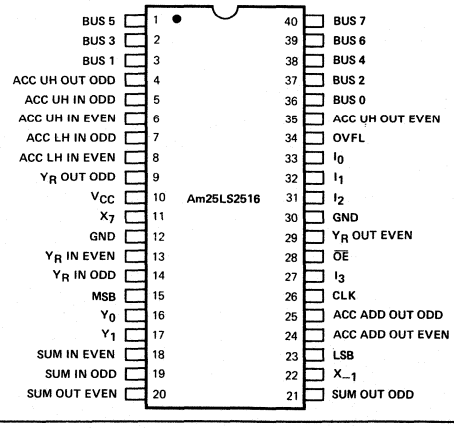
- Two's complement, two-bit lookahead carry-save arithmetic
- Microprogrammable — four-bit instruction code for load, multiply, and read operations
- Cascadable, two devices perform full 16-bit multiplication without additional hardware
- Eight-bit byte parallel, bidirectional, bussed I/O
- On-chip registers and double length accumulator
- Overflow indicator
- Three-state shared bus input/output lines
- High-speed architecture provides clock rates of 20MHz (Typ)
- 100% product assurance screening to MIL-STD-883 requirements

LOGIC SYMBOL



MPR-336

CONNECTION DIAGRAM



MPR-337

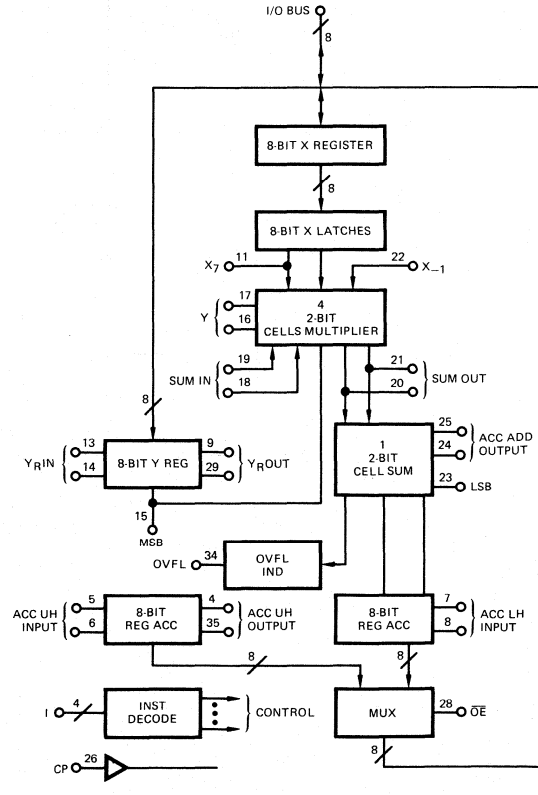
FUNCTIONAL DESCRIPTION

The Am25LS2516 is an eight-bit by eight-bit multiplier and accumulator employing serial/parallel, two's complement, carry-save arithmetic to deliver a 16-bit product in eight clock cycles. The device is fully cascadable for use in high-speed, real-time, digital signal processing applications.

The device includes an eight-bit X Register prior to the X latch providing X hold for chain or overlapping calculations. The X and Y registers are loaded by clocking prior to the beginning of a multiply cycle, the data supplied by the bidirectional bus or the accumulator register. The double length, 16-bit output is multiplexed onto the eight-bit bus; either the upper or lower halves of the result can be read at any one time.

The accumulator and the Y register are both organized as dual-rank shift registers, allowing them to shift two bits at a time. The serial inputs and outputs of the Y register, the low and high order halves of the accumulator and the two-bit serial accumulator adder output, both serially and in parallel, are all available at external pins to provide cascadability.

LOGIC DIAGRAM



MPR-338

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	MIN. = 4.75V	MAX. = 5.25V
MIL	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%	MIN. = 4.50V	MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

(Bus Inputs/Outputs)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V					−0.8	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					60	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					0.2	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−100	mA
I_{OZ}	Off-State (HIGH Impedance) Output Current	V_{CC} = MAX.	V_O = 2.4V				60	μA
			V_O = 0.4V				−800	

Non-Bus Inputs/Outputs

V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −440μA	MIL	2.5			Volts
				COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_R OUT, I_{OL} = 15mA				0.5	Volts
			Others I_{OL} = 4.0mA				0.4	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		Y_0, Y_1			0.8	Volts
				Others, MIL			0.7	
				Others, COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				See Table 1		mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				See Table 1		μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				See Table 1		mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				285	390	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Pins 28 and 31 HIGH, all other inputs at GND. Test after one full clock cycle of LOW-HIGH-LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Case) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to + V_{CC} max.
DC Input Voltage (Pins 5, 6, 7, 8, 18, 19, 26)	−0.5V to +5.5V
DC Input Voltage (Other pins)	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

TABLE I.

Terminals	I_{IL}	I_{IH}	I_I
Y IN	−.3mA	20μA	.1mA
I_0, I_1, I_3, OE	−.45mA	20μA	.1mA
Bus 0-7	−.6mA	90μA	.3mA
CP	−.8mA	80μA	.4mA
I_2, X_{-1}	−.9mA	40μA	.1mA
SUM IN	−1.4mA	80μA	.5mA
LSB	−1.6mA	80μA	.4mA
ACC IN all	−2mA	50μA	1mA
MSB	−3mA	150μA	1.5mA
Y_0, Y_1	−7.5mA	200μA	2mA

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	AM25LS2516DC
	−55°C to +125°C	AM25LS2516DM (Note 1)

Note 1. Military temperature range product in development.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Y_R Register OUT		12	18	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			15	23		
t_{PLH}	SUM OUT		13	20	ns	
t_{PHL}			15	23		
t_{PLH}	ACC ADDER OUT		27	41	ns	
t_{PHL}			27	41		
t_{PLH}	ACC UH OUT		11	17	ns	
t_{PHL}			13	20		
t_{PLH}	ACC Bus		23	34	ns	
t_{PHL}			17	26		
t_{PLH}	$\overline{OVFL}$		12	18	ns	
t_{PHL}			15	23		
t_{PLH}	X_7		13	20	ns	
t_{PHL}			17	26		
t_{ZH}	$\overline{OE}$ to Bus		12	18	ns	
t_{ZL}			9	14		
t_{HZ}			24	36	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			12	18		
t_s	X Register (Bus)	20			ns	C_L = 15pF, R_L = 2.0kΩ
t_s	Y Register (Bus)	15			ns	
t_s	X_{-1}	35			ns	
t_s	SUM IN	37			ns	
t_s	Y Register (Serial)	20			ns	
t_s	ACC LH or UH IN	8			ns	
t_s	Multiplier Y_0 and Y_1	33			ns	
t_s	Instruction	25			ns	
t_h	SUM IN, X_{-1}, Multiplier Y_0 and Y_1	0			ns	
t_h	I_{0-3} Hold Time	10			ns	
t_h	Hold Time on All Other Inputs	5			ns	
f_{max} (Note 1)	Maximum Clock Frequency	17			MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

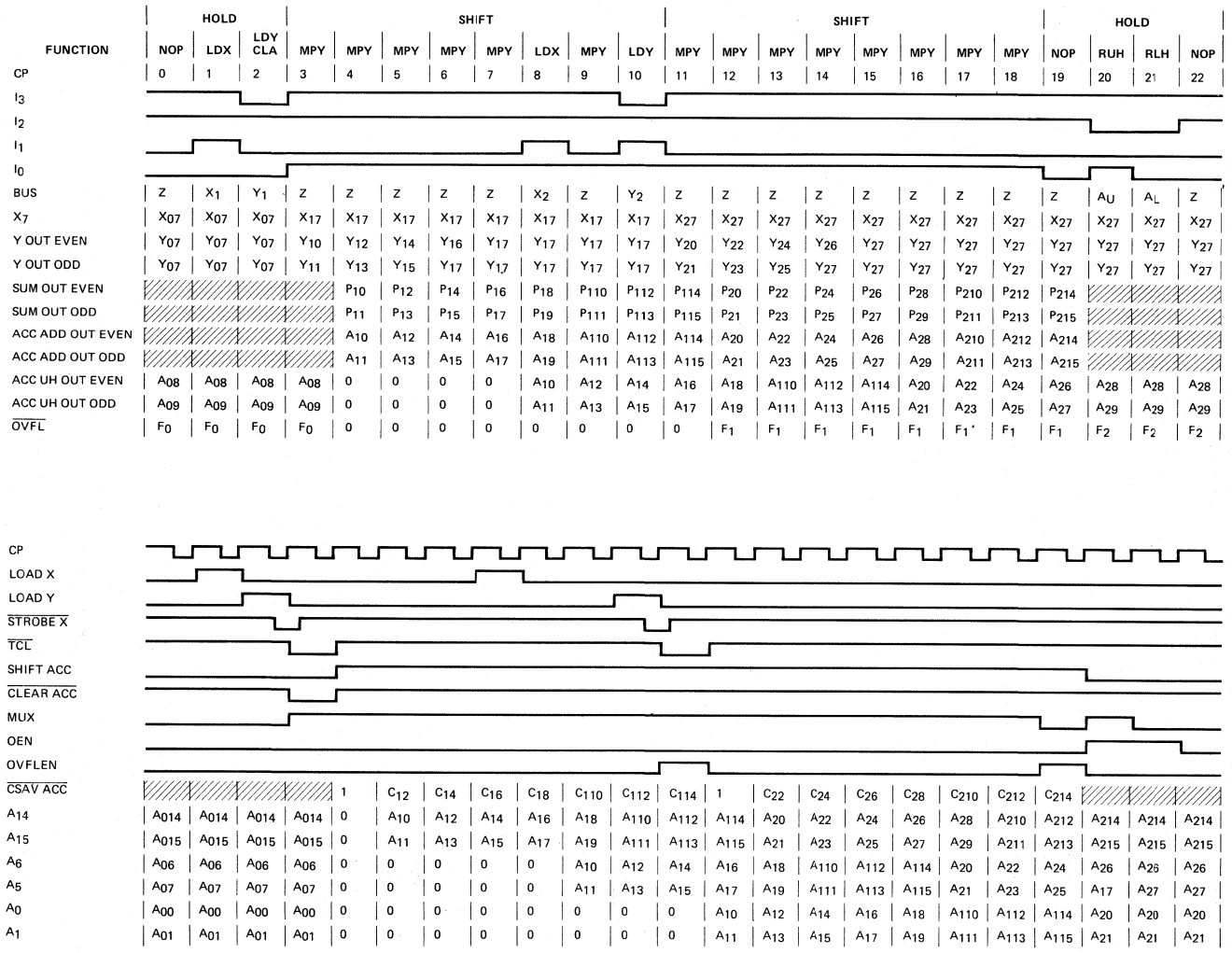
Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	YR Register OUT		24		26	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			33		37		
t_{PLH}	SUM OUT		27		27	ns	
t_{PHL}			34		34		
t_{PLH}	ACC ADDER OUT		50		52	ns	
t_{PHL}			57		60		
t_{PLH}	ACC UH OUT		23		23	ns	
t_{PHL}			30		30		
t_{PLH}	ACC Bus		42		45	ns	
t_{PHL}			38		39		
t_{PLH}	$\overline{OVFL}$		26		26	ns	
t_{PHL}			33		33		
t_{PLH}	X_7		30		33	ns	
t_{PHL}			39		42		
t_{ZH}	$\overline{OE}$ to Bus		30		33	ns	C_L = 50pF, R_L = 2.0kΩ
t_{ZL}			21		23	ns	
t_{HZ}			45		55	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			21		30	ns	
t_S	X Register (Bus)	20		22		ns	C_L = 50pF, R_L = 2.0kΩ
t_S	Y Register (Bus)	15		17		ns	
t_S	X_{-1}	45		51		ns	
t_S	SUM IN	52		62		ns	
t_S	Y Register (Serial)	20		20		ns	
t_S	ACC LH or UH IN	10		14		ns	
t_S	Multiplier Y_0 and Y_1	44		51		ns	
t_S	Instruction	27		30		ns	
t_H	SUM IN, X_{-1}, Multiplier and Y_1	0		0		ns	
t_H	I_{0-3} Hold Time	10		10		ns	
t_H	All Other Inputs	5		5		ns	
f_{max} (Note 1)	Maximum Clock Frequency	15.5		10		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

The following table provides a guide to the improvement in performance which may be obtained by control of the V_{CC} power supply.

	V_{CC} = 5.0V	V_{CC} = 5.0V ±5%	V_{CC} = 5.0V ±10%
T_A = 25°C	17MHz	16MHz	15MHz
T_A = 0°C to +70°C	16MHz	15.5MHz	–
T_C = −55°C to +125°C	12MHz	–	10MHz

TIMING DIAGRAMS



KEY:
////// Data invalid

Note: Variables shown are general.
For this example:

$P_1 = X_1Y_1$ $A_1 = P_1$ $F_1 = 0$
$P_2 = X_2Y_2$ $A_2 = P_1 + P_2$

DEFINITION OF FUNCTIONAL TERMS

Bus 0-Bus 7 – Bi-directional 8-bit data bus.

X_7 – Interconnection link to more significant byte if cascading (output).

X_{-1} – Interconnecting link between devices to least significant byte if cascading (input) link X7 to X1 to cascade – must be ground if not used.

Accum Upper Half out, even – Accumulator output upper byte, even bit.

Accum Upper Half out, odd – Accumulator output upper byte, odd bit.

Accum Upper Half input even – Accumulator input, upper byte, even bit.

Accum Upper Half input odd – Accumulator input, upper byte, odd bit.

Accum Lower Half input even – Accumulator input, lower byte, even bit.

Accum Lower Half input odd – Accumulator input, lower byte, odd bit.

YR out even – "Y" register output, even (link to "Y0").

YR out odd – "Y" register output, odd (link to "Y1").

YR in even – "Y" register input, even (link for cascading) ground when not used.

YR in odd – "Y" register input, odd (link for cascading) ground when not used.

Y_1 – Multiplier odd input (link to Y register odd).

Y_0 – Multiplier even input (link to Y register even).

Sum in even – Multiplier input even for cascading link to more significant byte, for standalone, ground.

Sum in odd – Multiplier input odd for cascading link to more significant byte, for standalone, ground.

Sum out even – Multiplier output even (link to sum in even for cascading) can be used directly.

Sum out odd – Multiplier output odd (link to sum output odd for cascading) can be used directly.

Acc Add out, even – Adder output even, for LSB (Hi) output equal sum of Accum and multiplier, for LSB (low) output equal sum of accumulator and zero.

Acc Add out, odd – Same as above except odd bit instead of even.

LSB – Control for summing adder – See Accumulator Add outputs for definition.

I_0-I_3 – 4-bit instruction field – provide cycle for cycle control of device function.

OVFL – Stored overflow indicator used only on least significant byte. Requires proper execution of instruction to operate.

MSB – Control for "Y" reg. and multiplier to indicate Most Significant Byte – Activates sign extension and negative waiting for 2's compliment – Low for lesser significant bytes and High for Most Significant Byte only.

CP – Clock Pulse.

$\overline{OE}$ – 3 state enable for Bus 0-Bus 7 outputs.

THE Am25LS2516 LSI MULTIPLIER/ACCUMULATOR

By Roy Levy

The Am25LS2516 is an 8-bit Multiplier/Accumulator designed for medium performance, minimum power, real time signal processing applications such as digital filtering, Fast Fourier Transforms, and statistical correlation. Using two's complement carry-save arithmetic, this 40-pin LSI device delivers a 16-bit product in eight clock cycles. This will permit two devices to be cascaded to achieve a 16-bit by 16-bit multiplication in 940ns when used over the full military operating range.

A functional block diagram of the Am25LS2516 is shown in Figure 1. The key elements are an 8-bit X input register followed by an 8-bit X latch, an 8-bit Y register, four 2-bit multipliers, a 2-bit adder, two 8-bit accumulators (high order and low order), a byte selecting multiplexer and instruction decode logic. These components, equivalent to approximately 625 gate elements, are integrated onto a single chip fabricated using Advanced Micro Devices' high-performance, Low-Power Schottky technology. The on-chip accumulator is provided to minimize component count and power dissipation in a high density system. It also allows completion of a multiply and accumulate operation in the same time normally required for a multiply only. Other LSI multipliers currently available require the accumulator function to be provided externally.

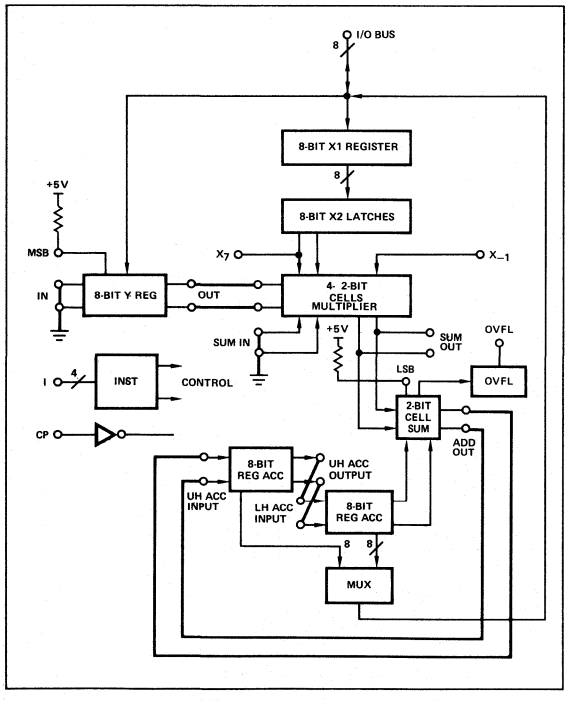


Figure 1. 8-Bit by 8-Bit Multiplier Block Diagram with External Connections Required to Accumulate A 16-Bit Product.

MULTIPLIER OPERATION

The Am25LS2516 is configured around an eight-line common input/output bidirectional bus. X and Y input and accumulator output data are routed via these bus lines. A two-rank register/latch combination is used for the X input to allow chaining of successive multiplies without losing a clock pulse; i.e., multiply and load vs. multiply. The latch holds the "X" data for the multiplier, allowing the X register to be loaded during any remaining multiply cycles. The "Y" Register can be parallel loaded, by command, from the 8-bit, on-chip bus from either the incoming 8 bits, or the Accumulator High or Accumulator Low Register (separate commands). The "Y" Register provides the 2-bit-at-a-time shift and the sign extend which allows the four 2-bit cells to operate in a serial by parallel mode. The multiplier produces a 2-bit product for each clock, LSB's first. Its output is accepted by the 2-bit adder as well as presented to external pins for expansion. A control gating array is provided to test for overflow during the last add cycle of the operation; i.e., cycle 8 for 8-bit multiply and cycle 16 for 16-bit multiply. The timing and control of this specific cycle is accomplished by the microcode chosen. The "HLDA" and "LYSA" instructions are provided for this purpose. The first cycle of a HOLD A following a multiply will cause the results of the overflow test to be stored. Two 8-bit accumulators are provided which must be externally connected in either an 8-bit, 16-bit, or greater configuration.

These accumulators as well as the Y Register, are both organized as dual-rank shift registers, which allow them to shift two bits at a time. The serial inputs and outputs of the Y Register and the low and high order halves of the accumulator are all brought out to external pins for cascading the device.

The accumulator output is available both serially and in parallel. The accumulator results are available one bit later than the multiply cycle and the accumulator stops shifting during read cycles. If the device is used to compute X • Y products without accumulation, a minimum of two overhead cycles must accompany each multiply – one for reading the upper (lower) half of the accumulator and one for clearing of the accumulator during the loading of the X or Y Registers. An output multiplexer selects the high or low order accumulator contents for presentation to the bus in parallel 8 bits at a time.

The heart of this device is an 8-bit multiplier (Figure 2) made up of four 2-bit cells. Each cell has three inputs (2 bits wide), two dual carry-save full adders, with four flip-flops for temporary storage (two for carry-save and two for partial product). The multiplier is actually subdivided into two separate adders with appropriate carry-save. The first adder forms a partial sum representing 0, 1X, 2X, or 3X by using combinations of X and 2X. The control of this combination of Y_0 and Y_1, respectively, to form $Y_0X_n + Y_1X_n + 1$. This sum (nX) is the input for the second adder. The second adder combines the first adder (nX) sum with the stored partial product shifted two places plus carry to form a new partial product.

$$P_{0MSB} + nX_0 + C = P_{0LSB}$$
$$P_{1MSB} + nX_1 + C = P_{1LSB}$$

The two partial product bits of the least significant cell are made available to the SUMmer and the SUM out terminals. The LSB input controls the SUM out providing a pass through or add dependent on polarity.

PROGRAMMING THE MULTIPLIER

The Am25LS2516 is an externally programmed device controlled by four instruction lines. This programmability provides a key to its flexibility. Sixteen microinstructions (see Table 1) are provided, which can be grouped into three major functions: Data Move, Read, and Multiply.

Instruction 0-3: The first instructions ("0", "1", "2", "3") load the "Y" Register from the Accumulator (high or low) and load the "X" Register while either clearing or not clearing, respectively, the Accumulator.

The next four instructions ("4", "5", "6", "7") load the "Y" Register from external "bus" and Holds on the accumulators and multiplier.

Instruction "7" is unique and is used to execute a chain multiply. It provides the last multiply operation while loading the "Y" Register, transferring the "X", and clearing the multiplier.

Instrucitons "8" and "9" provide the read-out (upper and lower halves) of the Accumulator.

Instructions "A" and "B" internally transfer the respective halves of the Accumulator to the "X" Register – another method of chain calculating.

Instruction "C" is used as an idling instruction after multiplication in order to hold the product in the accumulator until a read instruction can be performed. NOTE: The operations of the instruction are in some cases stored by clocking the instructions into an instruction register, accounting for a clocked delay in operations. Specifically, the shifting of the Accumulator is an internally stored command and as such is started and stopped one clock cycle late, allowing the Accumulator to complete its data shifting during the first HOLD A cycle following a multiply and starting it one clock cycle after the multiplying cycle is started.

Instruction "D" is a single iteration of the multiply and must be used for each bit in the multiplier minus one. The last bit of the multiplier will be handled by a HOLD A ("C") or a load Y and multiply (7).

Instruction "E" provides a load "X" Register and Hold.

Instruction "F" provides an intermediate instruction which can be executed during a multiply. It allows the "X" Register to load without disturbing the "X" Latch, while continuing the iteration of the multiply.

Instructions "C" and "7" also provide sampling and storage of the overflow condition.

TABLE I

MNEMONIC	INSTRUCTION $I_3I_2I_1I_0$ IN HEX	FUNCTION	REMARKS	
YLHC	0	LHA→Y, XFER X, CLR A CLR M, READ OVFL		
YUHC	1	UHA→Y, XFER X, CLR A CLR M, READ OVFL		
YLHA	2	LHA→Y, XFER X CLR M, READ OVFL		
YUHA	3	UHA→Y, XFER X CLR M, READ OVFL		
LYCA	4	LOAD Y, XFER X, CLR A CLR M	Same function as 5	
LYCA	5	CLR A LOAD Y, XFER X, CLR M	Same function as 4	
LYHA	6	LOAD Y, XFER X, HOLD A CLR M		
LYSA	7	LOAD Y, XFER X, SHIFT A CLR M, MULTIPLY	Enables overflow store in next state	*
RLHA	8	READ LHA READ OVFL		
RUHA	9	READ UHA READ OVFL		
XLHA	A	LHA→X READ OVFL		
XUHA	B	UHA→Y READ OVFL		
HLDA	C	HOLD A	Enable overflow store	
MULT	D	MULTIPLY SHIFT A		*
LXHA	E	LOAD X, HOLD A		
LXSA	F	LOAD X, SHIFT A MULTIPLY		*

*Continue multiplying instructions.

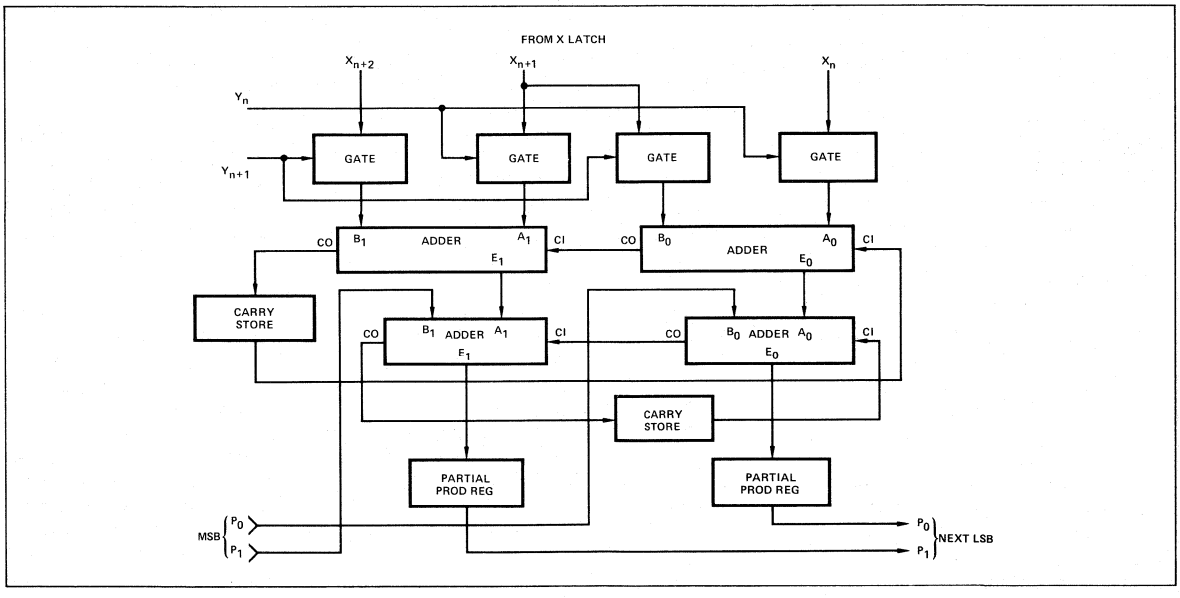
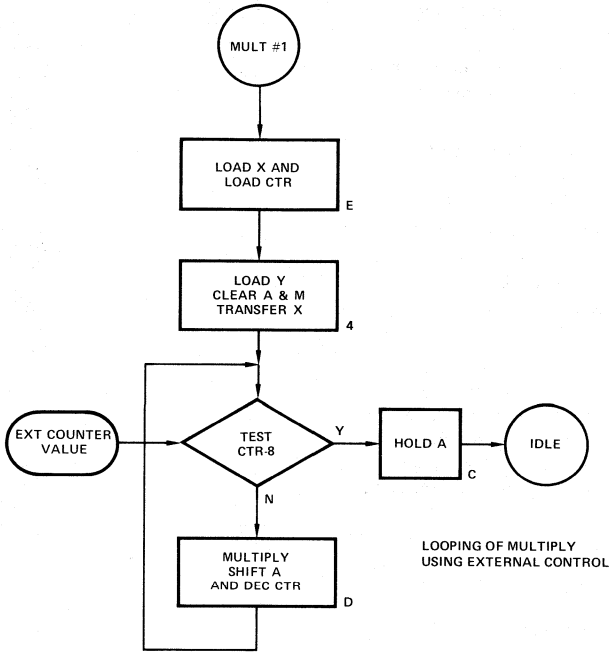


Figure 2. Am25LS2516 Multiplier Cell.

APPLICATION OF THE MULTIPLIER

The flow diagram for an 8-bit two's complement multiply is shown in Figure 3, together with the required program micro-steps. Figure 4 extends this to include accumulate, intermediate load of X and chain calculations. Figures 5a and b show the external connection of two Am25LS2516 devices to execute a 16-bit by 16-bit multiplication. A 32-bit product is completed in 16 clock cycles. This same technique may be extended in a similar fashion to longer word lengths. The flowchart of Figure 6 demonstrates a 16-bit two's complement multiply without accumulate, modified to a 12-bit by 12-bit function.

The Am25LS2516 Multiplier/Accumulator is the most complex LSI product manufactured to date with Low-Power Schottky technology. It will be extremely useful in high-density applications where minimum package count is a primary consideration. The device itself performs an 8 x 8 or 16 x 16 multiplication in approximately twice the time of parallel multipliers currently available, but using only one quarter the power in the multiplier portion of the function. In a fully configured system using both techniques, the Am25LS2516 performance begins to approach that of the parallel multiplier plus supporting devices.



PROGRAM MICRO STEPS

#	INST IN HEX
1	E
2	4
3	D
4	D
5	D
6	D
7	D
8	D
9	D
10	D
11	C
	IDLE

Figure 3. 8-Bit Two's Complement Multiply without Accumulate or Chain.

PROGRAM MICRO STEPS

#	INST IN HEX
1	E
2	4
3	D
4	D
5	D
6	F
7	D
8	D
9	D
10	7
11	D
12	D
13	D
14	D
15	D
16	D
17	D
18	D
19	C
20	C IDLE
21	C
IDLE	

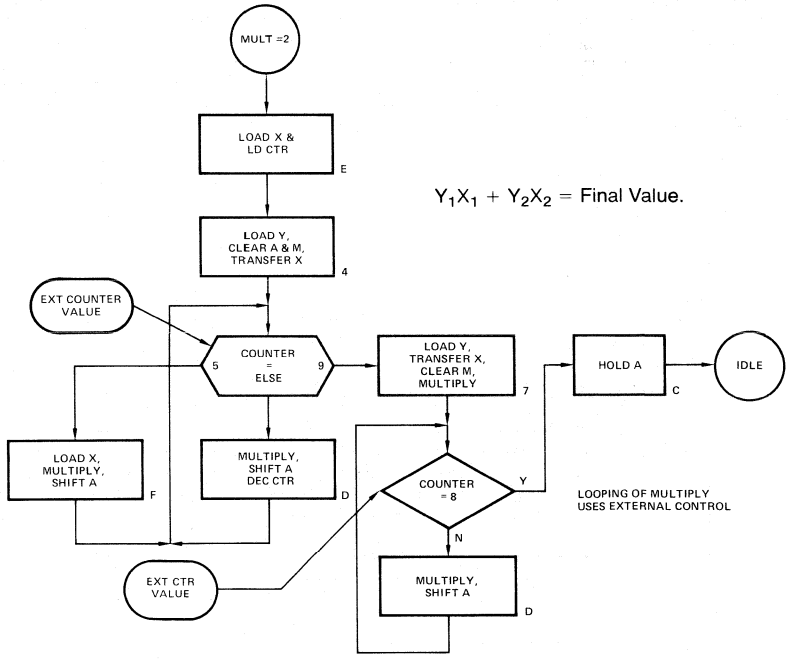


Figure 4. 8-Bit Two's Complement Multiply with Accumulate, Intermediate Load and Chain Calculations.

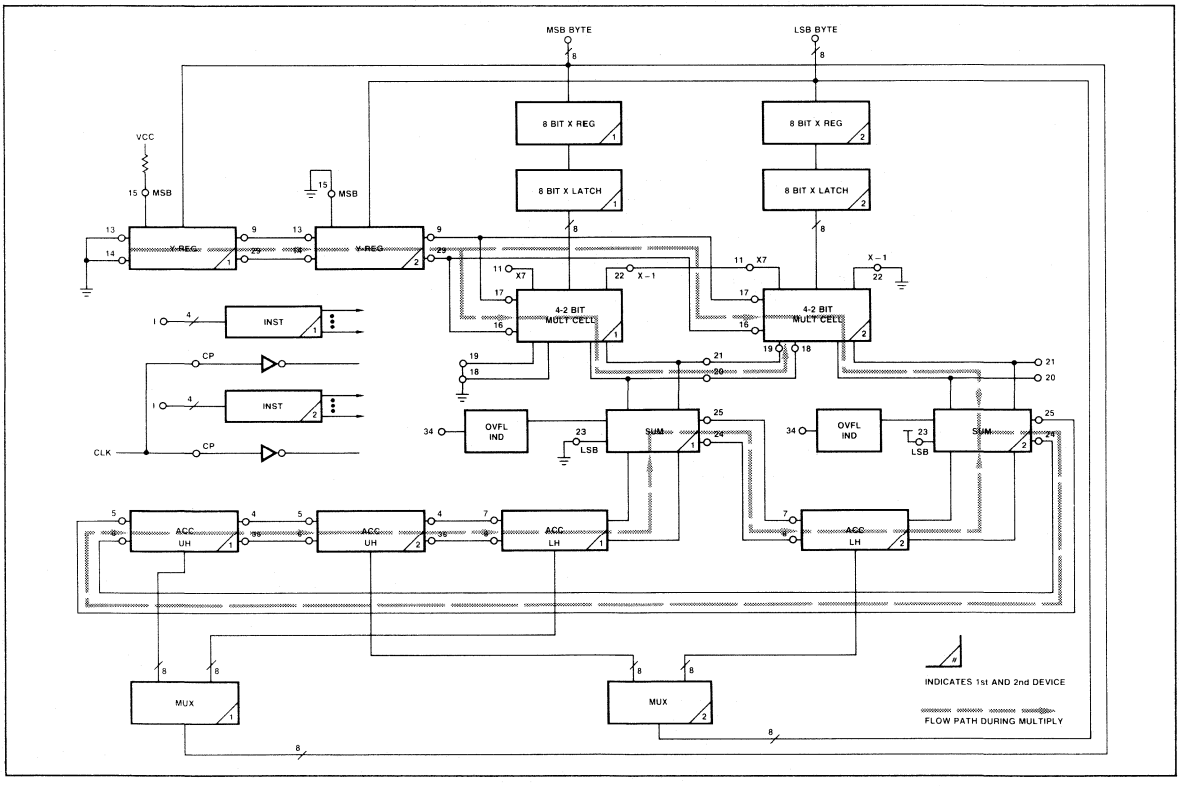


Figure 5a. Interconnection of Two Am25LS2516 (8 x 8 Multiplier) Devices to Execute a 16 x 16 Multiply.

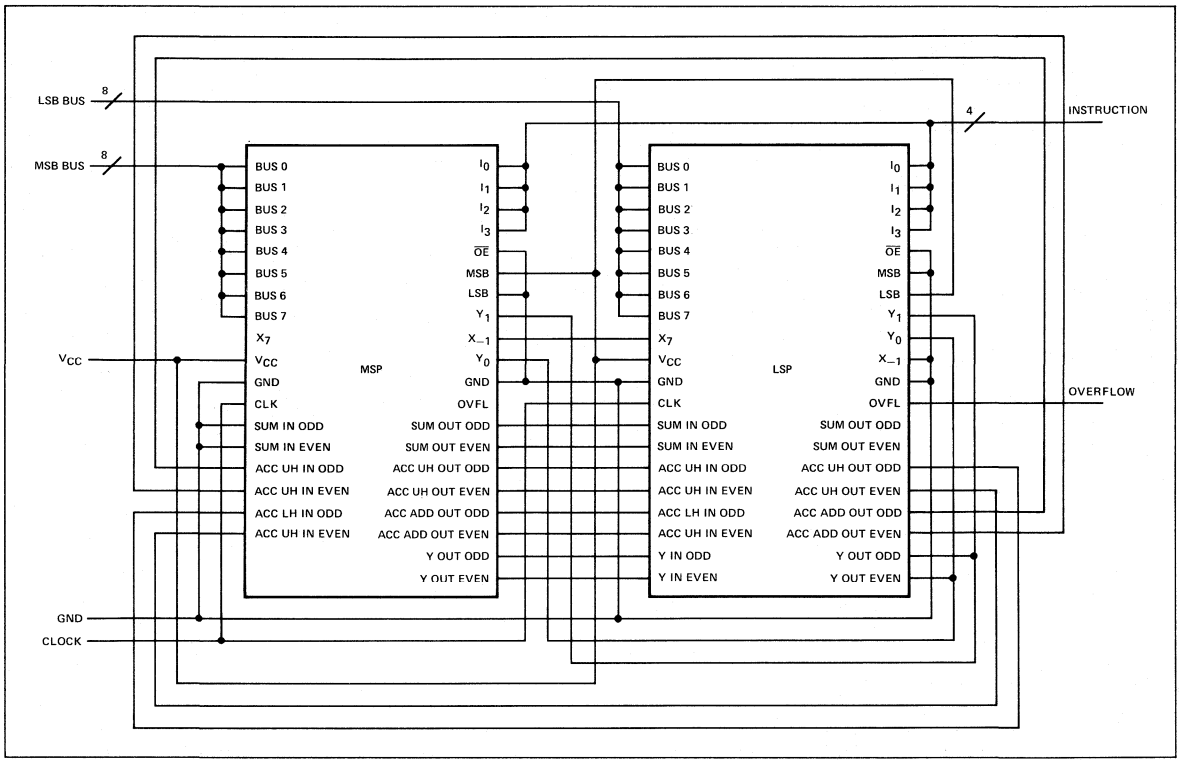


Figure 5b. Two Devices Cascaded in 16-Bit by 16-Bit Multiplier Application with 32-Bit Accumulated Product.

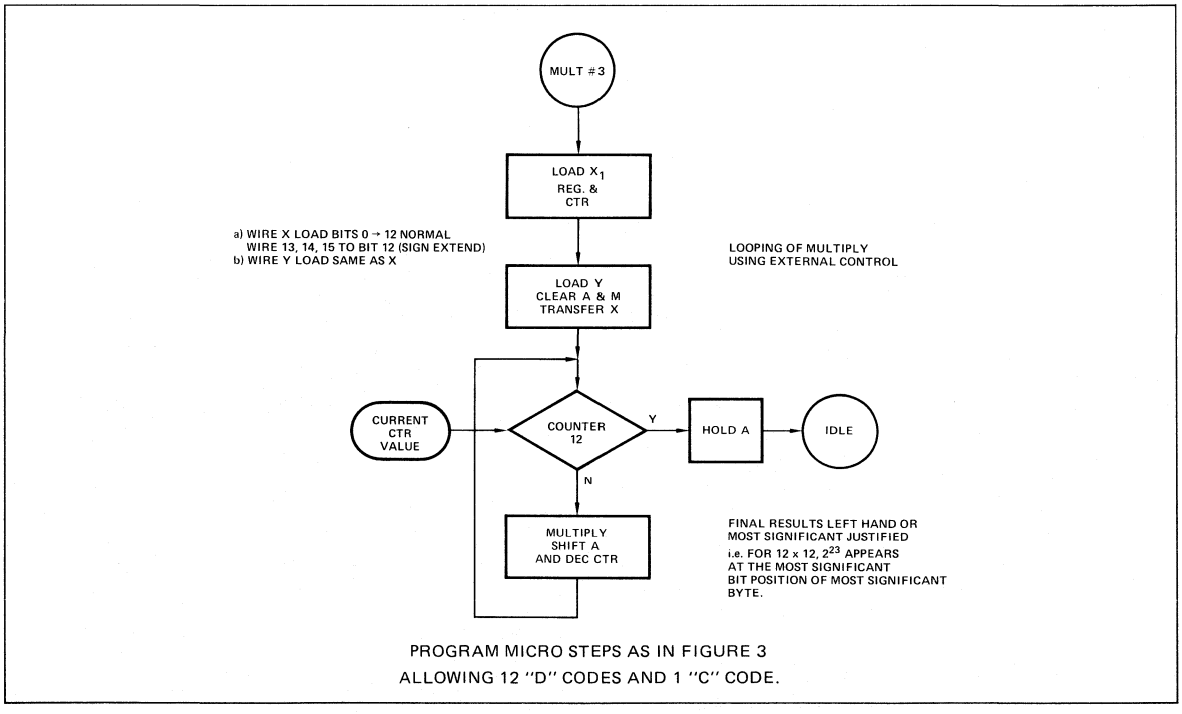


Figure 6. 16 Bit Two's Complement Multiply without Accumulate Modified to 12 x 12 (Using Two Am25LS2516 Devices Interconnected).

Am25LS2518

Quad D Register With Standard And Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Low-power Schottky version of the popular Am2918 and Am25S18
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops
- Second sourced by T. I. as the SN54/74LS388
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am25LS2518 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

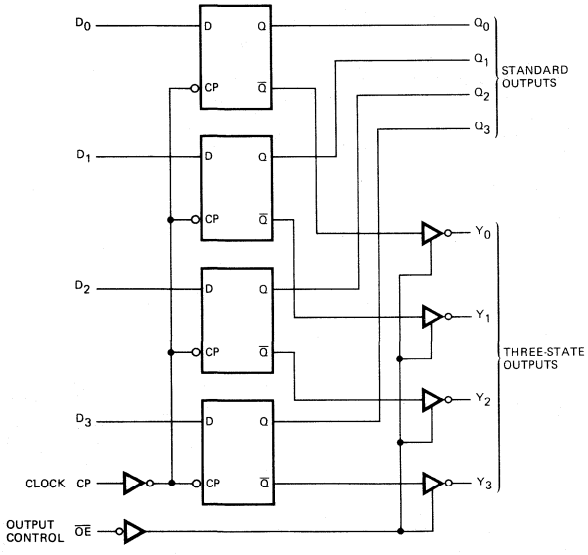
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25LS2518 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

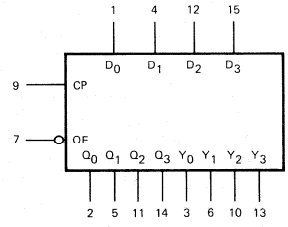
The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25LS2518 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

LOGIC DIAGRAM

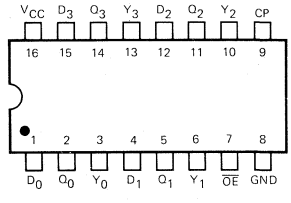


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q, $I_{OH} = -660\mu A$	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	MIL, $I_{OH} = -1.0mA$	2.4	3.4		
				COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				17	28	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

Am25LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				18	27		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	
t_{PHL}				18	27		
t_{pw}	Clock Pulse Width	LOW	18			ns	
		HIGH	15				
t_s	Data		15			ns	
t_h	Data		5.0			ns	
t_{ZH}	$\overline{OE}$ to Y_i			7.0	11	ns	
t_{ZL}				8	12		
t_{HZ}	$\overline{OE}$ to Y_i			14	21	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				12	18		
f_{max}	Maximum Clock Frequency (Note 1)		35	50		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i			38		45	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				38		45		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			35		40	ns	
t_{PHL}				35		40		
t_{pw}	Clock Pulse Width	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		5.0		5.0		ns	
t_{ZH}	$\overline{OE}$ to Y_i			15		17	ns	
t_{ZL}				16		17		
t_{HZ}	$\overline{OE}$ to Y_i			27		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24		30		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

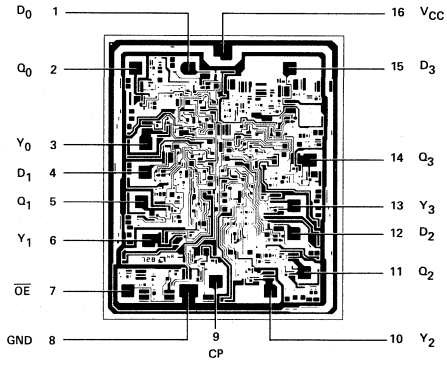
INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

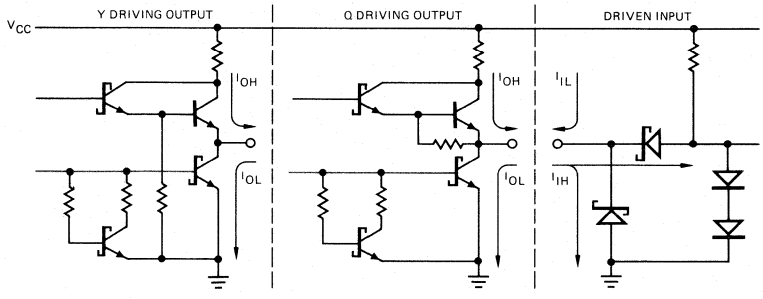
Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

Metallization and Pad Layout



DIE SIZE 0.083" X 0.099"

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS

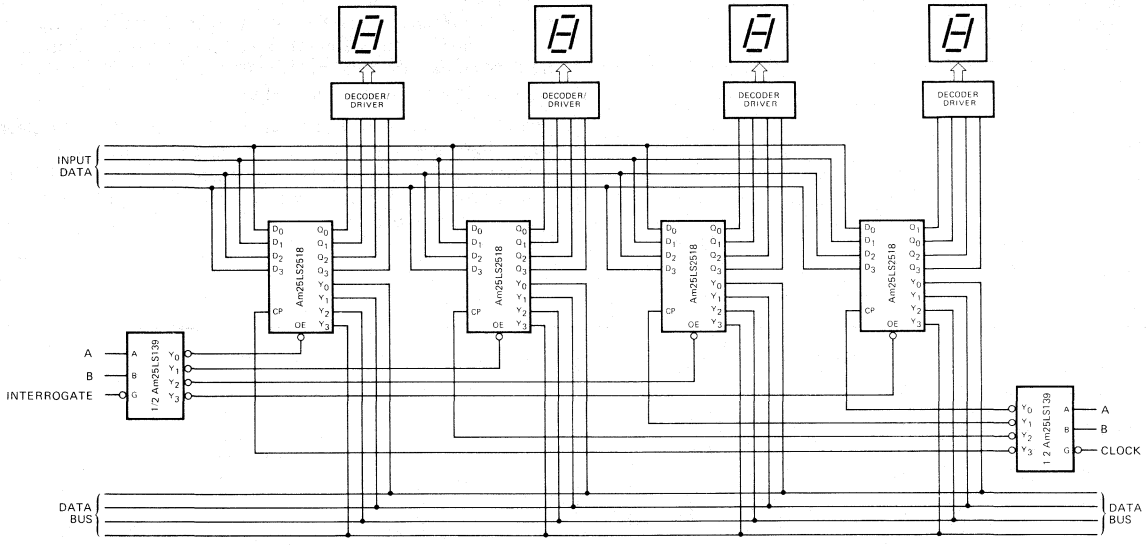


Note: Actual current flow direction shown.

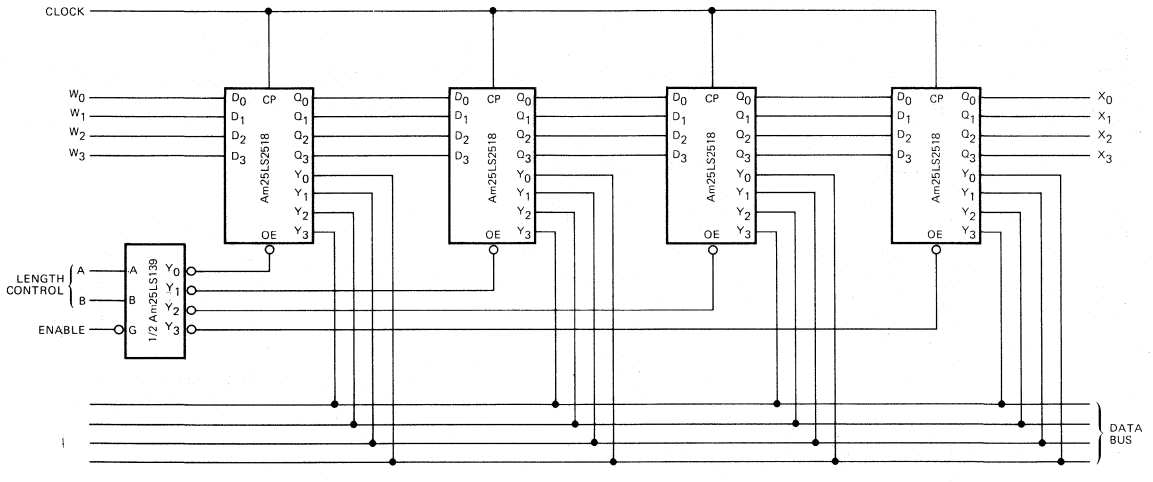
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS2518PC
Hermetic DIP	0°C to +70°C	AM25LS2518DC
Dice	0°C to +70°C	AM25LS2518XC
Hermetic DIP	-55°C to +125°C	AM25LS2518DM
Hermetic Flat Pak	-55°C to +125°C	AM25LS2518FM
Dice	-55°C to +125°C	AM25LS2518XM

APPLICATIONS



The Am25LS2518 used as display register with bus interrogate capability.



The Am25LS2518 as a variable length (1, 2, 3 or 4 word)shift register.

Am25LS2519

Quad Register With Two Independently Controlled Three-State Outputs

DISTINCTIVE CHARACTERISTICS

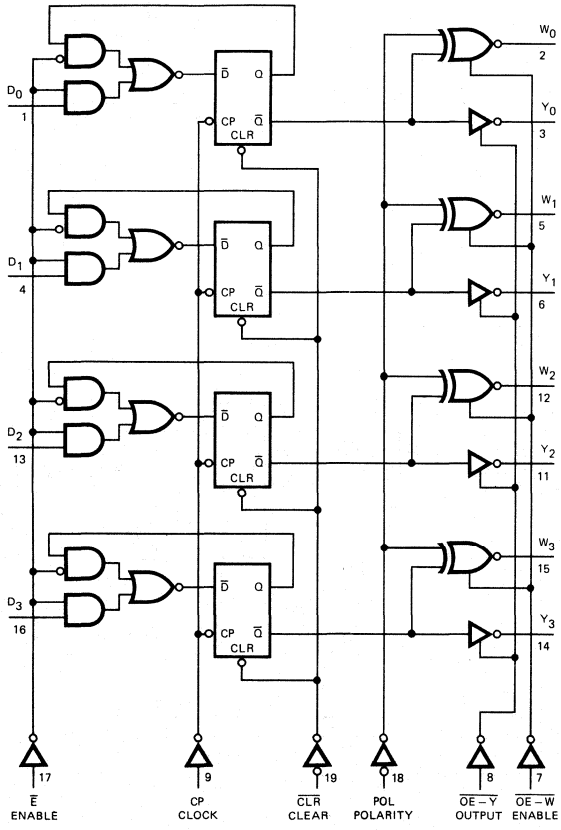
- Two sets of fully buffered three-state outputs
- Four D-type flip-flops
- Polarity control on W outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

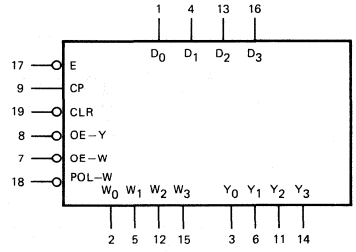
The Am25LS2519 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs – W and Y – are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am25LS2519 is packaged in a space saving (0.3-inch row spacing) 20-pin package.

LOGIC DIAGRAM

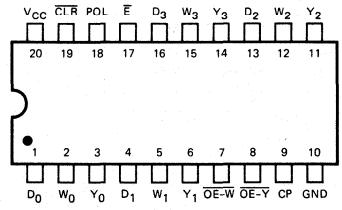


LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

m25LS2519

LECTRICAL CHARACTERISTICS

ıe Following Conditions Apply Unless Otherwise Specified:

OM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
IL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

C CHARACTERISTICS OVER OPERATING RANGE

ırameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	µA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	µA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.		MIL		24	36	mA
				COM'L		24	39	

ıtes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

m25LS

AXIMUM RATINGS (Above which the useful life may be impaired)

orage Temperature	−65°C to +150°C
ımperature (Ambient) Under Bias	−55°C to +125°C
ıpply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
C Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
C Input Voltage	−0.5 V to +7.0 V
C Output Current, Into Outputs	30 mA
C Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PHL}	Clock to Y_i			22	33	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				20	30		
t_{PLH}	Clock to W_i (Either Polarity)			24	36	ns	
t_{PHL}				24	36		
t_{PHL}	Clear to Y_i			29	43	ns	
t_{PLH}	Clear to W_i			25	37	ns	
t_{PHL}				30	45		
t_{PLH}	Polarity to W_i			23	34	ns	
t_{PHL}				25	37		
t_{pw}	Clear		18			ns	
t_{pw}	Clock Pulse Width	LOW	15			ns	
		HIGH	18				
t_s	Data		15			ns	
t_h	Data		5			ns	
t_s	Data Enable		20			ns	
t_h	Data Enable		0			ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		20	15		ns	
t_{ZH}	Output Enable to W or Y			11	17	ns	
t_{ZL}				13	20		
t_{HZ}	Output Enable to W or Y			13	20	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				11	17		
f_{max}	Maximum Clock Frequency (Note 1)		35	45		MHz	C_L = 15pF, R_L = 2.0kΩ

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i			39		42	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				39		45		
t_{PLH}	Clock to W_i (Either Polarity)			41		43	ns	
t_{PHL}				44		48		
t_{PHL}	Clear to Y_i			52		58	ns	
t_{PLH}	Clear to W_i			42		43	ns	
t_{PHL}				51		53		
t_{PLH}	Polarity to W_i			41		45	ns	
t_{PHL}				42		44		
t_{pw}	Clear		20		20		ns	
t_{pw}	Clock	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		10		10		ns	
t_s	Data Enable		25		25		ns	
t_h	Data Enable		0		0		ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		23		24		ns	
t_{ZH}	Output Enable to W_i or Y_i			24		27	ns	
t_{ZL}				29		35		
t_{HZ}	Output Enable to W_i or Y_i			33		45	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				22		26		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	C_L = 50pF, R_L = 2.0kΩ

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLE

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE}$-W	$\overline{OE}$-Y	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L = LOW
H = HIGH
Z = High Impedance

X = Don't Care
NC = No Change
↑ = LOW to HIGH Transition

DEFINITION OF FUNCTIONAL TERMS

D_i — Any of the four D flip-flop data lines.

$\overline{E}$ — Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.

CP — Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.

$\overline{OE}$-W, $\overline{OE}$-Y — Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE}$-W controls the W set of outputs, and $\overline{OE}$-Y controls the Y set.

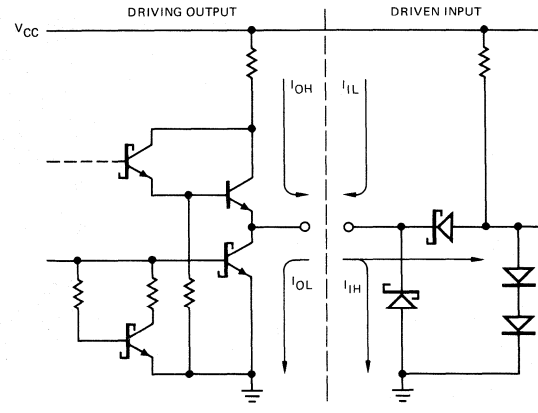
Y_i — Any of the four non-inverting three-state output lines.

W_i — Any of the four three-state outputs with polarity control.

POL — Polarity Control. The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.

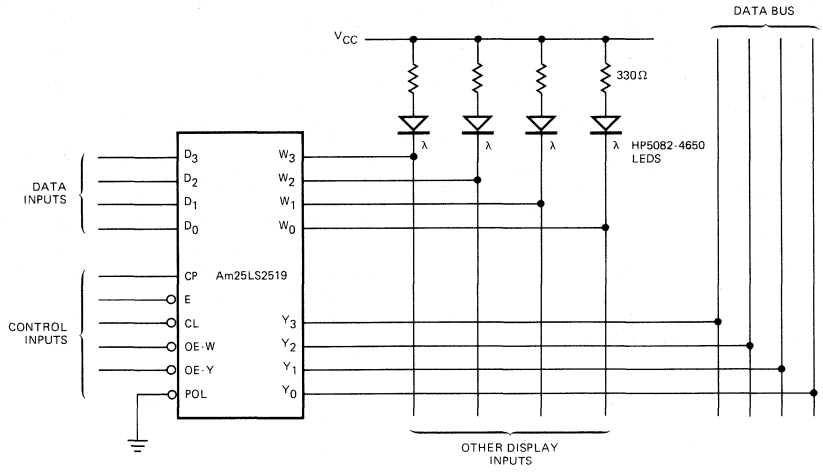
$\overline{CLR}$ — Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



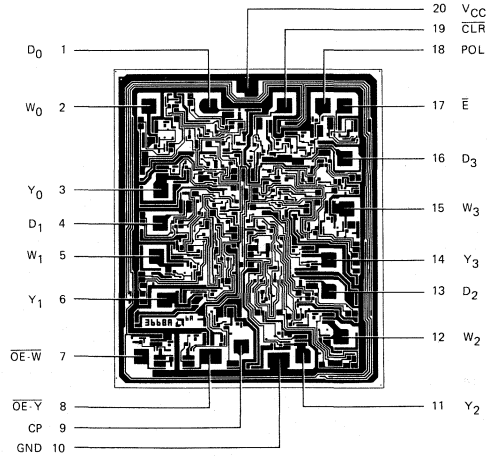
Note: Actual current flow direction shown.

APPLICATION



Convenient Register Content Monitor or Test Point

Metallization and Pad Layout



DIE SIZE 0.083" X 0.099"

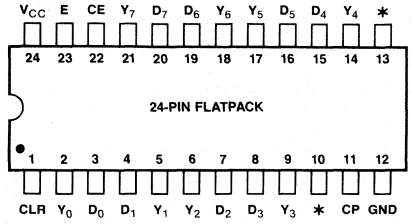
Am25LS2520

Octal D-Type Flip-Flop With Clear, Clock Enable And Three-State Control

DISTINCTIVE CHARACTERISTICS

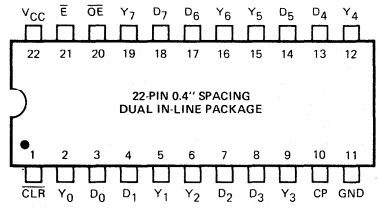
- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops
- Am25LS Family offers improved sink current, source current and noise margin
- 100% product assurance screening to MIL-STD-883 requirements

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation. *Reserved – do not use.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

FUNCTIONAL DESCRIPTION

The Am25LS2520 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

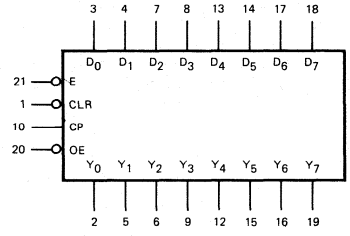
When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

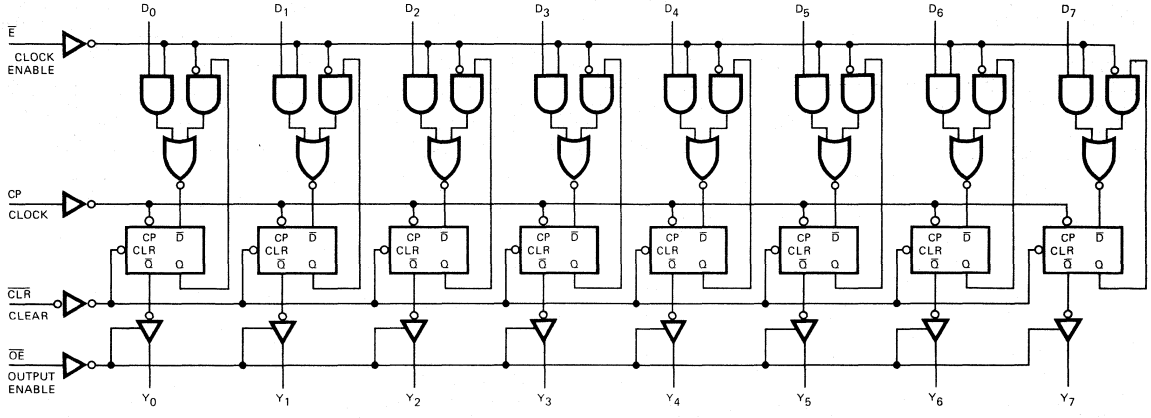
This device is packaged in a space-saving (0.4-inch row spacing) 22-pin package and in a 24-pin flatpack.

LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			24	37	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

Am25LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				24	36		
t_{PHL}	Clear to Y			22	35	ns	
t_s	Data (D_i)		10	3		ns	
t_h	Data (D_i)		10	3		ns	
t_s	Enable ($\overline{E}$)	Active	15	10		ns	
		Inactive	20	12			
t_h	Enable ($\overline{E}$)		0	0		ns	
t_s	Clear Recovery (In-Active) to Clock		11	7		ns	
t_{pw}	Clock	HIGH	20	14		ns	
		LOW	25	13			
t_{pw}	Clear		20	13		ns	
t_{ZH}	$\overline{OE}$ to Y_i			9	13	ns	
t_{ZL}				14	21		
t_{HZ}	$\overline{OE}$ to Y_i			20	30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24	36		
f_{max}	Maximum Clock Frequency (Note 1)			40		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			33		39	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				45		54		
t_{PHL}	Clear to Y			43		51	ns	
t_s	Data (D_i)		12		15		ns	
t_h	Data (D_i)		12		15		ns	
t_s	Enable ($\overline{E}$)	Active	17		20		ns	
		Inactive	20		23			
t_h	Enable ($\overline{E}$)		0		0		ns	
t_s	Clear Recovery (In-Active) to Clock		13		15		ns	
t_{pw}	Clock	HIGH	25		30		ns	
		LOW	30		35			
t_{pw}	Clear		22		25		ns	
t_{ZH}	$\overline{OE}$ to Y_i			19		25	ns	
t_{ZL}				30		39		
t_{HZ}	$\overline{OE}$ to Y_i			35		40	ns	C_L = 5.0 pF, R_L = 2.0 kΩ
t_{LZ}				39		42		
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{CLR}$ When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.

CP Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i The register three-state outputs.

$\overline{E}$ Clock Enable, When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

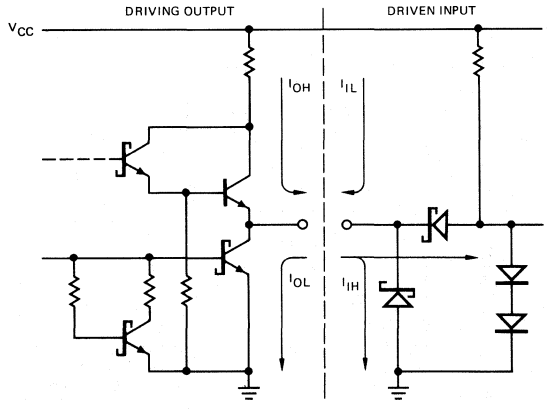
FUNCTION TABLE

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

H = HIGH
L = LOW
X = Don't Care

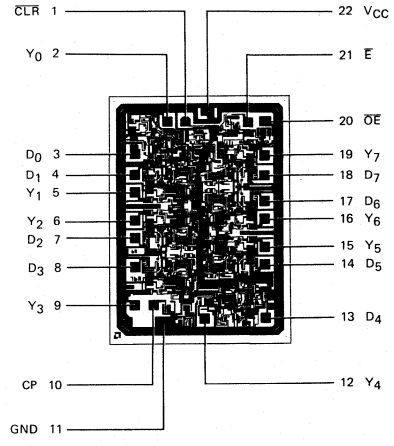
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

Am25LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Metallization and Pad Layout

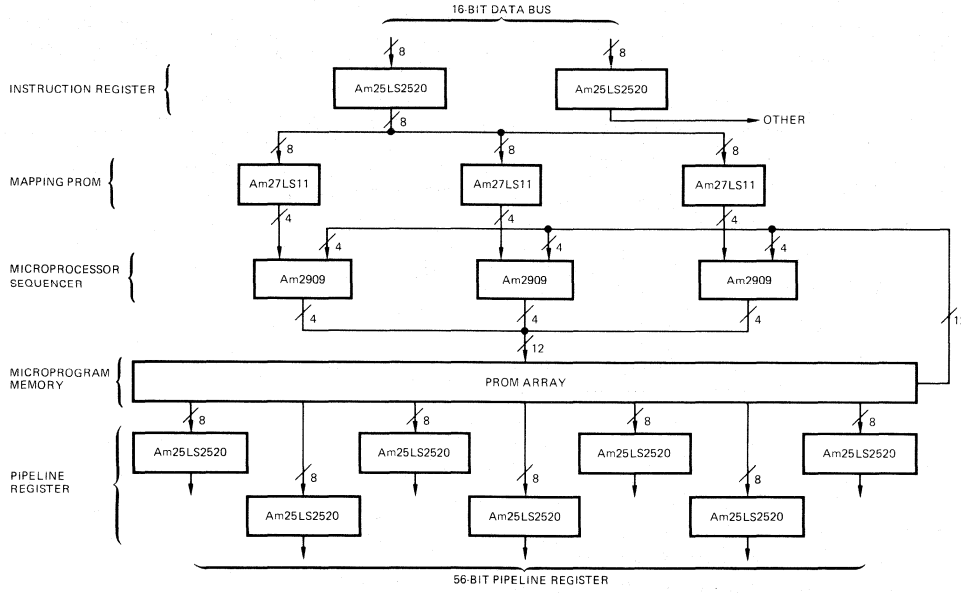


DIE SIZE 0.080" x 0.111"

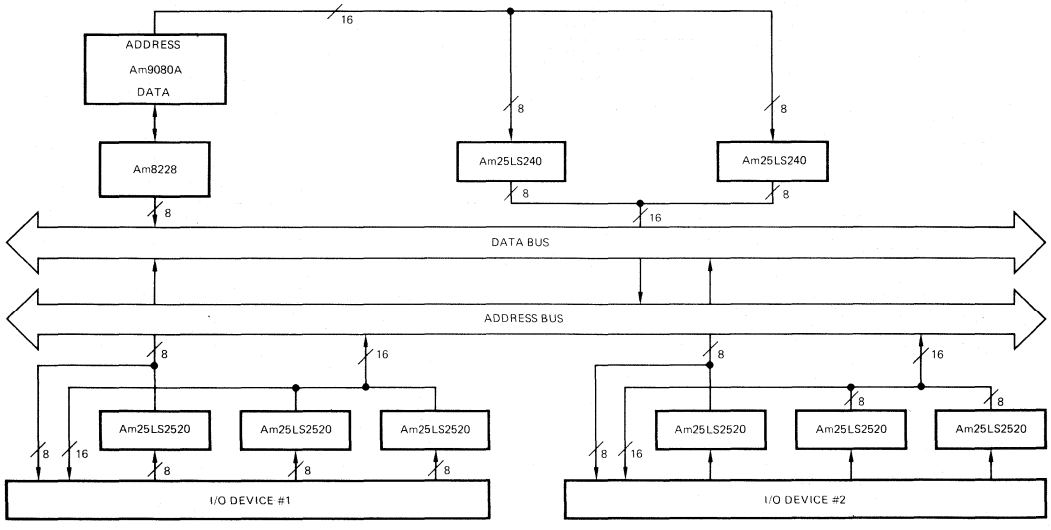
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS2520PC
Hermetic DIP	0°C to +70°C	AM25LS2520DC
Dice	0°C to +70°C	AM25LS2520XC
Hermetic DIP	−55°C to +125°C	AM25LS2520DM
Hermetic Flat Pak	−55°C to +125°C	AM25LS2520FM
Dice	−55°C to +125°C	AM25LS2520XM

APPLICATIONS



A typical Computer Control Unit for a microprogrammed machine.



The Am25LS2520 is a useful device in interfacing with the Am9080A system buses.

Am25LS2521

Eight-Bit Equal-To Comparator

DISTINCTIVE CHARACTERISTICS

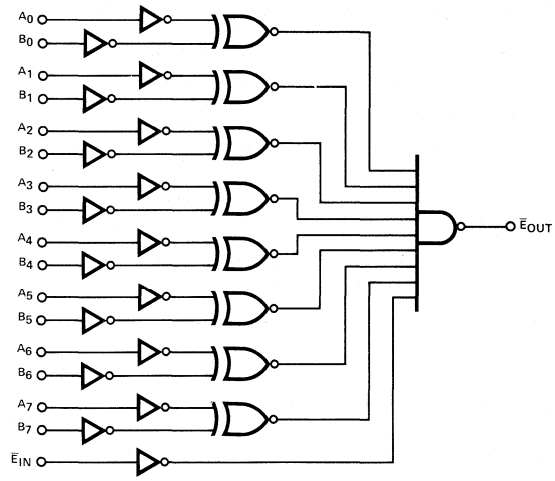
- 8-bit byte oriented equal comparator
- Cascadable using $\overline{E}_{IN}$
- High-speed, Low-Power Schottky technology
- t_{pd} A • B to $\overline{E}_{OUT}$ in 9ns
- Standard 20-pin package
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

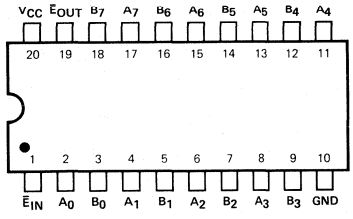
The Am25LS2521 is an 8-bit "equal to" comparator capable of comparing two 8-bit words for "equal to" with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the $\overline{E}_{IN}$ produces an active LOW on the output $\overline{E}_{OUT}$.

The logic expression for the device can be expressed as: $\overline{E}_{OUT} = \overline{(A_0 \odot B_0)\ (A_1 \odot B_1)\ (A_2 \odot B_2)\ (A_3 \odot B_3)\ (A_4 \odot B_4)\ (A_5 \odot B_5)\ (A_7 \odot B_7)\ E_{IN}}$. It is obvious that the expression is valid where $A_0 - A_7$ and $B_0 - B_7$ are expressed as either assertions or negations. This is also true for pair of terms i.e. A_0 can be compared with B_0 at the same time $\overline{A}_1$ is compared with $\overline{B}_1$. It is only essential that the polarity of the paired terms be maintained.

LOGIC DIAGRAM

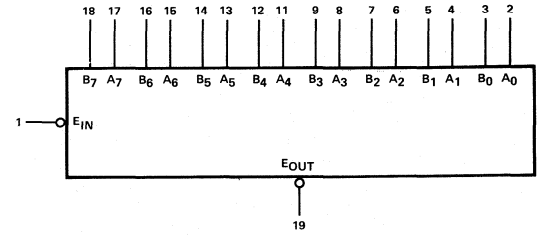


CONNECTION DIAGRAM



Note: Pin 1 is marked for orientation

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}, $I_{OH} = -440\mu A$	MIL	2.5			Volts
			COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	A_i, B_i			−0.36	mA
			$\overline{E}$			−0.72	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	A_i, B_i			20	μA
			$\overline{E}$			40	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$	A_i, B_i			0.1	mA
			$\overline{E}$			0.2	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			27	40	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{E}$ = GND, all other inputs and outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A_i or B_i to $\overline{Equal}$		9	15	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			9	15		
t_{PLH}	$\overline{E}$ to $\overline{Equal}$		5	7	ns	
t_{PHL}			6	8		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE *

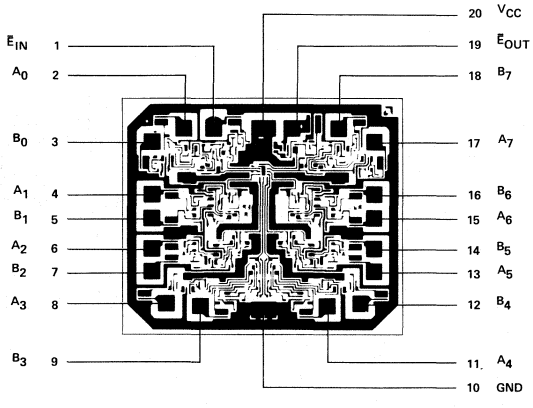
Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	A_i or B_i to		20		22	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}	$\overline{Equal}$ Output		19		21		
t_{PLH}	$\overline{E}$ to $\overline{Equal}$ Output		10.5		12	ns	
t_{PHL}			12.5		15		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

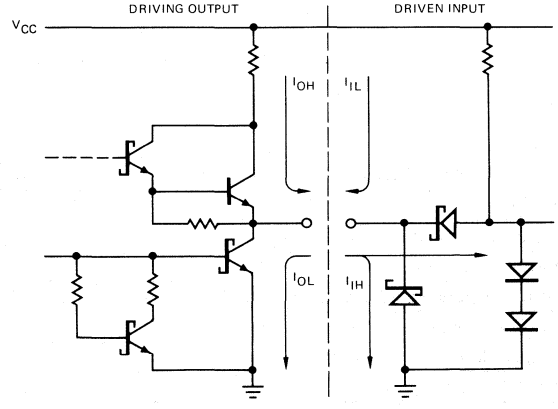
A_0–A_7	A input to comparator
B_0–B_7	B input to comparator
$\overline{E}_{IN}$	Enable active LOW
$\overline{E}_{OUT}$	$\overline{EQUAL}$ output active LOW

Metallization and Pad Layout



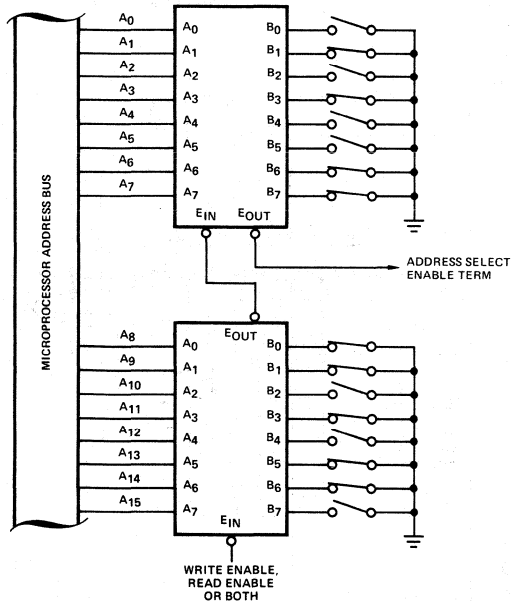
DIE SIZE 0.063" x 0.074"

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATION



MAX. $\overline{\text{ENABLE}}$ (HIGH-to-LOW) DELAY OVER 16-BITS
(Commercial Range)

t_{PHL}	A_i or B_i to $\overline{E}_{OUT}$	19ns
t_{PHL}	$\overline{E}_{IN}$ to $\overline{E}_{OUT}$	12.5ns
Total		31.5ns

MICROPROCESSOR ENABLE CONTROLLED, SELECTABLE, ADDRESS DECODER

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS2521PC
Hermetic DIP	0°C to +70°C	AM25LS2521DC
Dice	0°C to +70°C	AM25LS2521XC
Hermetic DIP	−55°C to +125°C	AM25LS2521DM
Hermetic Flat Pak	−55°C to +125°C	AM25LS2521FM
Dice	−55°C to +125°C	AM25LS2521XM

Am25LS2535

Eight Input Multiplexer With Control Register

DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Common register enable
- Asynchronous register clear
- Three-state output for expansion
- Am25LS features improved noise margin, higher drive, and faster operation
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am25LS2535 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

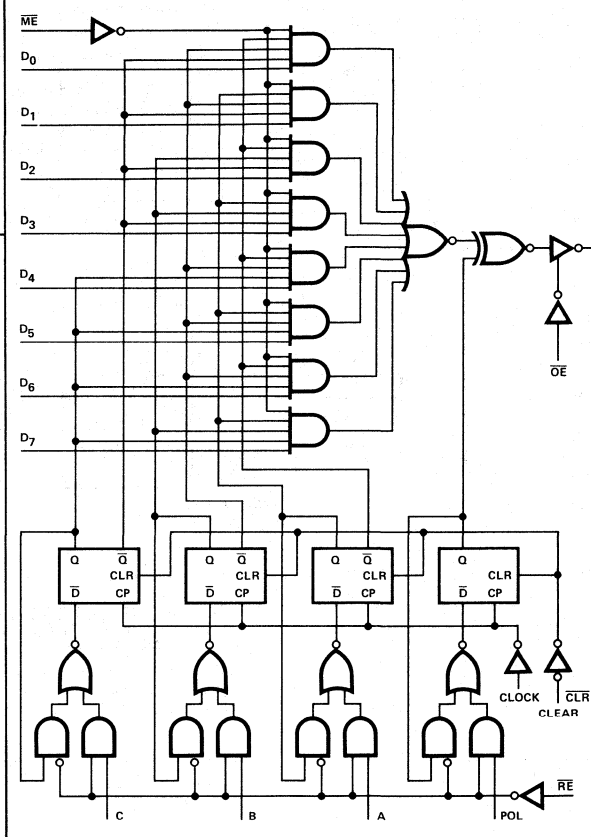
The Am25LS2535 contains an internal register which holds the A, B and C multiplexer select lines as well as the POL (polarity) control bit. When the Register Enable input ($\overline{RE}$) is LOW, new data is entered into the register on the LOW-to-HIGH, transition of the clock. When $\overline{RE}$ is HIGH, the register retains its current data. An asynchronous clear input ($\overline{CLR}$) is used to reset the register to a logic LOW level.

The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

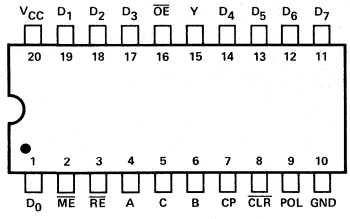
An active LOW Multiplexer Enable input ($\overline{ME}$) allows the selected multiplexer input to be passed to the output. When $\overline{ME}$ is HIGH, the output is determined only by the Polarity Control bit.

The Am25LS2535 also features a three-state Output Enable control ($\overline{OE}$) for expansion. When $\overline{OE}$ is LOW, the output is enabled. When $\overline{OE}$ is HIGH, the output is in the high impedance state.

LOGIC DIAGRAM

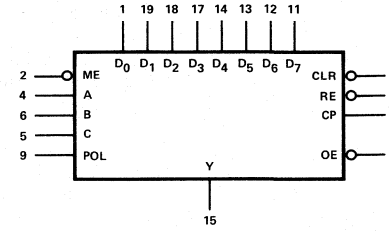


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -2.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -6.5mA$	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 20mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			−0.72	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			40	μA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			50	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			0.1	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			1.0	
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−50	μA
			$V_O = 2.4V$			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			97	148	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $D_1 - D_7$, A, B, C, POL, $\overline{ME}$, CLR at GND. All other inputs and outputs open.
Measured after a momentary ground then 4.5 V applied to clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y POL – LOW		21	32	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			19	29		
t_{PLH}	Clock to Y POL – HIGH		16	24	ns	
t_{PHL}			19	29		
t_{PLH}	D_n to Y		10	16	ns	
t_{PHL}			13	19		
t_{PLH}	$\overline{CLR}$ to Y		22	33	ns	
t_{PHL}			22	33		
t_{PLH}	$\overline{ME}$ to Y		12	18	ns	
t_{PHL}			12	18		
t_{ZL}	$\overline{OE}$ to Y		8	14	ns	
t_{ZH}			8	14		
t_{LZ}			10	17	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			10	17		
t_s	A, B, C, POL	10			ns	C_L = 15pF, R_L = 2.0kΩ
	$\overline{RE}$	15				
t_s	$\overline{CLR}$ Recovery	5			ns	
t_{pw}	Clock	10			ns	
	$\overline{Clear}$ (LOW)	10				
t_h	A, B, C, POL, $\overline{RE}$	0			ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Y, POL-L		40		47	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			34		38		
t_{PLH}	Clock to Y, POL-H		29		33	ns	
t_{PHL}			35		41		
t_{PLH}	D_N to Y		19		21	ns	
t_{PHL}			22		24		
t_{PLH}	$\overline{CLR}$ to Y		39		45	ns	
t_{PHL}			39		45		
t_{PLH}	$\overline{ME}$ to Y		22		26	ns	
t_{PHL}			19		20		
t_{ZL}	$\overline{OE}$ to Y		19		24	ns	
t_{ZH}			22		29		
t_{LZ}	OE to Y		24		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			24		30		
t_s	A, B, C POL	11		12		ns	C_L = 50pF, R_L = 2.0kΩ
	$\overline{RE}$	18		20			
t_s	$\overline{CLR}$ Recovery	6		7		ns	
t_{pw}	Clock	11		12		ns	
	$\overline{Clear}$ (LOW)	11		12			
t_H	A, B, C, POL, $\overline{RE}$	3		3		ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLE

MODE	INPUTS							INTERNAL				INPUTS		OUTPUT
	C	B	A	POL	$\overline{RE}$	$\overline{CLR}$	CP	Q_C	Q_B	Q_A	Q_{POL}	$\overline{ME}$	$\overline{OE}$	Y
Clear	X	X	X	X	X	L	X	L	L	L	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	L	L	$\overline{D}_0$
												X	H	Z
Reg. Disable	X	X	X	X	H	H	X	NC	NC	NC	NC	L	L	D_i/D_i (Note 1)
Select (Multiplex)	L	L	L	L/H	L	H	↑	L	L	L	L/H	L	L	$\overline{D}_0/D_0$
	L	L	H	↓	↓	↓	↓	L	L	H	↓	↓	↓	$\overline{D}_1/D_1$
	L	H	L					L	H	L				$\overline{D}_2/D_2$
	L	H	H					L	H	H				$\overline{D}_3/D_3$
	H	L	L					H	L	L				$\overline{D}_4/D_4$
	H	L	H					H	L	H				$\overline{D}_5/D_5$
	H	H	L					H	H	L				$\overline{D}_6/D_6$
	H	H	H					H	H	H				$\overline{D}_7/D_7$
Multiplexer Disable	X	X	X	X	X	H	X	X	X	X	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	X	X	X	H	H	L	L
Tri-state Output Disable	↓	↓	↓	↓	↓	↓	↓	X	X	X	X	X	H	Z

NC = No Change
X = Don't Care

Note 1: The output will follow the selected input, D_i, or its complement depending on the state of the POL flip-flop.

DEFINITION OF FUNCTIONAL TERMS

A, B, C Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.

POL Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.

$\overline{ME}$ Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.

$\overline{RE}$ Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.

$\overline{CLR}$ Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.

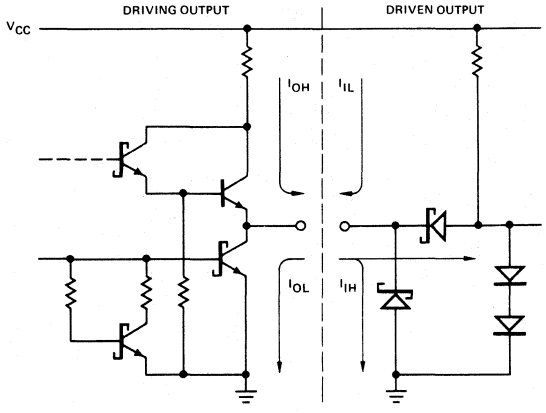
D_1-D_8 Data Inputs to the 8-input multiplexer.

CP Clock Pulse. When $\overline{RE}$ is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.

$\overline{OE}$ Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high impedance state.

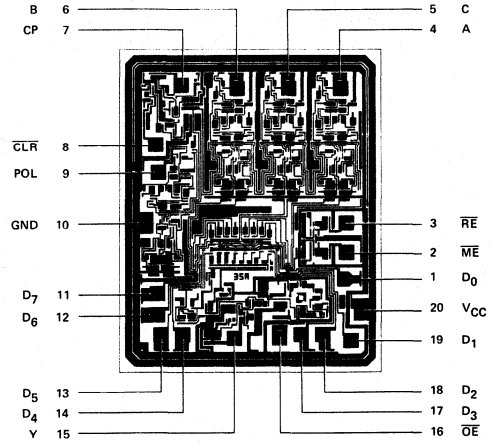
Y The chip output.

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



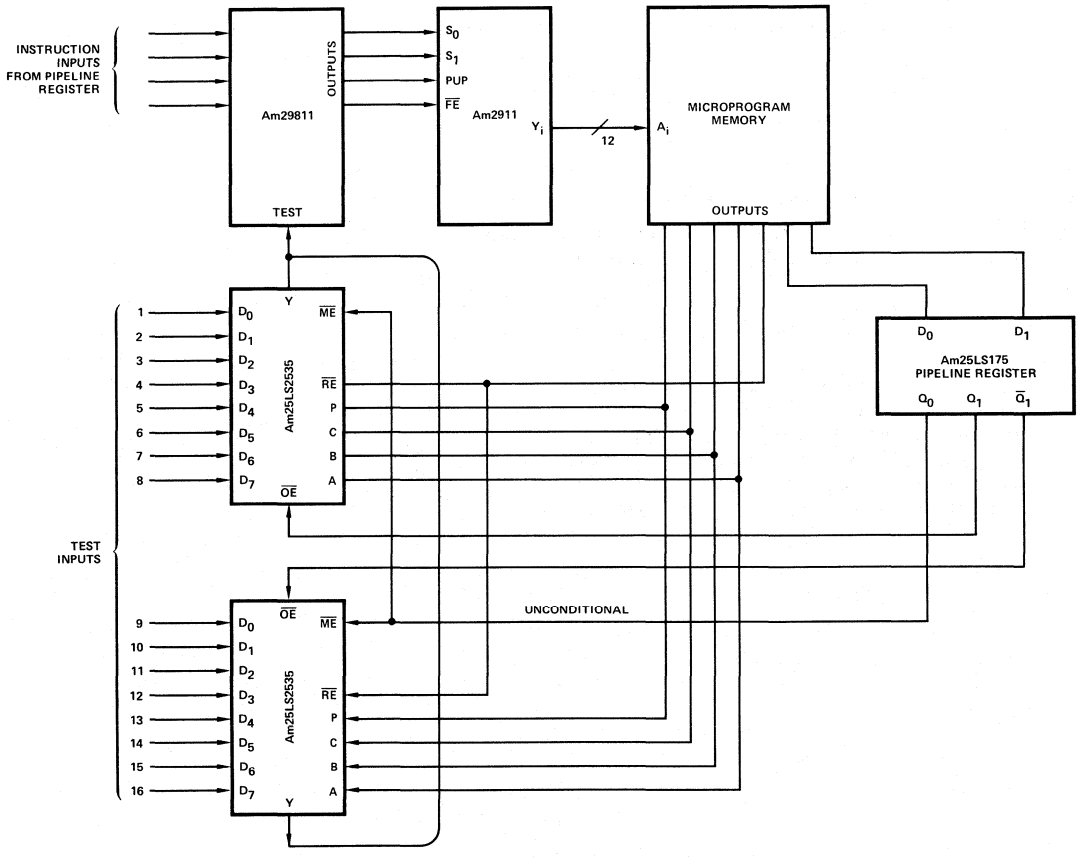
Note: Actual current flow direction shown.

Metallization and Pad Layout



DIE SIZE 0.080" X 0.099"

APPLICATION



A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

Am25LS2536

Eight-Bit Decoder With Control Storage

DISTINCTIVE CHARACTERISTICS

- 8-bit decoder/demultiplexer with control storage
- 3-state outputs
- Common clock enable
- Common clear
- Polarity control
- Advanced Low Power Schottky Process
- 100% product assurance screening to MIL-STD-883 requirements

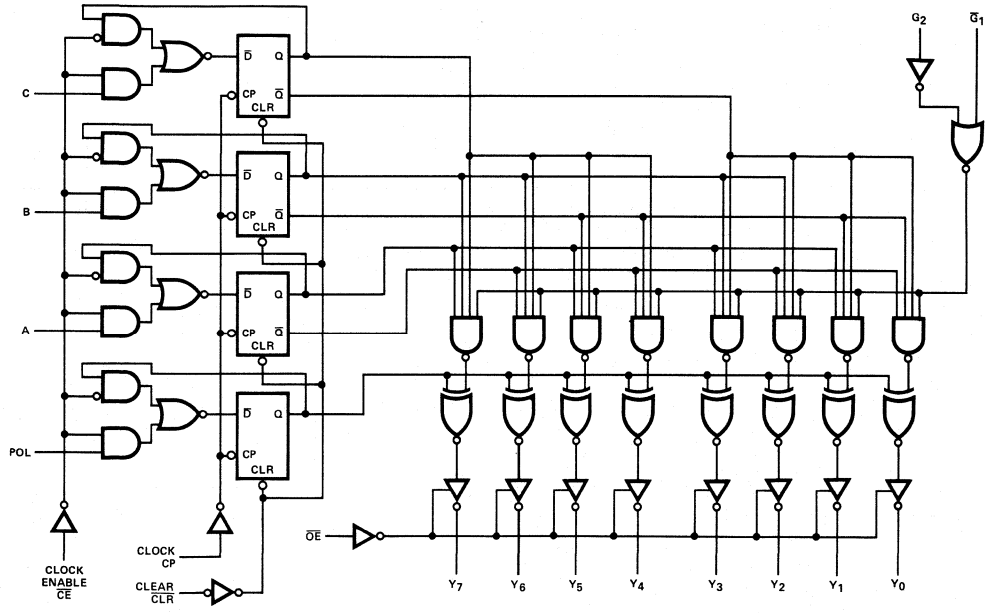
FUNCTIONAL DESCRIPTION

The Am25LS2536 is an eight-bit decoder with control storage. It provides a conventional 8-bit decoder function with two enable inputs which may also be used for data input. This can be used to implement a demultiplexer function. In addition, the exclusive "OR" gate allows for polarity control of the selected output. The 3-state outputs are enabled by a LOW on the ($\overline{OE}$) output enable.

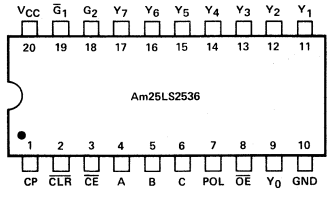
The three control bits representing the output selection and the single bit polarity control are stored in "D" type flip-flops. These flip-flops have both Clear, Clock, and Clock Enable functions provided. The $\overline{G_1}$ and G_2 input provide either polarity for input control or data.

LOGIC DIAGRAM

8-Bit Decoder/Demultiplexer with Control Storage

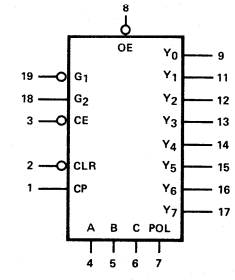


CONNECTION DIAGRAM



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = 20
GND = 10

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -2.6mA$, COM'L	2.4	3.2		Volts
			$I_{OH} = -1.0mA$, MIL	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 24mA$, COM'L		0.4	0.5	Volts
			$I_{OL} = 12mA$, MIL		0.35	0.4	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			37	56	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test Conditions: A = B = C = $\overline{G}_1$ = G_2 = $\overline{OE}$ = $\overline{CE}$ = GND; CLK = $\overline{CLR}$ = POL = 4.5 V.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	G_1 to $Y_0 - Y_7$			17	25	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}				23	34		
t_{PLH}	G_2 to $Y_0 - Y_7$			20	30	ns	
t_{PHL}				26	39		
t_{PLH}	CP to $Y_0 - Y_7$			24	36	ns	
t_{PHL}				30	45		
t_{PLH}	CLR to $Y_0 - Y_7$			24	36	ns	
t_{PHL}				31	46		
t_s	Clock Enable to CP		25			ns	
t_h			0				
t_s	A, B, C, POL to CP		15			ns	
t_h			0				
t_{HZ}	OE to $Y_0 - Y_7$			9	14	ns	C_L = 5pF, R_L = 667Ω
t_{LZ}				11	17		
t_{ZH}	OE to $Y_0 - Y_7$			15	22	ns	C_L = 45pF, R_L = 667Ω
t_{ZL}				16	24		
t_s	Set-up Time, Clear Recovery to CP		20			ns	
t_{pw}	Pulse Width	Clock	15			ns	
		Clear	15				

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	G_1 to $Y_0 - Y_7$			29		31	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}				39		42		
t_{PLH}	G_2 to $Y_0 - Y_7$			34		37	ns	
t_{PHL}				44		48		
t_{PLH}	CP to $Y_0 - Y_7$			40		42	ns	
t_{PHL}				51		55		
t_{PLH}	CLR to $Y_0 - Y_7$			47		54	ns	
t_{PHL}				58		66		
t_s	Clock Enable to CP		27		30		ns	
t_h			0		0			
t_s	A, B, C, POL to CP		17		20		ns	
t_h			0		0			
t_{HZ}	OE to $Y_0 - Y_7$			17		18	ns	C_L = 5.0pF, R_L = 667Ω
t_{LZ}				27		34		
t_{ZH}	OE to $Y_0 - Y_7$			25		27	ns	C_L = 5.0pF, R_L = 667Ω
t_{ZL}				28		30		
t_s	Set-up Time, Clear Recovery to CP		23		25		ns	
t_{pw}	Pulse Width	Clock	17		20		ns	
		Clear	15		15			

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLE

Mode	Inputs									Internal Registers				Three-State Outputs							
	C	B	A	POL	$\overline{CE}$	$\overline{CLR}$	G*	$\overline{OE}$	CP	Q_C	Q_B	Q_A	Q_{POL}	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
Clear	X	X	X	X	X	L	L	L	X	L	L	L	L	H	H	H	H	H	H	H	H
	X	X	X	X	X	L	H	L	X	L	L	L	L	L	H	H	H	H	H	H	H
Hold	X	X	X	X	H	H	NC	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
Select	L	L	L	H	L	H	H	L	↑	L	L	L	H	H	L	L	L	L	L	L	L
	L	L	H	H	L	H	H	L	↑	L	L	H	H	L	H	L	L	L	L	L	L
	L	H	L	H	L	H	H	L	↑	L	H	L	H	L	L	H	L	L	L	L	L
	L	H	H	H	L	H	H	L	↑	L	H	H	H	L	L	L	H	L	L	L	L
	H	L	L	H	L	H	H	L	↑	H	L	L	H	L	L	L	L	H	L	L	L
	H	L	H	H	L	H	H	L	↑	H	L	H	H	L	L	L	L	L	H	L	L
	H	H	L	H	L	H	H	L	↑	H	H	L	H	L	L	L	L	L	L	H	L
	H	H	H	H	L	H	H	L	↑	H	H	H	H	L	L	L	L	L	L	L	H
	L	L	L	L	L	H	H	L	↑	L	L	L	L	L	H	H	H	H	H	H	H
	L	L	H	L	L	H	H	L	↑	L	L	H	L	H	L	H	H	H	H	H	H
	L	H	L	L	L	H	H	L	↑	L	H	L	L	H	H	L	H	H	H	H	H
	L	H	H	L	L	H	H	L	↑	L	H	H	L	H	H	H	L	H	H	H	H
	H	L	L	L	L	H	H	L	↑	H	L	L	L	H	H	H	H	L	H	H	H
	H	L	H	L	L	H	H	L	↑	H	L	H	L	H	H	H	H	H	L	H	H
	H	H	L	L	L	H	H	L	↑	H	H	L	L	H	H	H	H	H	H	L	H
	H	H	H	L	L	H	H	L	↑	H	H	H	L	H	H	H	H	H	H	H	L
	X	X	X	H	L	H	L	L	↑	X	X	X	H	L	L	L	L	L	L	L	L
	X	X	X	L	L	H	L	L	↑	X	X	X	L	H	H	H	H	H	H	H	H
Output Disable	X	X	X	X	X	X	X	H	X	NC	NC	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z

*

$\overline{G_1}$	G_2	G
L	L	L
L	H	H
H	L	L
H	H	L

NC = No Change X = Don't Care Z = High-Impedance ↑ = Low-to-High Transition

DEFINITION OF TERMS

$\overline{CLR}$ CLEAR – When the CLEAR input is LOW, the control register outputs (Q_A, Q_B, Q_C, Q_{POL}) are set LOW regardless of any other inputs.

CP CLOCK – Enters data into the control register on the LOW-to-HIGH transition.

$\overline{CE}$ CLOCK ENABLE – Allows data to enter the control register when $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH, the Q_i outputs do not change state, regardless of data or clock input transitions.

A,B,C Inputs to the control register which are entered on the LOW-to-HIGH clock transition if $\overline{CE}$ is LOW.

POL Input to the control register bit used for determining the polarity of the selected output.

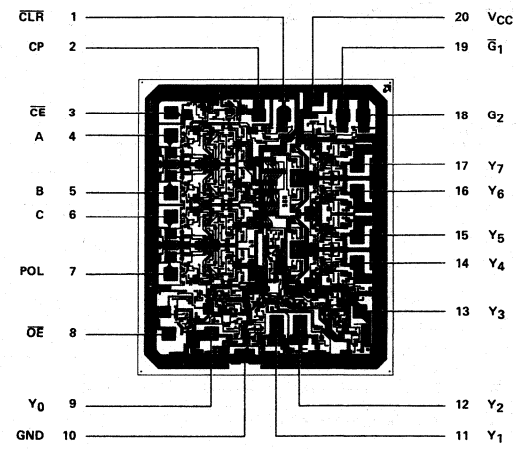
$\overline{G}_1$ Active LOW part of the expression $G = G_1G_2$ [or $G = (\overline{G_1})\,G_2$] where G is either data input for the selected Y_n or is used as an input enable.

G_2 Active HIGH part of the expression $G = G_1G_2$.

Y_n The three-state outputs. When active ($\overline{OE}$ = LOW), one of eight outputs is selected by the code stored in the control register, with the polarity of all eight determined by the bit stored in the POL flip-flop of the control register. The selected output can further be controlled by G according to the expression $Y_{SELECTED} = \overline{G \oplus Q_{POL}}$.

$\overline{OE}$ OUTPUT ENABLE. When $\overline{OE}$ is HIGH the Y_n outputs are in the high impedance state; when $\overline{OE}$ is LOW the Y_n's are in their active state as determined by the other control logic. The $\overline{OE}$ input affects the Y_n output buffers only and has no effect on the control register or any other logic.

Metallization and Pad Layout



DIE SIZE 0.084" X 0.099"

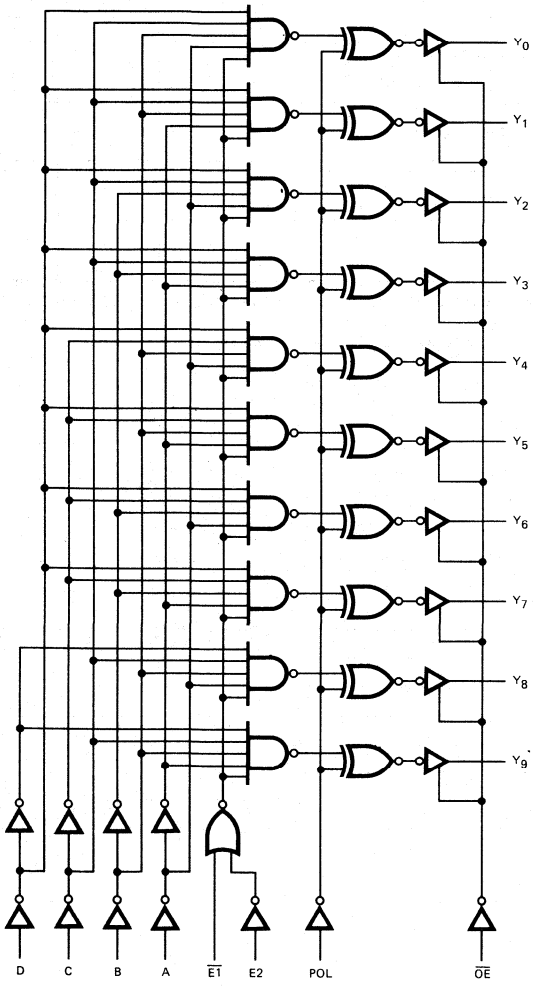
Am25LS2537

One-Of-Ten Decoder With Three-State Outputs And Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state outputs
- Separate output polarity control
- Inverting and non-inverting enable inputs
- Does not respond to codes above nine
- A.C. parameters specified over operating temperature and power supply ranges
- 100% product assurance screening to MIL-STD-883 requirements

LOGIC DIAGRAM



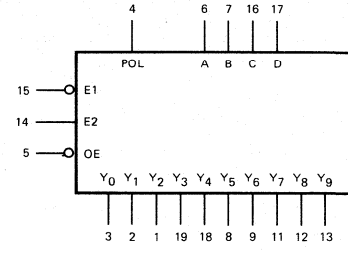
FUNCTIONAL DESCRIPTION

The Am25LS2537 is a demultiplexer/one-of-ten decoder that accepts four active high BCD inputs and selects one-of-ten mutually exclusive outputs. The device features three-state outputs as well as a buffered common polarity control such that the outputs are mutually exclusive active-low or mutually exclusive active-high. The logic design of the Am25LS2537 ensures that all outputs are unselected when the binary codes greater than nine are applied to the inputs. The inputs A, B, C, and D of the Am25LS2537 correspond to the respective binary weight of 1, 2, 4, and 8.

The output enable ($\overline{OE}$) input controls the three-state outputs. When the $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the outputs are enabled. The polarity (POL) input is used to drive the Y outputs to either the active-HIGH state or the active-LOW state. When the POL input is LOW, the outputs are active-HIGH. When the POL input is HIGH, the Y outputs are active-LOW. The device features one active-HIGH and one active-LOW enable input which can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

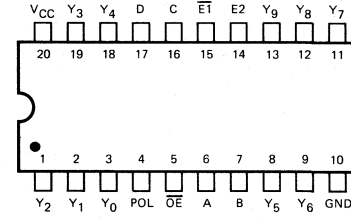
The Am25LS2537 is packaged in a space saving (0.3-inch row spacing) 20-pin package. The device also features Am25LS family faster switching specifications, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L = T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% MIN. = 4.75 V MAX. = 5.25 V
MIL = T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0 V				0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	V_O = 0.4 V			−20	µA
			V_O = 2.4 V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			25	40	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = D = E1 = GND; E2 = POL = $\overline{OE}$ = 4.5 V.
5. V_{OL} is specified with total device I_{OL} = 60mA (max.).

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B, C, D to Y_i		22	33	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	E_1 to Y_i		19	28	ns	
t_{PHL}			21	31		
t_{PLH}	$\overline{E_2}$ to Y_i		21	31	ns	
t_{PHL}			23	34		
t_{PLH}	POL to Y_i		18	27	ns	
t_{PHL}			21	31		
t_{ZH}	$\overline{OE}$ Control to Y_i		22	33	ns	
t_{ZL}			14	21		
t_{HZ}	$\overline{OE}$ Control to Y_i		19	28	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			23	34		

2

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{PLH}	A, B, C, D to Y_i		41		48	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			32		39		
t_{PLH}	E_1 to Y_i		34		40	ns	
t_{PHL}			38		45		
t_{PLH}	$\overline{E_2}$ to Y_i		38		45	ns	
t_{PHL}			42		49		
t_{PLH}	POL to Y_i		32		37	ns	
t_{PHL}			42		52		
t_{ZH}	$\overline{OE}$ Control to Y_i		44		55	ns	
t_{ZL}			23		25		
t_{HZ}	$\overline{OE}$ Control to Y_i		33		37	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			38		42		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLE

FUNCTION	INPUTS								OUTPUTS									
	$\overline{OE}$	$\overline{E_1}$	E_2	POL	D	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9
3-State	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	H	X	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	X	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H
	L	X	L	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	X	L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	L	H	L	H	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	L	L	H	L	L	H	L	L	L	L	L	L	H	L	L	L	L	L
	L	L	H	L	L	H	L	H	L	L	L	L	L	H	L	L	L	L
	L	L	H	L	L	H	H	L	L	L	L	L	L	L	H	L	L	L
	L	L	H	L	L	H	H	H	L	L	L	L	L	L	L	H	L	L
	L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L
	L	L	H	L	H	L	L	H	L	L	L	L	L	L	L	L	L	H
	L	L	H	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	H	H	L	L	L	L	L	L	L	L	L	L
Active-LOW Output	L	L	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	L	L	H	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
	L	L	H	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H
	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H
	L	L	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
	L	L	H	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H
	L	L	H	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H
	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H
	L	L	H	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
	L	L	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L
	L	L	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH
L = LOW

X = Don't Care
Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D To select inputs to the decoder.

E1 The active-LOW enable input. A HIGH on the E1 input inhibits the decoder function regardless of any other inputs.

$\overline{E2}$ The active-HIGH enable input. A LOW on the $\overline{E2}$ input forces all the decoder functions to the inactive state regardless of any other inputs.

POL The polarity control for the output function. When the polarity control is HIGH, the outputs are active-LOW. When the POL input is LOW, the outputs are active-HIGH.

$\overline{OE}$ Output Enable. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the output to the high impedance (off) state.

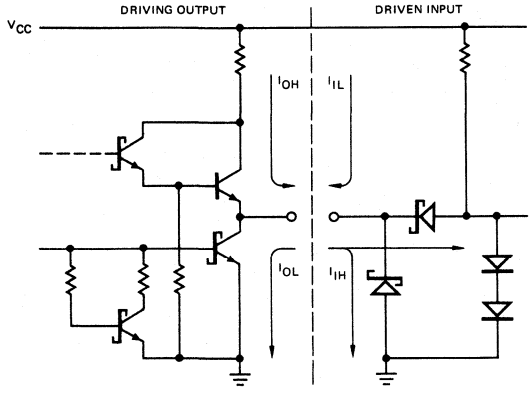
Y_i Decoder outputs. The ten outputs of the decoder.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

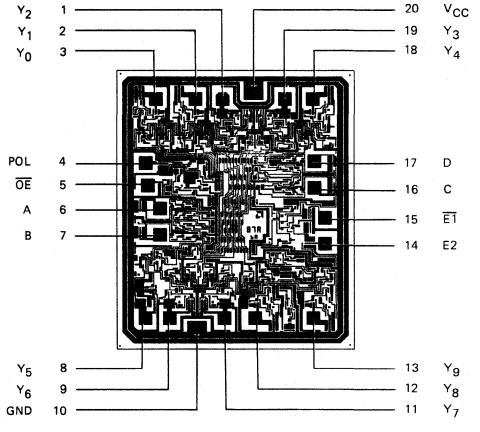
		Am25LS				
			Output HIGH		Output LOW	
Pin No.'s	Input/Output	Input Load	MIL	COM'L	MIL	COM'L
1	Y_2	–	50	130	33	33
2	Y_1	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	POL	1.0	–	–	–	–
5	$\overline{OE}$	1.0	–	–	–	–
6	A	1.0	–	–	–	–
7	B	1.0	–	–	–	–
8	Y_5	–	50	130	33	33
9	Y_6	–	50	130	33	33
10	GND	–	–	–	–	–
11	Y_7	–	50	130	33	33
12	Y_8	–	50	130	33	33
13	Y_9	–	50	130	33	33
14	$\overline{E2}$	1.0	–	–	–	–
15	E1	1.0	–	–	–	–
16	C	1.0	–	–	–	–
17	D	1.0	–	–	–	–
18	Y_4	–	50	130	33	33
19	Y_3	–	50	130	33	33
20	V_{CC}	–	–	–	–	–

Am25LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



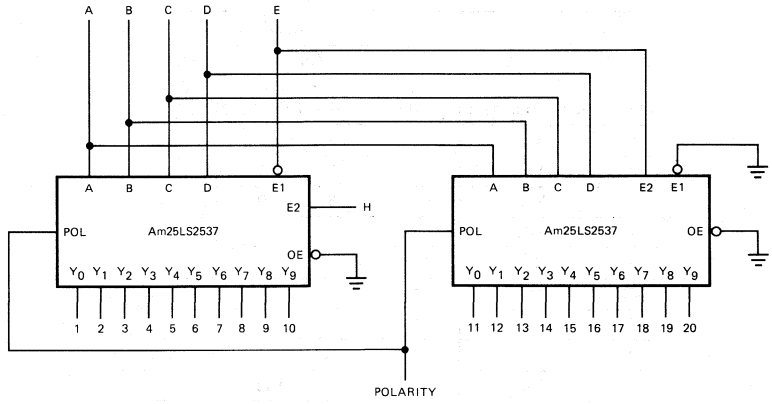
Note: Actual current flow direction shown.

Metallization and Pad Layout

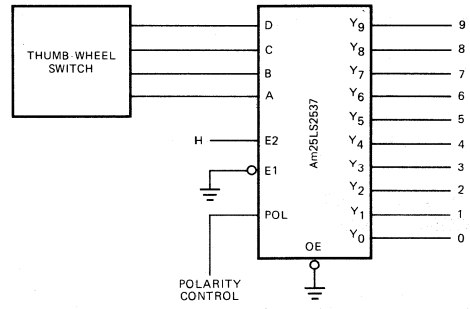


DIE SIZE 0.081" X 0.096"

APPLICATIONS



One-of-Twenty Decoder with Active-High or Active-Low Output Polarity.
Could be used for I/O Decoding in an Am9080A system.



BCD to Decimal (One-of-Ten) Decoder.

Am25LS2538

One-of-Eight Decoder
With Three-State Outputs And Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- A. C. parameters specified over operating temperature and power supply ranges
- 100% product assurance screening to MIL-STD-883 requirements

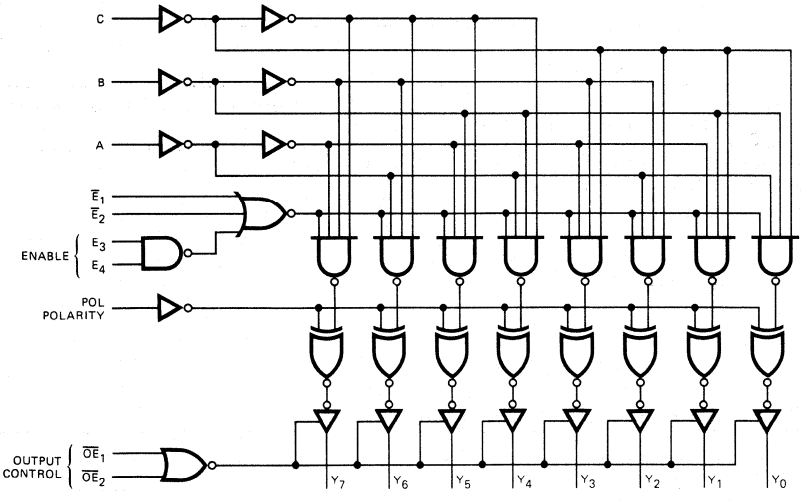
FUNCTIONAL DESCRIPTION

The Am25LS2538 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs—A, B, and C—that are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

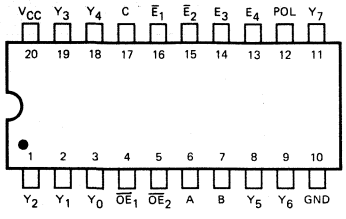
A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package. It also features Am25LS family improved switching specifications, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

LOGIC DIAGRAM
One-of-Eight Decoder

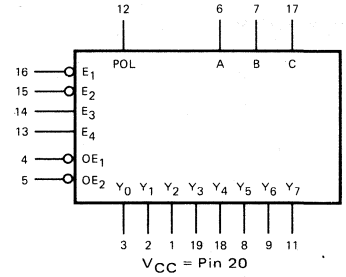


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -1.0mA$ (MIL)	2.4	3.4		Volts
			$I_{OH} = -2.6mA$ (COM'L)	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			21	34	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1 = \overline{E}_2$ = GND : $E_3 = E_4$ = POL = $\overline{OE}_1 = \overline{OE}_2 = 4.5V$.
5. V_{OL} is specified with total device $I_{OL} = 60mA$ (max.).

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

WITCHING CHARACTERISTICS

T_A = +25°C, V_{CC} = 5.0V)

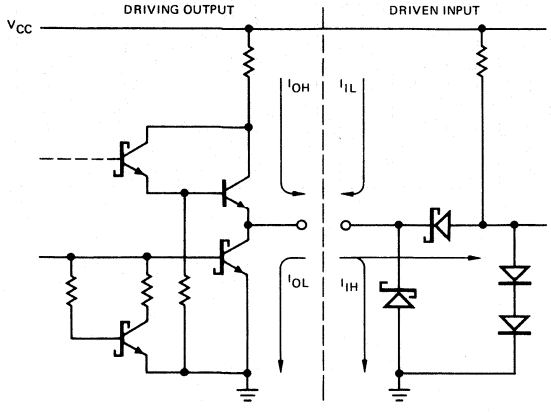
arameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		20	30	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			15	22		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		19	28	ns	
t_{PHL}			20	30		
t_{PLH}	E_3, E_4 to Y_i		21	31	ns	
t_{PHL}			23	34		
t_{PLH}	POL to Y_i		16	24	ns	
t_{PHL}			20	30		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	
t_{ZL}			14	21		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			20	30		

;WITCHING CHARACTERISTICS)VER OPERATING RANGE*

		Am25LS COM'L		Am25LS MIL			
		T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%			
arameters	Description	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		36		42	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			29		37		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		34		39	ns	
t_{PHL}			38		45		
t_{PLH}	E_3, E_4 to Y_i		38		45	ns	
t_{PHL}			43		52		
t_{PLH}	POL to Y_i		29		34	ns	
t_{PHL}			39		49		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		38		45	ns	
t_{ZL}			23		25		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		29		33	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			33		36		

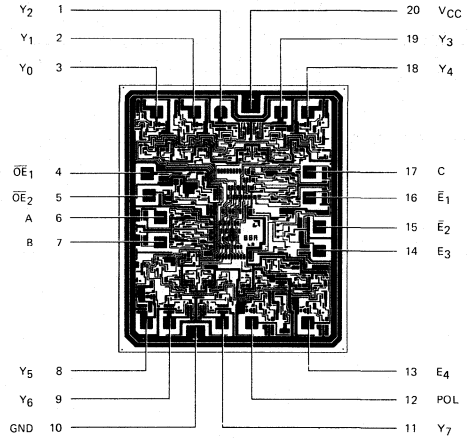
AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Metallization and Pad Layout



DIE SIZE 0.081" X 0.096"

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D The three select inputs to the decoder/demultiplexer.

$\overline{E}_1$, $\overline{E}_2$ The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.

E_3, E_4 The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited.

POL Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.

$\overline{OE}_1$, $\overline{OE}_2$ Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high impedance state.

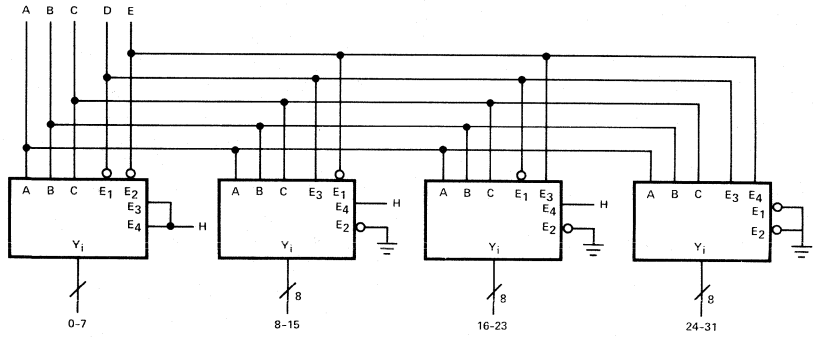
Y_i The eight outputs for the decoder/demultiplexer.

FUNCTION TABLE

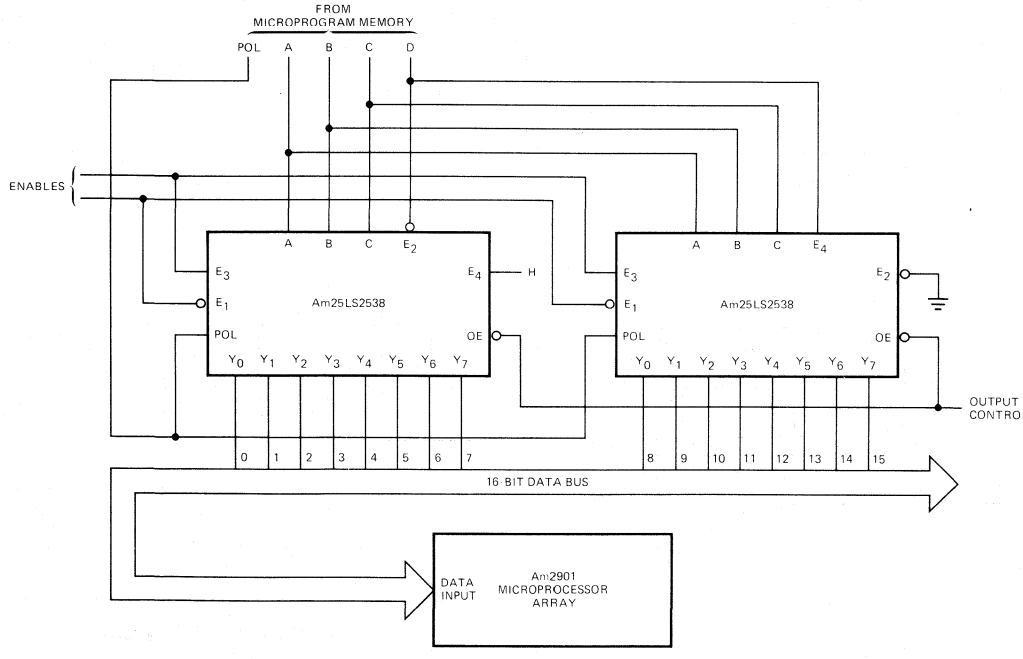
FUNCTION	INPUTS										OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	POL	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High Impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	H	X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	H	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	H	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	L	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	L	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	X	L	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	X	L	H	X	X	X	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	L	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output	L	L	L	L	H	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH L = LOW X = Don't Care Z = High Impedance

APPLICATIONS



One-of-thirty two decoder without additional decoding devices. Can be used for I/O decoding in an Am9080A system.



Two Am25LS2538s can be used to perform a one-of-sixteen-bit mask function or a one-of-sixteen-bit select function to perform bit manipulation in a microprocessor system.

Examples:

D	C	B	A	POL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Function
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Bit Select
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	Bit Select
0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	Bit Mask
1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	Bit Mask

Am25LS2539

Dual One-Of-Four Decoder With Three-State Outputs And Polarity Control

DISTINCTIVE CHARACTERISTICS

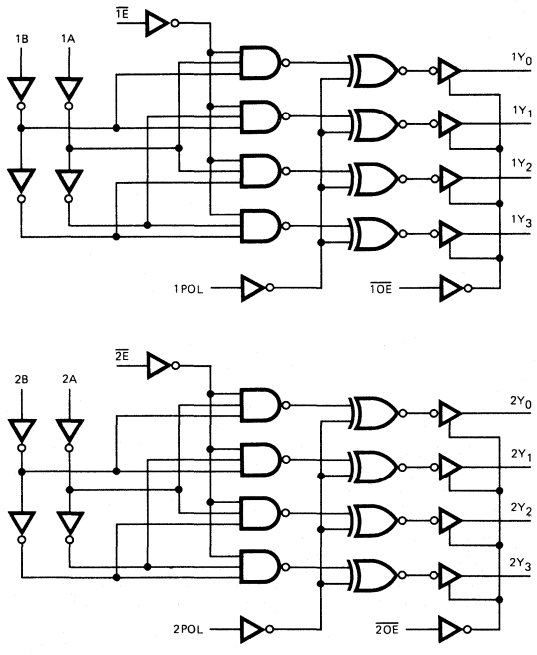
- Two independent decoders/demultiplexers
- Three-state outputs
- Buffered common polarity control
- A. C. parameters specified over operating temperature and power supply ranges
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

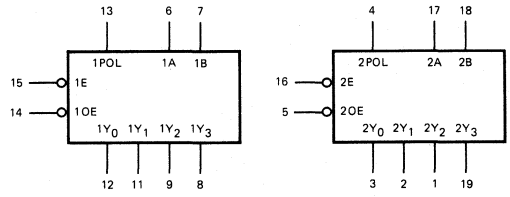
The Am25LS2539 is a dual two-line to four-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. Each decoder has two buffered select inputs—A and B which are decoded to one-of-four Y outputs. An enable input ($\overline{E}$) is used for gating or can be used as a data input for demultiplexing applications. When the enable input goes HIGH, all four decoder functions are inhibited.

An output enable ($\overline{OE}$) input is used to control the three-state outputs of the device. When the $\overline{OE}$ input is LOW, the outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high impedance (off) state. The device also has separate buffered polarity (POL) inputs to force the outputs to either an active-HIGH state or an active-LOW state. When the POL input is LOW, the outputs are active-HIGH and when the POL input is HIGH, the outputs are active-LOW. The device is packaged in a space saving (0.3 inch row spacing) 20-pin package. The device features Am25LS family improved switching specification, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

LOGIC DIAGRAM

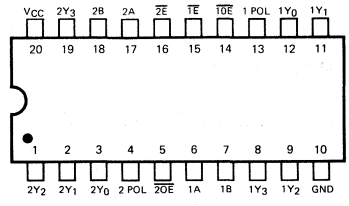


LOGIC SYMBOLS



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				22	37	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: $A = B = \overline{E} = GND$; $POL = \overline{OE} = 4.5V$.
5. V_{OL} is specified with total device $I_{OL} = 60mA$ (max.).

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

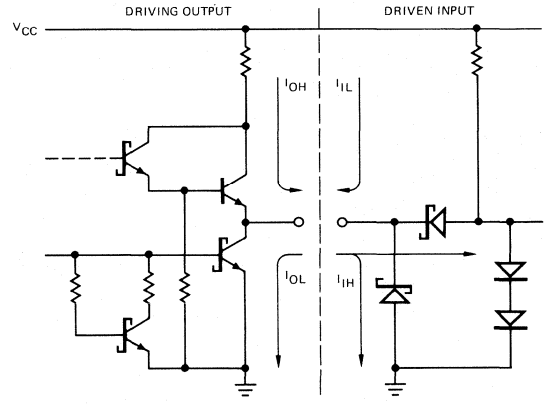
Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B to Y_i		22	33	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	$\overline{E}$ to Y_i		19	28	ns	
t_{PHL}			21	31		
t_{PLH}	POL to Y_i		16	24	ns	
t_{PHL}			19	28		
t_{ZH}	$\overline{OE}$ to Y_i		15	23	ns	
t_{ZL}			15	22		
t_{HZ}	$\overline{OE}$ to Y_i		19	28	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			23	34		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{PLH}	A, B, to Y_i		41		48	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			34		42		
PLH	$\overline{E}$ to Y_i		34		40	ns	
t_{PHL}			38		45		
t_{PLH}	POL to Y_i		29		34	ns	
t_{PHL}			39		49		
t_{ZH}	$\overline{OE}$ to Y_i		38		45	ns	
t_{ZL}			24		25		
t_{HZ}	$\overline{OE}$ to Y_i		33		37	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			36		37		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

DEFINITION OF FUNCTIONAL TERMS

A, B — Select the two select inputs to the decoder/demultiplexer.

$\overline{E}$ Enable — The enable input to the decoder. A HIGH input forces the decoding functions to be inhibited regardless of the A and B inputs.

POL — Polarity Input. The polarity input forces the outputs either an active-HIGH state or an active-LOW state. A LOW on the polarity input forces the output active-HIGH. A HIGH on the polarity input forces the outputs active-LOW.

$\overline{OE}$ — Output Enable. A LOW on the $\overline{OE}$ input enables the outputs. A HIGH on the $\overline{OE}$ inputs forces the outputs to the high impedance (off) state.

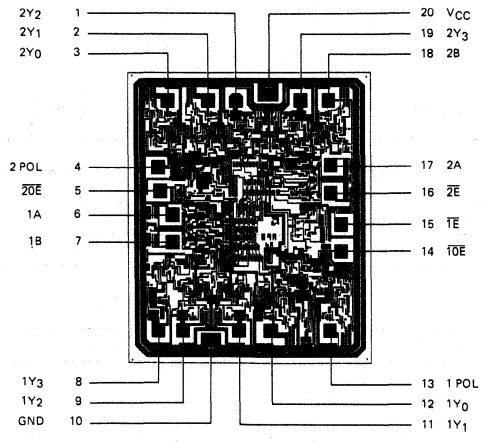
Y_0, Y_1, Y_2, Y_3 — The four decoder/demultiplexer outputs.

FUNCTION TABLE

Function	Inputs					Outputs			
	$\overline{OE}$	$\overline{E}$	POL	B	A	Y_0	Y_1	Y_2	Y_3
High Impedance	H	X	X	X	X	Z	Z	Z	Z
Disable	L	H	L	X	X	L	L	L	L
	L	H	H	X	X	H	H	H	H
Active-High Output	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	L	H	L	L
	L	L	L	H	L	L	L	H	L
	L	L	L	H	H	L	L	L	H
Active-Low Output	L	L	H	L	L	L	H	H	H
	L	L	H	L	H	H	L	H	H
	L	L	H	H	L	H	H	L	H
	L	L	H	H	H	H	H	H	L

H = HIGH X = Don't Care
L = LOW Z = High Impedance

Metallization and Pad Layout

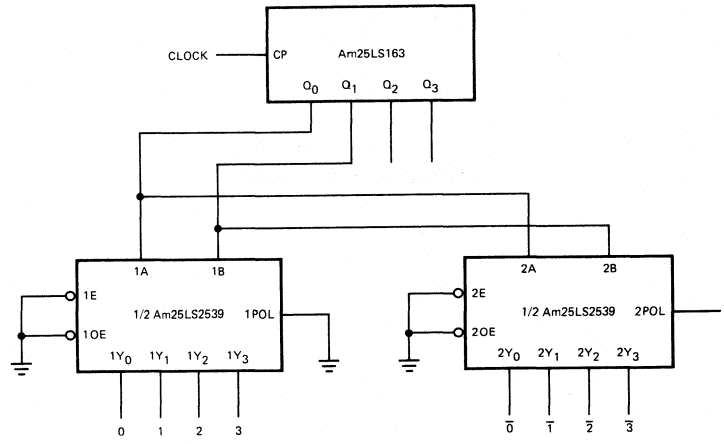


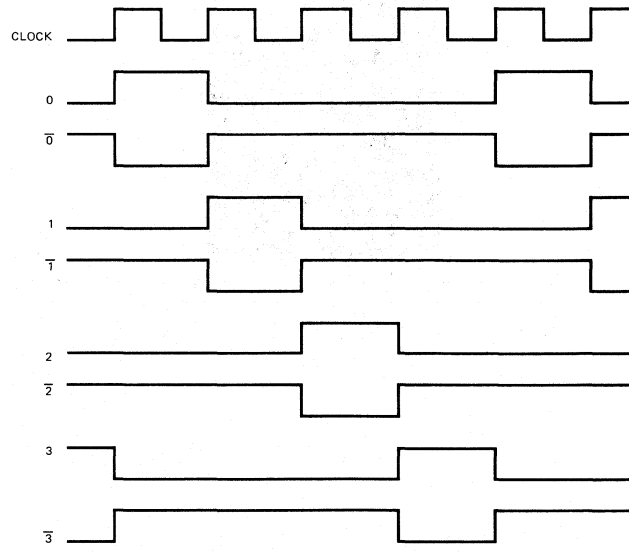
DIE SIZE 0.081" X 0.096"

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS2539PC
Hermetic DIP	0°C to +70°C	AM25LS2539DC
Dice	0°C to +70°C	AM25LS2539XC
Hermetic DIP	–55°C to +125°C	AM25LS2539DM
Hermetic Flat Pak	–55°C to +125°C	AM25LS2539FM
Dice	–55°C to +125°C	AM25LS2539XM

APPLICATIONS





FOUR PHASE CLOCK GENERATOR

Am25LS2548

Chip Select Address Decoder with Acknowledge

DISTINCTIVE CHARACTERISTICS

- One-of-Eight Decoder provides eight chip select outputs
- Acknowledge output responds to enables and read or write command
- Open-collector Acknowledge output for wired-OR application
- Inverting and non-inverting enable inputs for upper address decoding
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

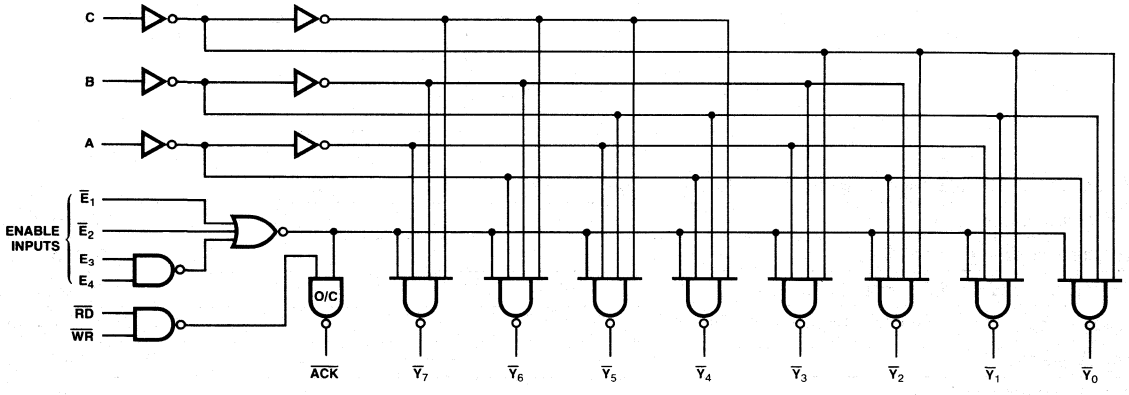
The Am25LS2548 Address Decoder combines a three-line to eight-line decoder with four qualifying enable inputs (two active HIGH and two active LOW) and the acknowledge output required for "ready" or "wait state" control of all popular MOS microprocessors.

The acknowledge output, $\overline{ACK}$, is active LOW and responds to the combination of all enables active and a read ($\overline{RD}$) or write ($\overline{WR}$) input command.

The eight chip select outputs are individually active LOW in response to the combination of all enables active and the corresponding 3-bit input code at inputs A, B, and C.

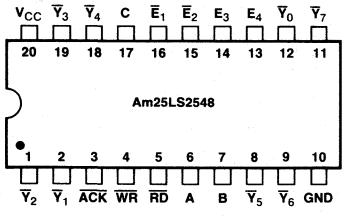
The Am25LS2548 is intended for chip select decoding in small, medium or large systems where multiple chip selects must be generated and address space must be allocated conservatively.

LOGIC DIAGRAM



BLI-045

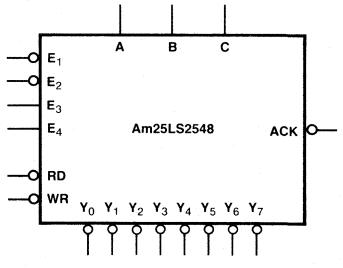
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-046

LOGIC SYMBOL



BLI-047

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −440μA	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			15	20	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. TEST CONDITIONS: A = B = C = $\overline{E}_1$ = $\overline{E}_2$ = GND: RD = WR = E_3 = E_4 = 4.5V.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B or C to $\overline{Y}_i$ (Three Level Delay)		14	20	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			19	27	ns	
t_{PLH}	A, B, or C to $\overline{Y}_i$ (Two Level Delay)		13	18	ns	
t_{PHL}			15	21	ns	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{Y}_i$		13	18	ns	
t_{PHL}			16	23	ns	
t_{PLH}	E_3, E_4 to $\overline{Y}_i$		15	21	ns	
t_{PHL}			19	27	ns	
t_{PLH}	$\overline{WR}$, $\overline{RD}$ to $\overline{ACK}$		25	35	ns	
t_{PHL}			16	22	ns	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{ACK}$		29	40	ns	
t_{PHL}			25	35	ns	
t_{PLH}	E_3, E_4 to $\overline{ACK}$		29	40	ns	
t_{PHL}			25	35	ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	 Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	 Max.	Units	Test Conditions
t_{PLH}	A, B or C to Y_i (Three Level Delay)		27		30	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			34		36	ns	
t_{PLH}	A, B or C to Y_i (Two Level Delay)		23		25	ns	
t_{PHL}			28		31	ns	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{Y}_i$		23		25	ns	
t_{PHL}			29		31	ns	
t_{PLH}	E_3, E_4 to $\overline{Y}_i$		27		28	ns	
t_{PHL}			34		36	ns	
t_{PLH}	$\overline{WR}$, $\overline{RD}$ to $\overline{ACK}$		45		45	ns	
t_{PHL}			31		35	ns	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{ACK}$		45		45	ns	
t_{PHL}			39		40	ns	
t_{PLH}	E_3, E_4 to $\overline{ACK}$		45		45	ns	
t_{PHL}			39		40	ns	

DEFINITION OF FUNCTIONAL TERMS

A, B, C Three-line to eight-line chip select decoder inputs.

$\overline{E}_1$, $\overline{E}_2$ The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled, and forces $\overline{ACK}$ HIGH.

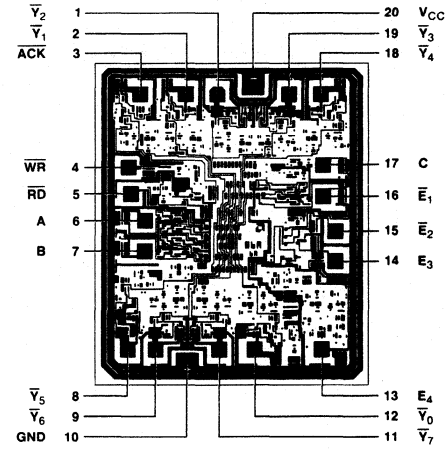
E_3, E_4 The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited, and forces $\overline{ACK}$ HIGH.

$\overline{WR}$, $\overline{RD}$ The write input, $\overline{WR}$, and read input, $\overline{RD}$, are active LOW inputs used as conditions for an active LOW output at the acknowledge, $\overline{ACK}$, output.

$\overline{ACK}$ The acknowledge output, $\overline{ACK}$, is an active LOW output used to signal the microprocessor that specific devices have been selected. $\overline{ACK}$ goes LOW only when $\overline{E}_1$ and $\overline{E}_2$ are LOW, E_3 and E_4 are HIGH and $\overline{WR}$ or $\overline{RD}$ is LOW.

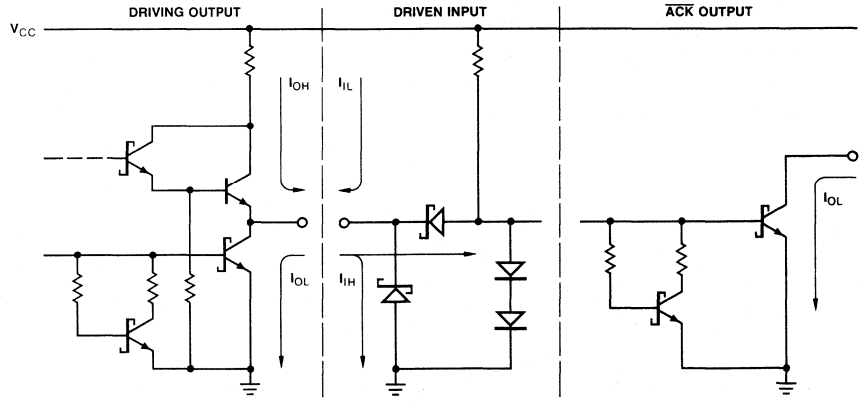
$\overline{Y}_i$ The eight active LOW chip select outputs.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.081" X 0.096"

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



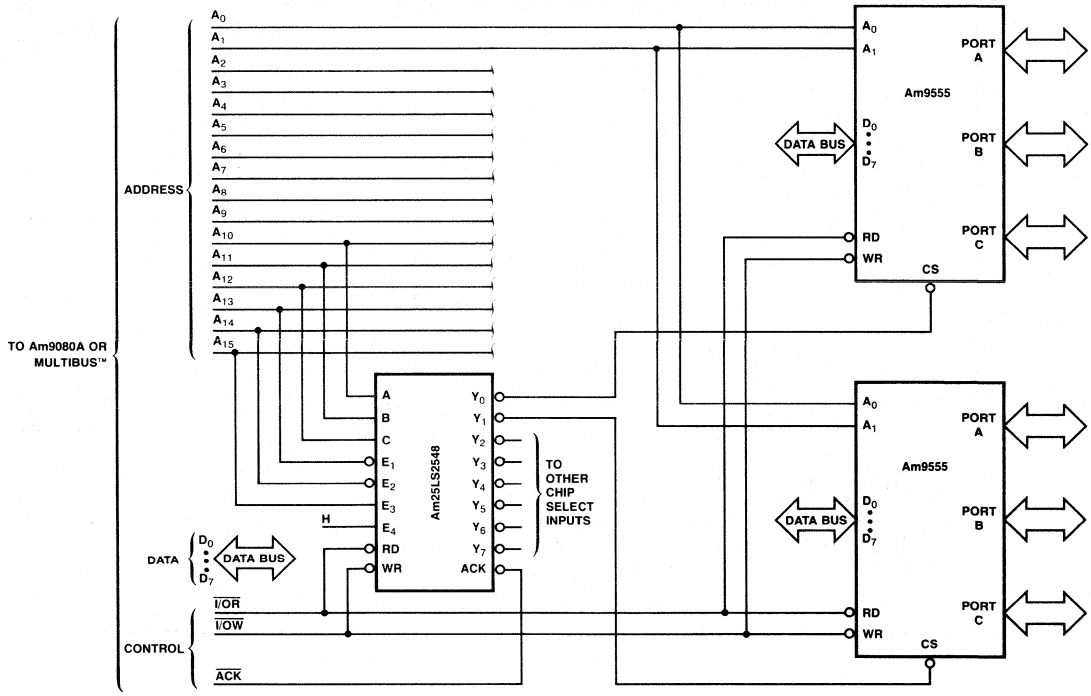
Note: Actual current flow direction shown.

BLI-048

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS2548PC
Hermetic DIP	0°C to +70°C	AM25LS2548DC
Dice	0°C to +70°C	AM25LS2548XC
Hermetic DIP	−55°C to +125°C	AM25LS2548DM
Hermetic Flat Pak	−55°C to +125°C	AM25LS2548FM
Dice	−55°C to +125°C	AM25LS2548XM

APPLICATION DIAGRAM



BLI-049

FUNCTION TABLES

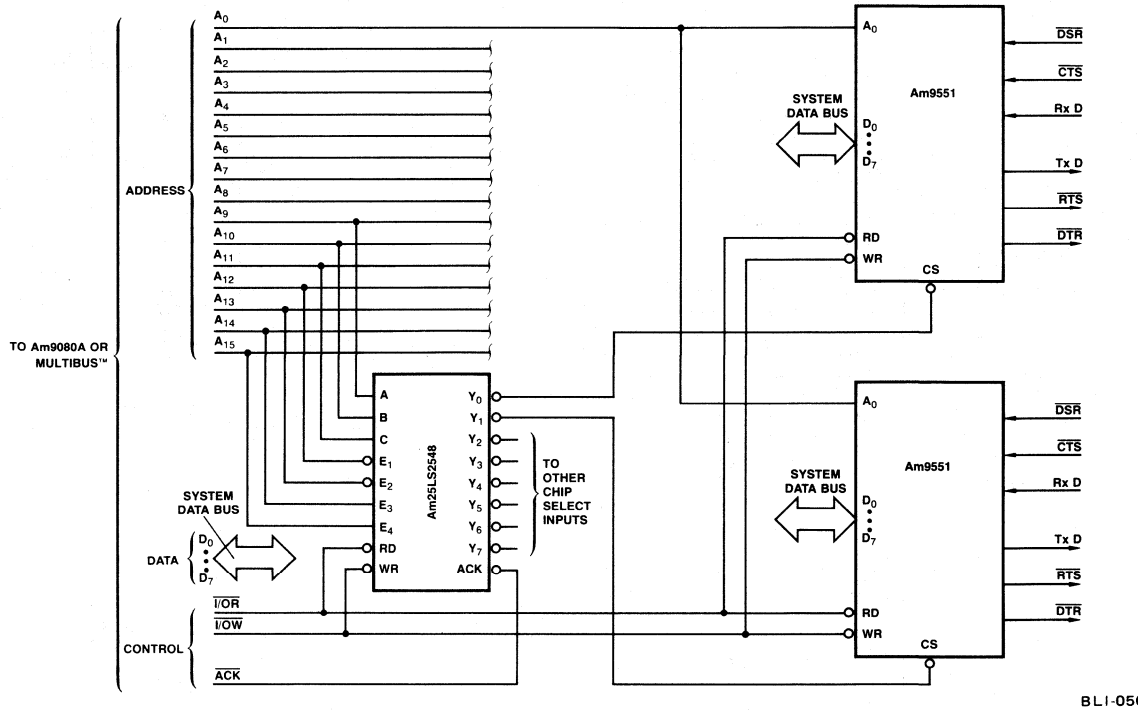
CHIP SELECT OUTPUTS Y_i

C	B	A	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	H	L	H	H
H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	H	L
X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	X	L	X	H	H	H	H	H	H	H	H
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H

ACKNOWLEDGE OUTPUT $\overline{ACK}$

$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

APPLICATION DIAGRAM



BLI-050

Am25LS2568 • Am25LS2569

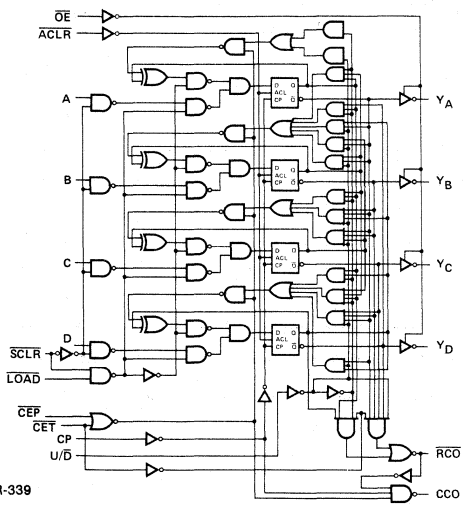
Four-Bit Up/Down Counters with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 4-bit synchronous counter, synchronously programmable
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus organized systems
- Internal look-ahead carry logic and two count enable lines for high speed cascaded operation
- Ripple carry output for cascading
- Clock carry output for convenient modulo configuration
- Fully buffered outputs
- Second sourced as the 54LS/74LS568 and LS569
- Advanced low-power Schottky technology
- 100% product assurance screening to MIL-STD-883 requirements

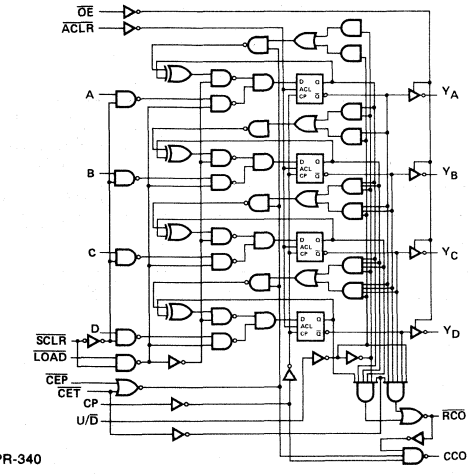
LOGIC DIAGRAMS

Am25LS2568 (BCD)



MPR-339

Am25LS2569 (BINARY)



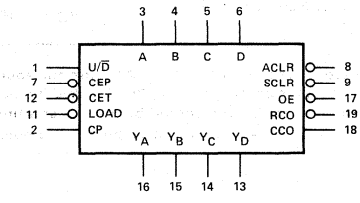
MPR-340

FUNCTIONAL DESCRIPTION

The Am25LS2568 and Am25LS2569 are programmable up/down BCD and Binary counters respectively with three-state outputs for bus organized systems. All functions except output enable ($\overline{OE}$) and asynchronous clear ($\overline{ACLR}$) occur on the positive edge of the clock input (CP).

With the $\overline{LOAD}$ input LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Counting is enabled only when $\overline{CEP}$ and $\overline{CET}$ are LOW and LOAD is HIGH. The up-down input (U/$\overline{D}$) controls the direction of count, HIGH counts up and LOW counts down. Internal look-ahead carry logic and an active LOW ripple carry output ($\overline{RCO}$) allows for high-speed counting and cascading. During up-count, the $\overline{RCO}$ is LOW at binary 9 for the LS2568 (binary 15 for the LS2569) and upon down-count, it is LOW at binary 0. Normal cascaded operations requires only the $\overline{RCO}$ to be connected to the succeeding block at $\overline{CET}$. When counting, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse and only when $\overline{RCO}$ is LOW. Two active LOW reset lines are available, synchronous clear ($\overline{SCLR}$) and a master reset asynchronous clear ($\overline{ACLR}$). The output control ($\overline{OE}$) input forces the counter output into the high impedance state when HIGH and when LOW, the counter outputs are enabled.

LOGIC SYMBOL



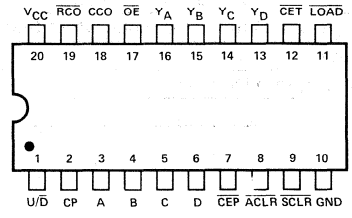
V_{CC} = Pin 20

GND = Pin 10

MPR-341

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MPR-342

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0 V ±5%	MIN. = 4.75 V	MAX. = 5.25 V
MIL	T_A = −55°C to +125°C	V_{CC} = 5.0 V ±10%	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)				Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_i	MIL, I_{OH} = −1.0mA		2.4	3.4		Volts
				COM'L, I_{OH} = −2.6mA		2.4	3.2		
			$\overline{RCO}$, CCO	I_{OH} = −440μA	MIL	2.5	3.4		
					COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA				0.4	Volts
				I_{OL} = 8.0mA				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{ACLR}$, $\overline{OE}$, U/$\overline{D}$, $\overline{Load}$					0.3	mA
			A, B, C, D, CP, $\overline{CEP}$					0.4	
			$\overline{CET}$, $\overline{SCLR}$					0.65	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V						20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0 V						0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	V_O = 0.4 V					−20	μA
			V_O = 2.4 V					20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.				−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.					28	43	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{OE}$ = HIGH, all other inputs = GND, all outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +7.0
DC Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5.0 m

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Any Q; $\overline{Load}$ = LOW			12	18	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				14	21		
t_{PLH}	Clock to Any Q; $\overline{Load}$ = HIGH			12	18	ns	
t_{PHL}				14	21		
t_{PLH}	$\overline{CET}$ to $\overline{RCO}$			11	16	ns	
t_{PHL}				6	10		
t_{PLH}	U/$\overline{D}$ to $\overline{RCO}$			15	23	ns	
t_{PHL}				13	20		
t_{PLH}	Clock to $\overline{RCO}$			24	35	ns	
t_{PHL}				18	26		
t_{PLH}	Clock to CCO			10	15	ns	
t_{PHL}				10	15		
t_{PLH}	$\overline{CET}$ or $\overline{CEP}$ to CCO			10	15	ns	
t_{PHL}				17	25		
t_{PLH}	$\overline{ACLR}$ to Any Q			N.A.	N.A.	ns	
t_{PHL}				17	26		
t_s	Set-up	A, B, C, D	22			ns	
		$\overline{SCLR}$	20				
		$\overline{Load}$	30				
		U/$\overline{D}$	30				
		$\overline{CET}$, $\overline{CEP}$	25				
t_s	$\overline{SCLR}$ Recovery (inactive) to Clock		30			ns	
t_h	Data Hold		0			ns	
f_{max}	Maximum Clock Frequency (Note 1)		25	40		MHz	
t_{pw}	Clock Pulse Width		25			ns	
t_{PZH}	$\overline{OE}$ to Any Q; Enable				11	ns	
t_{PZL}					19		
t_{PHZ}	$\overline{OE}$ to Any Q; Disable				18	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{PLZ}					24		

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS2568/2569
FUNCTION TABLE

	INPUTS												OUTPUTS					
MODE	LOAD	CEP	CET	U/$\overline{D}$	ASYNC CLEAR	SYNC CLEAR	$\overline{OE}$(1)	D_0	D_1	D_2	D_3	CP	Q_0	Q_1	Q_2	Q_3	RC	CLOCK CARRY
Clear (ASYNC)	X	X	X	1	0	X	0	X	X	X	X	X	0	0	0	0	1	1
	X	X	X	0	0	X	0	X	X	X	X	X	0	0	0	0	0	⊔(2)
Clear (SYNC)	X	X	X	1	1	0	0	X	X	X	X	↑	0	0	0	0	1	1
	X	X	X	0	1	0	0	X	X	X	X	↑	0	0	0	0	0	⊔(2)
Load	0	X	1	X	1	1	0	X	X	X	X	↑	$Q_n = D_n$				1	1
	0	X	0	0	1	1	0	0	0	0	0	↑	0	0	0	0	0	⊔(2)
	0	X	0	1	1	1	0	1	1	1	1(3)	↑	1	1	1	1(3)	0	⊔(2)
Count Up	1	0	0	1	1	1	0	X	X	X	X	↑	Q_{n+1}				(4)	(5)
Count Down	1	0	0	0	1	1	0	X	X	X	X	↑	Q_{n-1}				(6)	(5)
Inhibit	1	0	1	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
	1	1	0	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
	1	1	1	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
Output Disable	X	X	X	X	X	X	1	X	X	X	X	X	Z	Z	Z	Z	N.C.	N.C.

↑ = CLOCK LOW-to-HIGH transition
X = Don't Care
D_n = D_0 thru D_3 input level prior to clock transition
Q_{n+1} = Next higher count in binary sequence
Q_{n-1} = Next lower count in binary sequence
N.C. = No change

Notes:
1. Register performs all correct logic for any state of $\overline{OE}$, but $\overline{OE}$ = 0 to view outputs.
2. Follows CLOCK if CET = CEP = 0, otherwise remains HIGH.
3. 1001 for LS68.
4. LOW for one full CLOCK cycle when maximum count is reached, otherwise remains HIGH.
5. Follows CLOCK when RC = 0.
6. LOW for one full CLOCK cycle when minimum count is reached, otherwise remains HIGH.

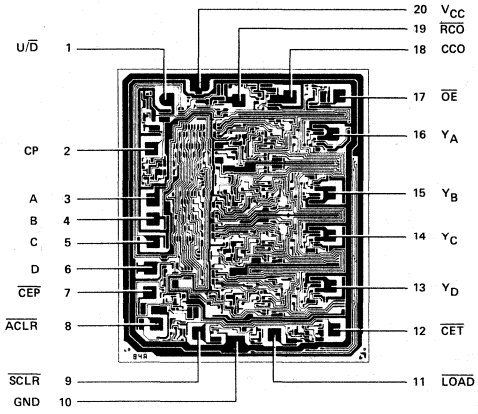
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Min.	Am25LS COM'L Max.	Am25LS MIL $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Any Q; $\overline{Load}$ = LOW			22		24	ns	$C_L = 50pF$, $R_L = 2.0k\Omega$
t_{PHL}				29		35		
t_{PLH}	Clock to Any Q; $\overline{Load}$ = HIGH			22		24	ns	
t_{PHL}				29		35		
t_{PLH}	$\overline{CET}$ to $\overline{RCO}$			18		19	ns	
t_{PHL}				17		21		
t_{PLH}	U/$\overline{D}$ to $\overline{RCO}$			26		28	ns	
t_{PHL}				26		30		
t_{PLH}	Clock to $\overline{RCO}$			39		40	ns	
t_{PHL}				34		39		
t_{PLH}	Clock to CCO			17		18	ns	
t_{PHL}				22		27		
t_{PLH}	$\overline{CET}$ or $\overline{CEP}$ to CCO			16		17	ns	
t_{PHL}				36		45		
t_{PLH}	$\overline{ACLR}$ to Any Q			N.A.		N.A.	ns	
t_{PHL}				37		45		
t_s	Set-up	A, B, C, D	29		35		ns	
		$\overline{SCLR}$	25		30			
		$\overline{Load}$	38		45			
		U/$\overline{D}$	38		45			
		$\overline{CET}$, $\overline{CEP}$	33		40			
t_s	SCLR Recovery (inactive) to Clock		39		50		ns	
t_h	Data Hold		0		5		ns	
f_{max}	Maximum Clock Frequency (Note 1)		20		18		MHz	
t_{pw}	Clock Pulse Width		31		37		ns	
t_{ZH}	$\overline{OE}$ to Any Q; Enable			16		20	ns	
t_{ZL}				26		34		
t_{HZ}	$\overline{OE}$ to Any Q; Disable			20		22	ns	$C_L = 5.0pF$, $R_L = 2.0k\Omega$
t_{LZ}				30		36		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
N.A. not applicable.

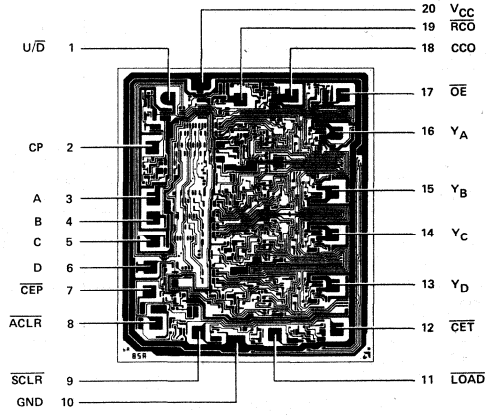
Metallization and Pad Layouts

Am25LS2568



DIE SIZE 0.087" X 0.103"

Am25LS2569

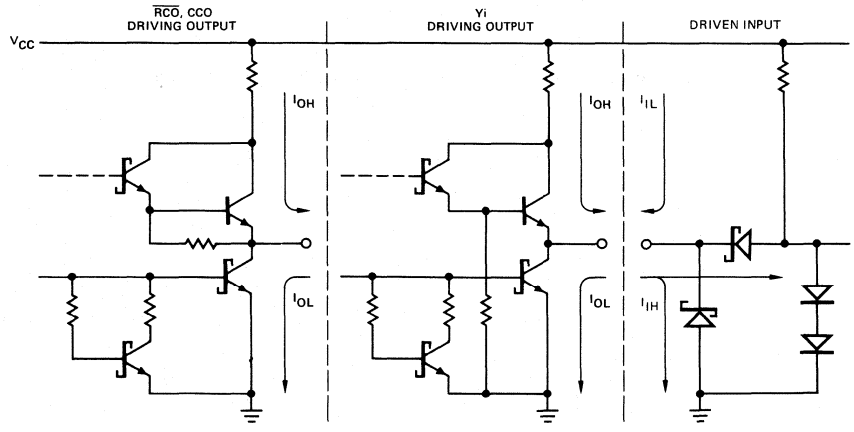


DIE SIZE 0.087" X 0.103"

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D	The four programmable data inputs.
$\overline{CEP}$	Count Enable Parallel. Can be used to enable and inhibit counting in high speed cascaded operation. $\overline{CEP}$ must be LOW to count.
$\overline{CET}$	Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count.
CP	Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.
$\overline{LOAD}$	Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.
$U/\overline{D}$	Up/Down Count Control. HIGH counts up and LOW counts down.
$\overline{ACLR}$	Asynchronous Clear. Master reset of counters to zero when $\overline{ACLR}$ is LOW, independent of the clock.
$\overline{SCLR}$	Synchronous clear of counters to zero on the next clock edge when $\overline{SCLR}$ is LOW.
$\overline{OE}$	A HIGH on the output control sets the four counter outputs in the high impedance, and a LOW, enables the output.
Y_A, Y_B, Y_C, Y_D	The four counter outputs.
$\overline{RCO}$	Ripple Carry Output. Output will be LOW on the maximum count on up-count. Upon down-count, $\overline{RCO}$ is LOW at 0000.
CCO	Clock Carry Output. While counting and $\overline{RCO}$ is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS

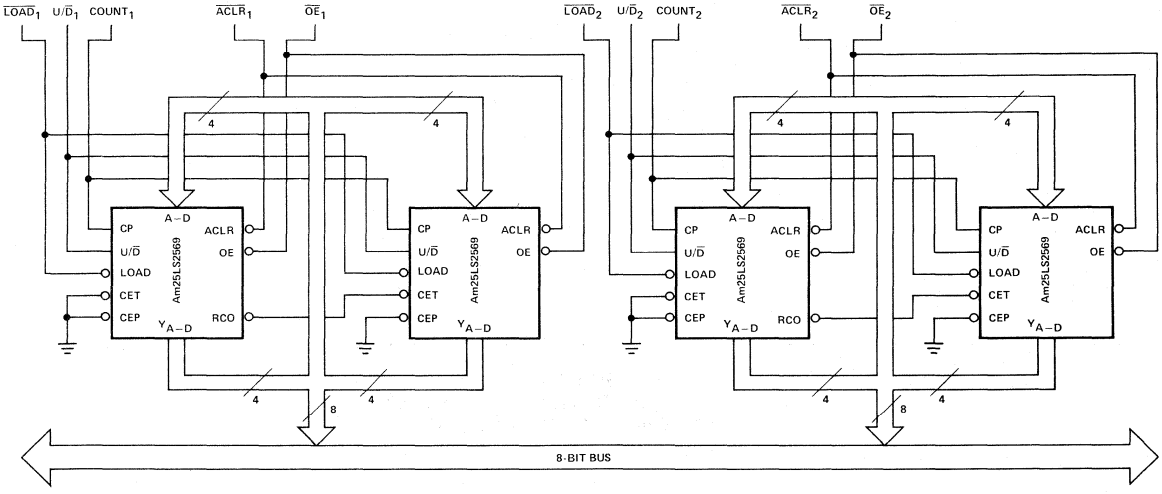


Note: Actual current flow direction shown.

ORDERING INFORMATION

Package Type	AMD Package Outline	Temperature Range	Am25LS2568 Order Number	Am25LS2569 Order Number
Molded DIP	P-20-1	0°C to +70°C	AM25LS2568PC	AM25LS2569PC
Hermetic DIP	D-20-1	0°C to +70°C	AM25LS2568DC	AM25LS2569DC
Dice	–	0°C to +70°C	AM25LS2568XC	AM25LS2569XC
Hermetic DIP	D-20-1	−55°C to +125°C	AM25LS2568DM	AM25LS2569DM
Hermetic Flat Pak	F-20-1	−55°C to +125°C	AM25LS2568FM	AM25LS2569FM
Dice	–	−55°C to +125°C	AM25LS2568XM	AM25LS2569XM

APPLICATION



MICROPROGRAMMABLE DUAL-EVENT 8-BIT COUNTERS

High Performance Schottky Index

Am25S05

Four-Bit by Two-Bit 2's Complement Multiplier

Distinctive Characteristics

- Provides 2's complement multiplication at high speed without correction.
- Can be used in a combinatorial array or in a time sequenced mode.
- Multiplies two 12-bit signed numbers in typically 115ns.
- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Reduced input loading as compared to Am2505.
- 100% reliability assurance testing in compliance with MIL-STD-883.

3

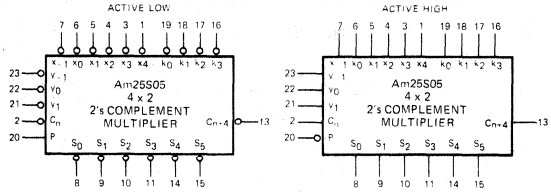
FUNCTIONAL DESCRIPTION

The Am25S05 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4x2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function S = XY + K where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m+n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

A number of connection schemes are possible. Figure 1 shows the connection scheme that results in the fastest multiply. If higher speed is required an array can be split into several parts, and the parts added with high-speed look-ahead carry adders.

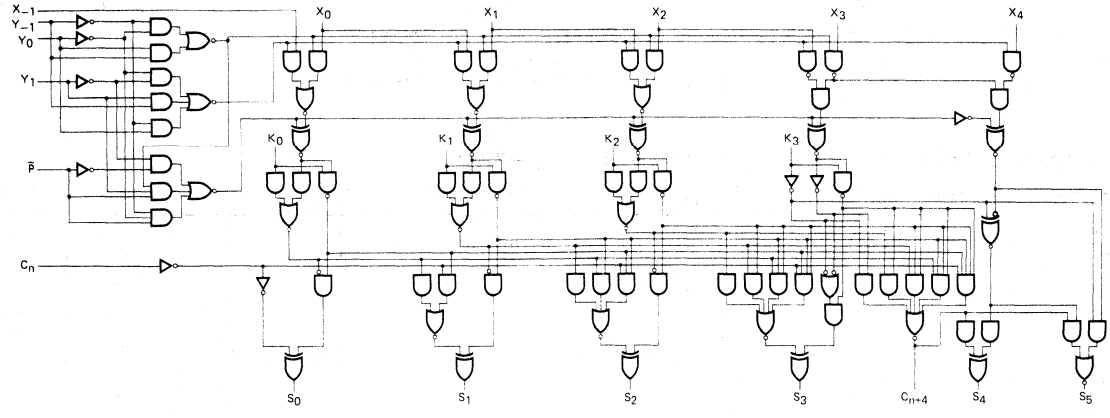
Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control $\overline{P}$.

LOGIC SYMBOLS



V_{CC} = Pin 24
GND = Pin 12

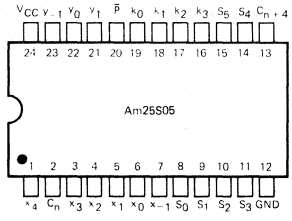
LOGIC DIAGRAM



Am25S05 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM25S05PC
Hermetic DIP	0°C to +75°C	AM25S05DC
Dice	0°C to +75°C	AM25S05XC
Hermetic DIP	–55°C to +125°C	AM25S05DM
Hermetic Flat Pak	–55°C to +125°C	AM25S05FM
Dice	–55°C to +125°C	AM25S05XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S05XC, DC, PC	T_A = 0°C to +75°C	V_{CC} = 4.75 V to 5.25 V
Am25S05XM, DM	T_A = −55°C to +125°C	V_{CC} = 4.50 V to 5.50 V
Am25S05FM	T_C = −55°C to +125°C	V_{CC} = 4.50 V to 5.50 V

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	XM	2.5	3.3		Volts
			XC	2.7	3.3		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2.0	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., Y_1 = 0V			120	175	mA

Note 1. Typical Limits are at V_{CC} = 5.0V, 25°C Ambient and maximum loading.
Note 2. Actual input currents are obtained by multiplying unit load current by the input load factor. (See loading rules)

Switching Characteristics (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, R_L = 280Ω)

Parameters	From (Input)	To (Output)	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	C_n	C_{n+4}	See Test Table	4 4	8 9	12 14	ns
t_{PLH} t_{PHL}	C_n	$S_{0,1,2,3}$		6 5	12 10	18 15	ns
t_{PLH} t_{PHL}	C_n	$S_{4,5}$		7 6	15 13	22 20	ns
t_{PLH} t_{PHL}	Any k	C_{n+4}		3 5	6.5 10	12 15	ns
t_{PLH} t_{PHL}	Any k	$S_{0,1,2,3}$		6 4	13.5 9.5	20 14	ns
t_{PLH} t_{PHL}	Any k	$S_{4,5}$		3 3	15.5 12.5	23 19	ns
t_{PLH} t_{PHL}	Any x	C_{n+4}		8 9	17 18	26 27	ns
t_{PLH} t_{PHL}	Any x	$S_{0,1,2,3}$		10 10	21 21	32 32	ns
t_{PLH} t_{PHL}	Any x	$S_{4,5}$		6 5	23.5 21.5	35 32	ns
t_{PLH} t_{PHL}	Any y	C_{n+4}		11 10	23 20	34 30	ns
t_{PLH} t_{PHL}	Any y	$S_{0,1,2,3}$		11 11	23 23	34 34	ns
t_{PLH} t_{PHL}	Any y	$S_{4,5}$		12 12	25 25	37 37	ns

SWITCHING TIME TEST TABLE

Input	Outputs	Inputs at 0V (remaining inputs at 4.5V)
C_n	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All X
k_2	C_{n+4}, S_{23}, S_{45}	P, Y_{-1}, Y_1, All X
k_3	S_3	P, Y_{-1}, Y_1, All X
k_3	S_{45}	P, Y_{-1}, Y_1, All X, C_n
x_{-1}	C_{n+4}, S_{0123}, S_{45}	P, Y_1, All k
x_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All k
x_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_2	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_3	S_3	P, Y_{-1}, Y_1, All k
x_3	S_{45}	P, Y_{-1}, Y_1, All k, C_n
x_4	S_{45}	P, Y_1, All k, C_n
y_{-1}	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_0	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_1	C_{n+4}, S_{0123}, S_{45}	X_0, X_1, X_2, X_3, X_4, All k

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS

C_n The carry input to the high-speed adder.

C_{n+4} The carry output from the high-speed adder.

K_i The constant field used for accumulating partial products. i = 0, 1, 2, 3. At the beginning of the array the K field can be used to add a 2's complement number to the least significant half of the double length product.

$\overline{P}$ The polarity control input. This input must be at a low-logic level for numbers in the active high logic representation, and held high for numbers in the active low logic representation.

S_i The product outputs. i = 0, 1, 2, 3, 4, 5.

X_i The multiplicand inputs. i = -1, 0, 1, 2, 3, 4. At the first column of the array x_{-1} must be held at logic '0', and at the last column of the array x_4 is connected to x_3.

y_i The multiplier inputs. i = -1, 0, 1. At the first row of the array y_{-1} must be held at logic '0'.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

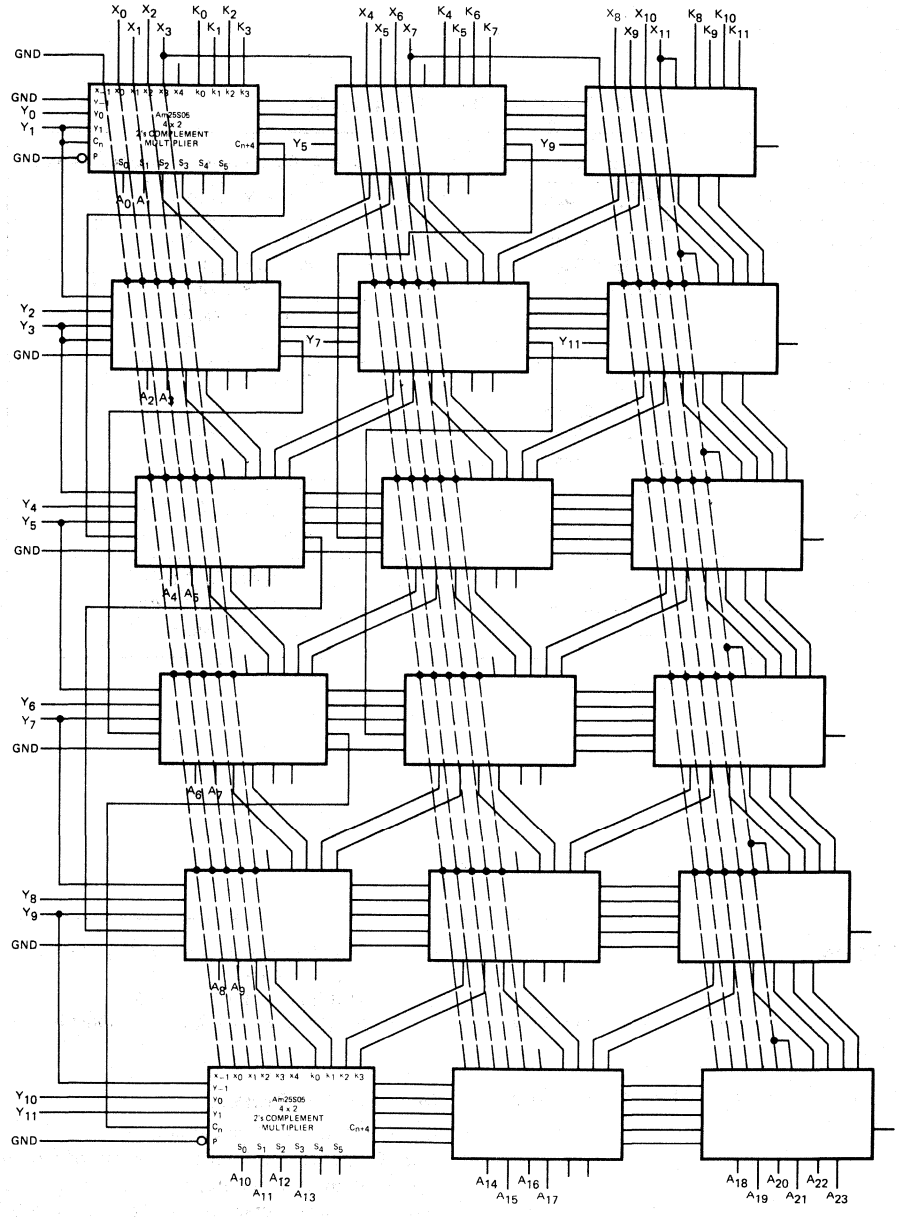
V_{IL} Maximum logic LOW input voltage.

V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

APPLICATION



Critical speed carries between columns have been interchanged with 2's complement carry-ins Y_5, Y_7, Y_9, Y_{11} for highest speed.

Figure 1. High Speed 12x12 2's Complement Multiplication

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400 Series	1.25	1.25
Advanced Micro Devices 9300/2500 Series	1.25	1.25
FSC Series 9300	1.25	1.25
TI Series 54/7400	1.25	1.25
Signetics Series 8200	2.5	2.5
National Series DM 75/85	1.25	1.25
DTL Series 930	15	1.25

OPERATION TABLE

Y Multiplier			Operation X Multiplicand
y_{-1}	y_0	y_1	
0	0	0	K + 0
1	0	0	K + X
0	1	0	K + X
1	1	0	K + 2X
0	0	1	K – 2X
1	0	1	K – X
0	1	1	K – X
1	1	1	K – 0

Active Low Inputs and Outputs
'1' = Low, '0' = High, P = High
Active High Inputs and Outputs
'1' = High, '0' = Low, $\overline{P}$ = Low

Am25S05 LOADING RULES IN UNIT LOADS

Input/Output	Pin No.'s	Input Unit Load Input HIGH	Input LOW	Fanout Output HIGH	Output LOW
x_4	1	0.2	0.2	–	–
C_n	2	0.2	0.2	–	–
x_3	3	0.2	0.2	–	–
x_2	4	0.4	0.4	–	–
x_1	5	0.4	0.4	–	–
x_0	6	0.4	0.4	–	–
x_{-1}	7	0.2	0.2	–	–
S_0	8	–	–	20	10
S_1	9	–	–	20	10
S_2	10	–	–	20	10
S_3	11	–	–	20	10
GND	12	–	–	–	–
C_{n+4}	13	–	–	20	10
S_4	14	–	–	20	10
S_5	15	–	–	20	10
k_3	16	2	2	–	–
k_2	17	2	2	–	–
k_1	18	2	2	–	–
k_0	19	2	2	–	–
$\overline{P}$	20	1	1	–	–
y_1	21	0.6	0.6	–	–
y_0	22	0.6	0.6	–	–
y_{-1}	23	0.6	0.6	–	–
V_{CC}	24	–	–	–	–

A Schottky TTL Unit Load is defined as 50μA at 2.7V at the HIGH Logic Level and –2.0 mA at 0.5 V at the LOW Logic Level.

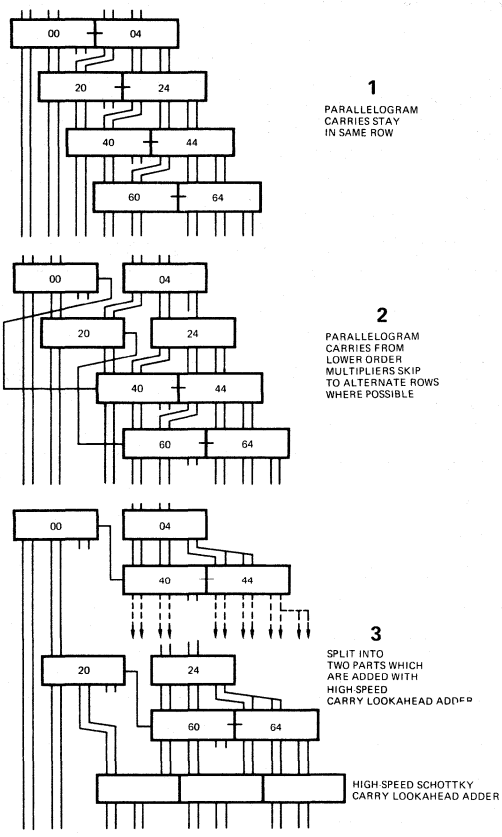
USER NOTES

1. Arithmetic in the multiplier is performed in the 2's complement notation, which requires a carry in at the first stage. This is accomplished by connecting the y_i multiplier bit to the appropriate carry input terminal i = 1, 3, 5 . . .
2. The multiplier can perform multiplication in either the active high (positive logic) or active low (negative logic) representations by reinterpreting the active logic level and by grounding or leaving the polarity control pin $\overline{P}$ open circuit respectively.
3. Multiplication can be performed in number representations other than 2's complement by either correcting the 2's complement product or adding in a correction at the beginning of the multiplication at the K inputs. 2's complement numbers are represented as: $X_2 = x - x_s 2^{n-1}$.

Number representation	Correction
2's complement	None
1's complement	Add $x_s Y_2 + y_s X_2 + x_s y_s$ at k inputs
Unsigned (magnitude)	Extend multiplier and multiplicand one bit at the least significant end. Form $x_0 y_0 + y_0 x + x_0 y$ with conditional adder and add to array shifted two places up at k inputs. Force $k_s, y_s, x_s = 0$.
Sign magnitude	$x_s = 0, y_s = 0$ None
	$x_s = 1, y_s = 0$ Form $[(XY)_2 + 2^{n-1} y]$
	$x_s = 0, y_s = 1$ Form $[(XY)_2 + 2^{n-1} x]$
	$x_s = 1, y_s = 1$ Add $2^{n-1}(x + y) - 2^{2n-2}$

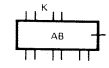
4. For the highest speed array with the multipliers arranged in a parallelogram structure carries between certain multipliers are exchanged with the y carry-ins needed for 2's complement subtract. The delays in the array are then equalized as best possible as shown in Figure 1.
5. For higher speed multiplication the array can be split into several parts that can be added together with high-speed adders.
6. Rounding off to a single length product can be achieved by adding a '1' to the array at the most significant positive k input of the array, ignoring the most significant product digit, and using the remainder of the most significant part of the product.
7. Truncation of a product without round off enables some of the multipliers in the array to be removed.

CONNECTION SCHEMES



TYPICAL MULTIPLICATION TIMES

Array Size Bits	Total Multiplication Time (ns)	Package Count	
		Am25S05	Am54S/74S181
4x4	35	2	
8x8	75	8	
12x12	115	18	
12x12	82	18	5
16x16	155	32	
16x16	111	32	7
16x16	98	32	16
20x20	195	50	
20x20	130	50	9
24x24	235	72	
24x24	149	72	11
24x24	125	72	24
28x28	275	98	
28x28	168	98	13
32x32	315	128	
32x32	187	128	15
32x32	152	128	32



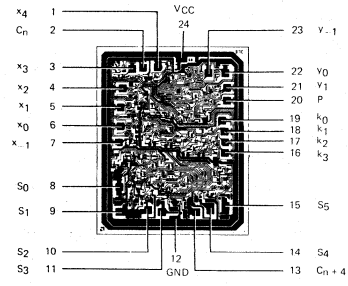
Am25S05

$Y = (y_{-1}\ y_0\ y_1)\ 2^A$

$X = (x_{-1}\ x_0\ x_1\ x_2\ x_3)\ 2^B$

Fig. 2

Metallization and Pad Layout



DIE SIZE 0.088" X 0.110"

Am25S07•Am25S08

Hex/Quad Parallel D Registers With Register Enable

Distinctive Characteristics

- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

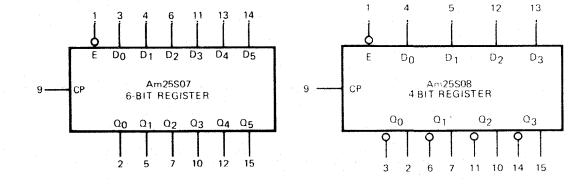
3

FUNCTIONAL DESCRIPTION

The Am25S07 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am25S08 is a 4-bit register with a buffered common register enable. The devices are similiar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

LOGIC SYMBOLS

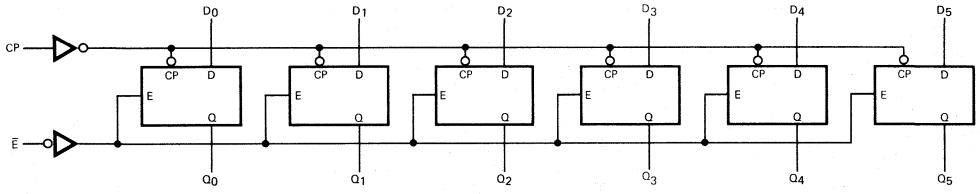


MPR-343 MPR-344

V_{CC} = Pin 16
GND = Pin 8

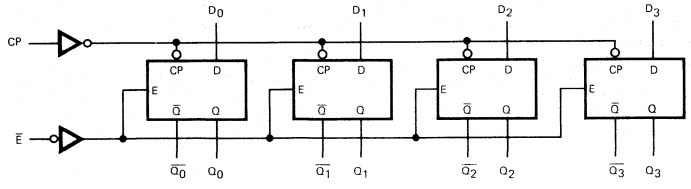
LOGIC DIAGRAMS

Am25S07



MPR-345

Am25S08

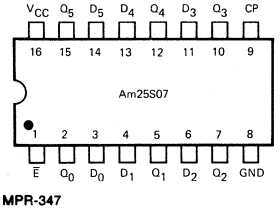


MPR-346

Low-Power Schottky versions of these devices available also. Order Am25LS07 and Am25LS08.

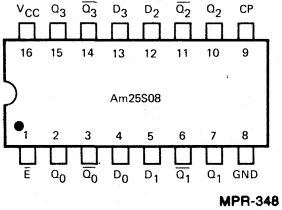
CONNECTION DIAGRAMS
Top Views

Am25S07



MPR-347

Am25S08



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Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S07XC, Am25S08XC	T_A = 0°C to +70°C	V_{CC} = 5.0 V ±5% (COM'L)	MIN. = 4.75 V	MAX. = 5.25 V
Am25S07XM, Am25S08XM	T_A = −55°C to +125°C	V_{CC} = 5.0 V ±10% (MIL)	MIN. = 4.5 V	MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1 mA V_{IN} = V_{IH} or V_{IL}	XC	2.7	3.4		Volts
			XM	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20 mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18 mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	S07		90	144	mA
			S08		60	96	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Output	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 280Ω	4	8	12	ns
t_{PHL}	Clock to Output		4	11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data		5.5			ns
t_s	Enable		9			ns
t_h	Data		3			ns
t_h	Enable		3			ns

Am25S07 LOADING RULES (In STTL Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
D_0	3	1	–	–
D_1	4	1	–	–
Q_1	5	–	20	10
D_2	6	1	–	–
Q_2	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_3	10	–	20	10
D_3	11	1	–	–
Q_4	12	–	20	10
D_4	13	1	–	–
D_5	14	1	–	–
Q_5	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

Am25S08 LOADING RULES (In STTL Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
$\overline{Q}_0$	3	–	20	10
D_0	4	1	–	–
D_1	5	1	–	–
$\overline{Q}_1$	6	–	20	10
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
$\overline{Q}_2$	11	–	20	10
D_2	12	1	–	–
D_3	13	1	–	–
$\overline{Q}_3$	14	–	20	10
Q_3	15	–	20	10
V_{CC}	16	–	–	–

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{E}$ Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Q_i The TRUE register outputs.

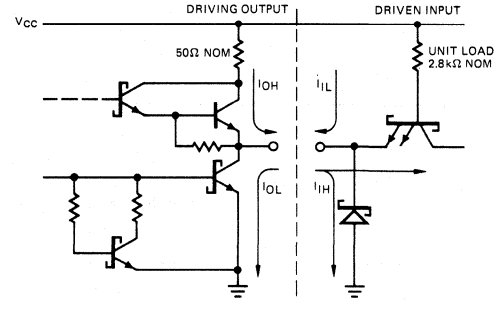
$\overline{Q}_i$ The complement register outputs

FUNCTION TABLE

Inputs			Outputs	
$\overline{E}$	D_i	CP	Q_i	$\overline{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

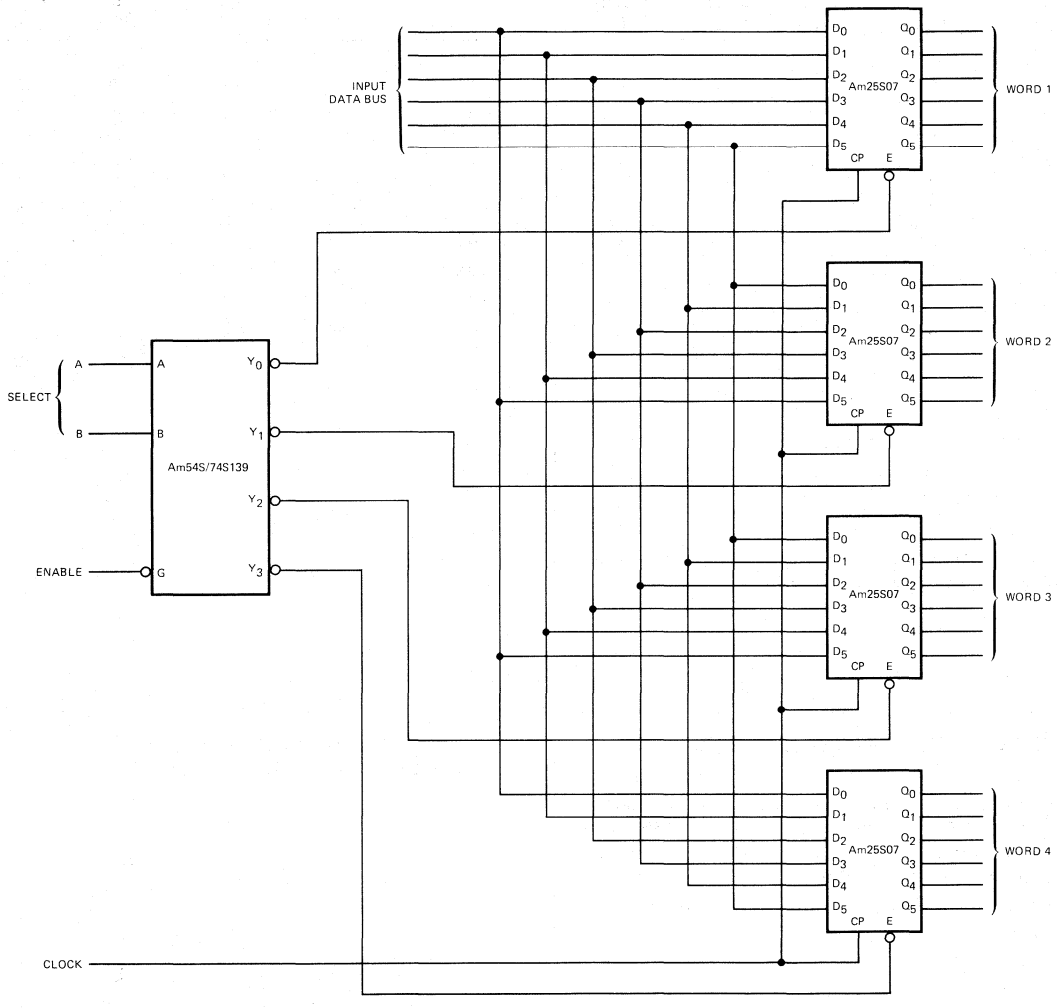
H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25S08 Only

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

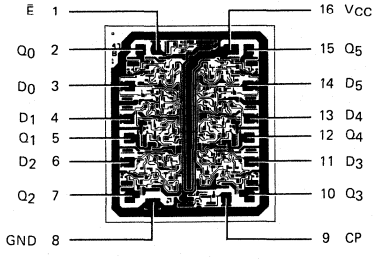
APPLICATIONS



Selective Register Loading of Data on Synchronous Clock.

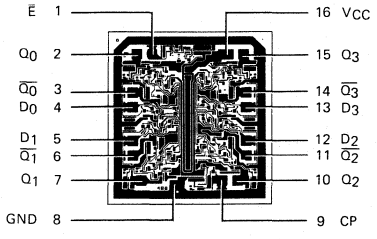
Metallization and Pad Layout

Am25S07



DIE SIZE: 0.070" X 0.083"

Am25S08



DIE SIZE: 0.067" X 0.073"

Am25S09

Quad Two-Input, High-Speed Register

istinctive Characteristics

Four-bit register accepts data from one of two 4-bit input fields.

Edge triggered clock action

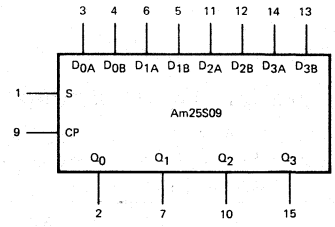
High-speed Schottky technology.

- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am25S09 is a dual port high-speed, four-bit register using advanced Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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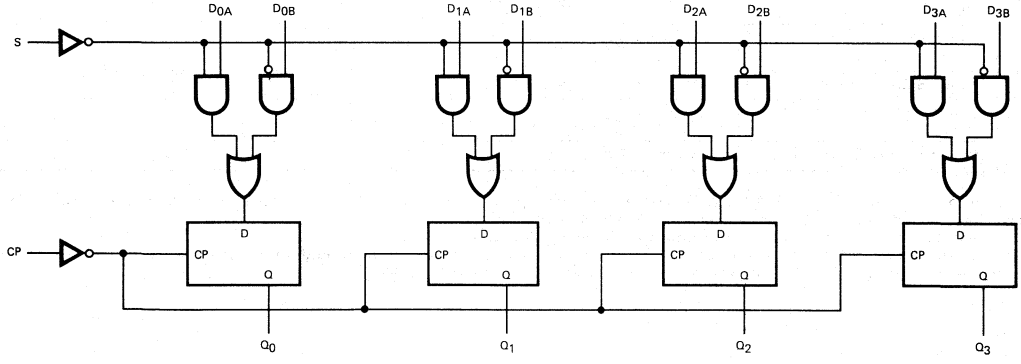
LOGIC DIAGRAM



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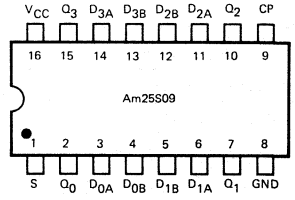
Low-Power Schottky version of this part available also. Order part number Am25LS09.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +5.5
DC Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5.0 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S09XC T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am25S09XM T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20.0mA V_{IN} = V_{IH} or V_{IL}			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2.0	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			75	120	mA

Notes: 1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q HIGH	V_{CC} = 5.0 V, C_L = 15pF, R_L = 280Ω		8	12	ns
t_{PHL}	Clock to Q LOW			11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data Set-up Time		5.5			ns
t_s	Select Input Set-up Time		10			ns
t_h	Data Hold Time		3			ns
t_h	Select Input Hold Time		3			ns

FUNCTION TABLE

SELECT S	CLOCK CP	DATA D_{iA}	INPUTS D_{iB}	OUTPUT Q_i
L	↑	L	X	L
L	↑	H	X	H
H	↑	X	L	L
H	↑	X	H	H

H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

L = LOW Voltage Level
i = 0, 1, 2, or 3

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
S	1	1	–	–
Q_0	2	–	20	10
D_{0A}	3	1	–	–
D_{0B}	4	1	–	–
D_{1B}	5	1	–	–
D_{1A}	6	1	–	–
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
D_{2A}	11	1	–	–
D_{2B}	12	1	–	–
D_{3B}	13	1	–	–
D_{3A}	14	1	–	–
Q_3	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and −2.0 mA measured at 0.5 V LOW.

DEFINITION OF FUNCTIONAL TERMS

D_{0A}, D_{1A}, D_{2A}, D_{3A} The "A" word into the two-input multiplexer of the D flip-flops.

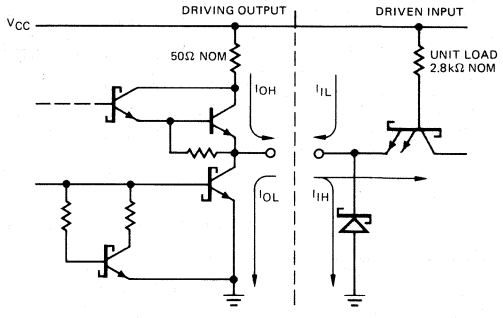
D_{0B}, D_{1B}, D_{2B}, D_{3B} The "B" word into the two-input multiplexer of the D flip-flops.

Q_0, Q_1, Q_2, Q_3 The outputs of the four D-type flip-flops of the register.

S Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH the B word is applied to the D inputs of the flip-flops.

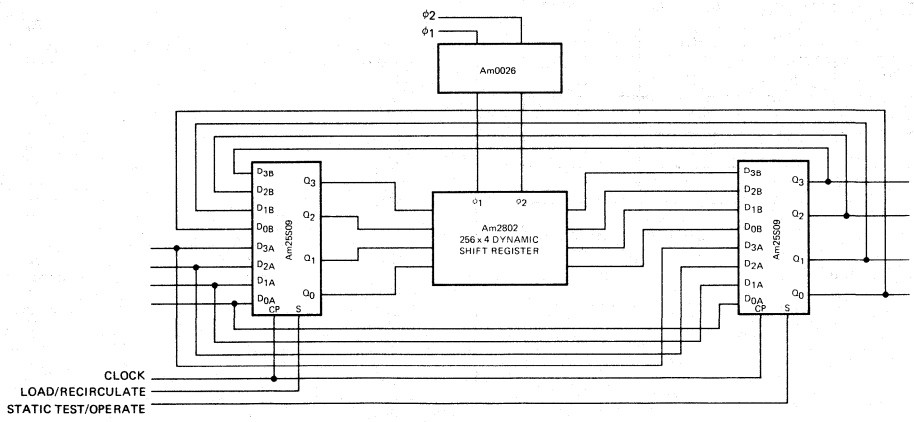
CP Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

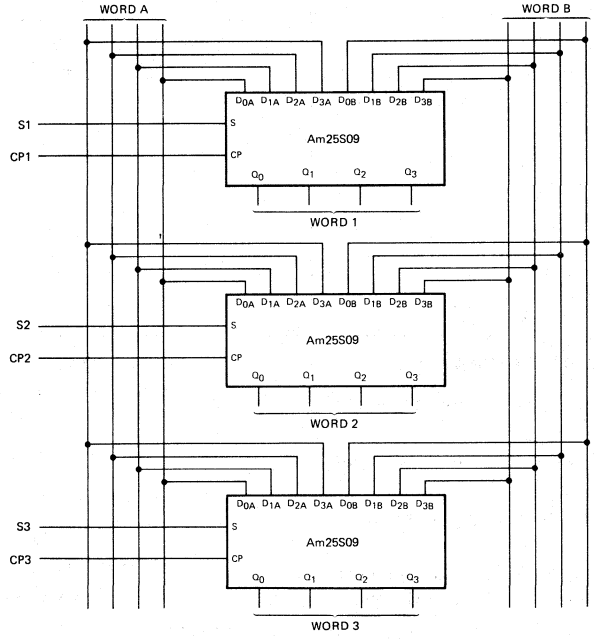


Note: Actual current flow direction shown

APPLICATIONS

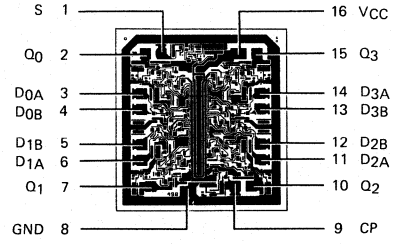


Am25S09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.



Am25S09 used to store a word from either data bus A or data bus B.

Metallization and Pad Layout



DIE SIZE: 0.067" X 0.073"

Am25S10

Four-Bit Shifter With Three-State Outputs

istinctive Characteristics

Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.

Three-state outputs for bus organized systems.

- 6.5 ns typical data propagation delay
- Alternate source is 54S/74S350
- 100% reliability assurance testing in compliance with MIL-STD-883.

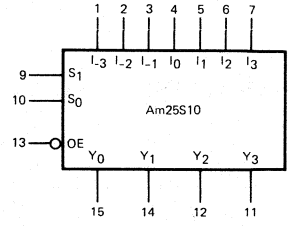
3

FUNCTIONAL DESCRIPTION

The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field S_0 and S_1. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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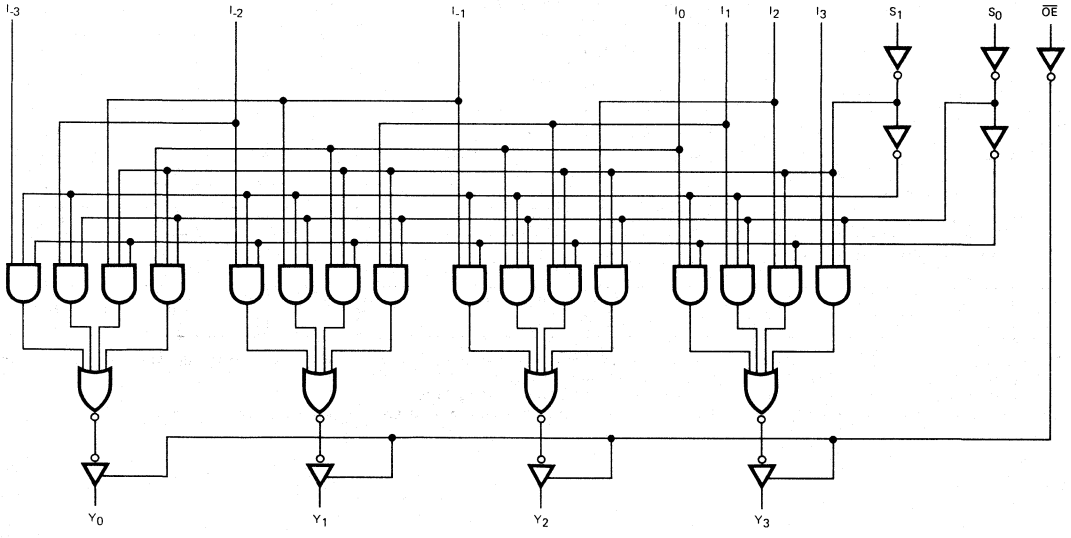
LOGIC DIAGRAM



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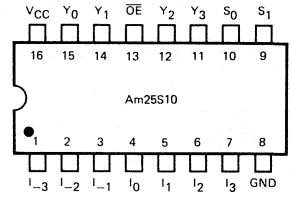
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25S10PC
Hermetic DIP	0°C to +70°C	AM25S10DC
Dice	0°C to +70°C	AM25S10XC
Hermetic DIP	−55°C to +125°C	AM25S10DM
Hermetic Flat Pak	−55°C to +125°C	AM25S10FM
Dice	−55°C to +125°C	AM25S10XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

MPR-354

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +5.5
DC Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5.0 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S10XC T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V

Am25S10XM T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	XM I_{OH} = −2mA	2.4	3.4		Volts
			XC I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2.0	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	µA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX.	V_O = 2.4 V			50	µA
			V_O = 0.5 V			−50	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All outputs open, All inputs = GND			60	85	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data Input to Output	V_{CC} = 5.0 V, C_L = 15pF, R_L = 280Ω		5	7.5	ns
t_{PHL}				8	12	
t_{PLH}	Select to Output			11	17	ns
t_{PHL}				13	20	
t_{ZH}	Output Control $\overline{OE}$ to Output				19.5	ns
t_{ZL}					21	
t_{HZ}	Output Control $\overline{OE}$ to Output	V_{CC} = 5 V, C_L = 5pF, R_L = 280Ω		5	8	ns
t_{LZ}				10	15	

DEFINITION OF FUNCTIONAL TERMS

I_i The seven data inputs of the shifter.

$\overline{OE}$ Enable. When the enable is HIGH, the four outputs are in the high impedance state. When the enable is LOW, the selected I_i inputs are present at the outputs.

S_0, S_1 Select inputs. Controls the number of places the inputs are shifted.

Y_i The four outputs of the shifter.

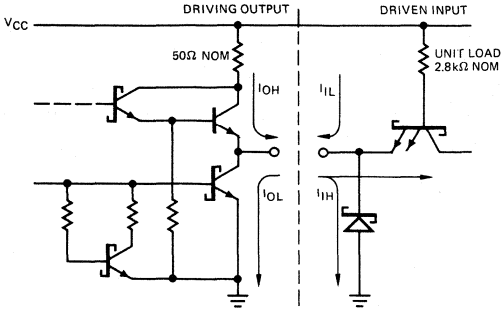
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load (Note 1)	Fan-out Output HIGH XM	Fan-out Output HIGH XC	Fan-out Output LOW
I_{-3}	1	1	–	–	–
I_{-2}	2	1.5	–	–	–
I_{-1}	3	1.5	–	–	–
I_0	4	1.5	–	–	–
I_1	5	1.5	–	–	–
I_2	6	1.5	–	–	–
I_3	7	1	–	–	–
GND	8	–	–	–	–
S_1	9	1	–	–	–
S_0	10	1	–	–	–
Y_3	11	–	40	130	10
Y_2	12	–	40	130	10
$\overline{OE}$	13	1	–	–	–
Y_1	14	–	40	130	10
Y_0	15	–	40	130	10
V_{CC}	16	–	–	–	–

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and –2.0mA measured at 0.5 V LOW.

Note: 1. The fan-in on I_{-2}, I_{-1}, I_0, I_1 and I_2 will not exceed 1.5 Unit Loads when measured at V_{IL} = 0.5 V. As V_{IL} is decreased to 0 V, the input current I_{IL} MAX. increases to –4, –6, –8, –6 and –4 mA respectively due to the decrease in current sharing with the internal select buffer outputs.

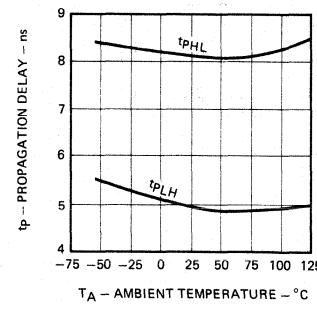
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



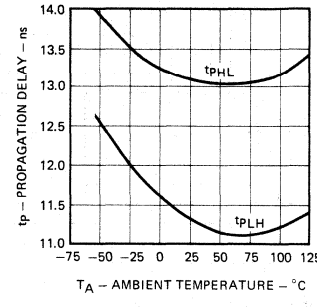
Note: Actual current flow direction shown.

PERFORMANCE CURVES
SWITCHING CHARACTERISTICS

Data to Output (Typical)



Select to Output (Typical)



LOGIC EQUATIONS

$$Y_0 = \overline{S}_0 \overline{S}_1 I_0 + S_0 \overline{S}_1 I_{-1} + \overline{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$

$$Y_1 = \overline{S}_0 \overline{S}_1 I_1 + S_0 \overline{S}_1 I_0 + \overline{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$

$$Y_2 = \overline{S}_0 \overline{S}_1 I_2 + S_0 \overline{S}_1 I_1 + \overline{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$

$$Y_3 = \overline{S}_0 \overline{S}_1 I_3 + S_0 \overline{S}_1 I_2 + \overline{S}_0 S_1 I_1 + S_0 S_1 I_0$$

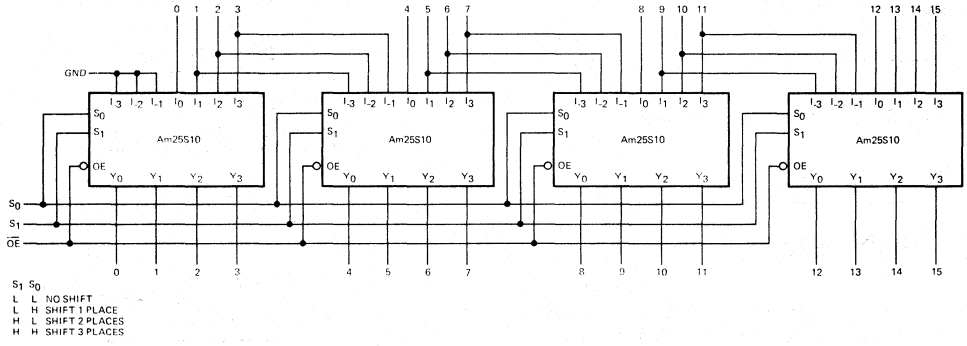
Note: For additional information, see page 5-54

TRUTH TABLE

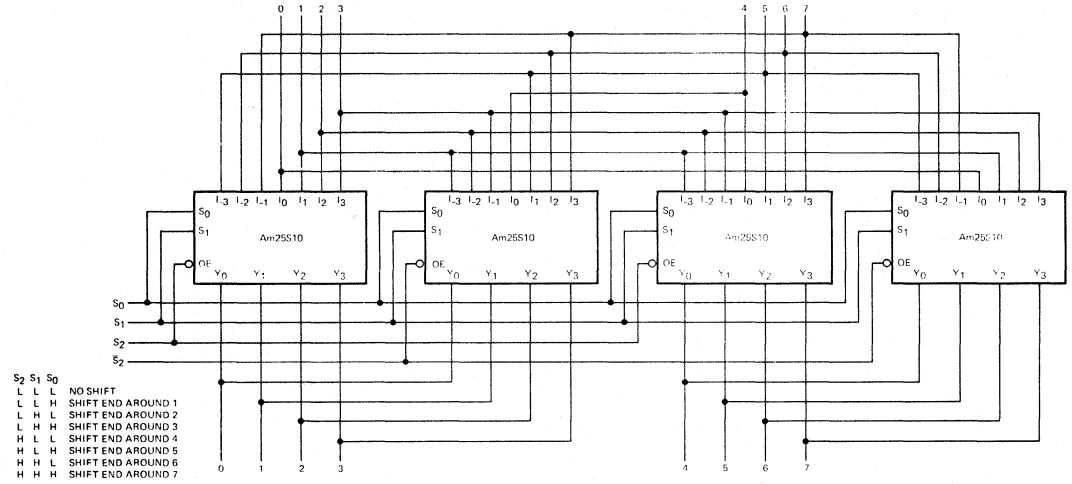
$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance State
D_n at input I_n may be either HIGH or LOW and output Y_m will follow the selected D_n input level.

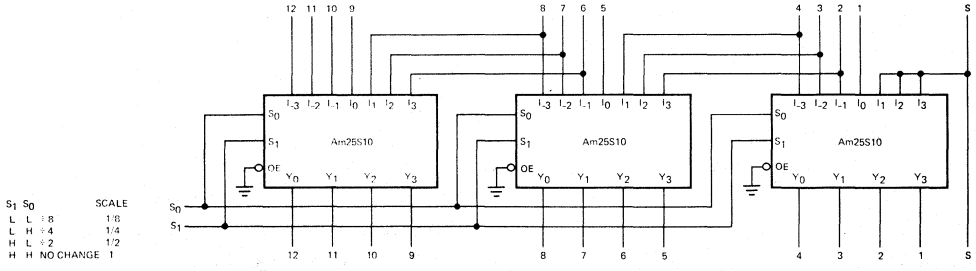
APPLICATIONS



16-Bit Shift-Up 0, 1, 2, or 3 Places

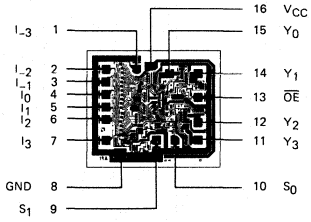


8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places



13-Bit 2's Complement Scaler

Metallization and Pad Layout



DIE SIZE 0.056" X 0.066"

Am25S10
FOUR-BIT SHIFTER

By John R. Mick

INTRODUCTION

The Am25S10 is a high-speed MSI combinatorial logic block built using advanced Schottky technology. The device has the ability to shift four bits of data 0, 1, 2 or 3 places. The Am25S10 has two select lines that are decoded internally to determine the number of places the data is shifted. The device has seven data inputs I_{-3}, I_{-2}, I_{-1}, I_0, I_1, I_2, and I_3 and 4 three-state data outputs Y_0, Y_1, Y_2, and Y_3 as shown in the logic symbol diagram of Figure 1. The three-state outputs allow several devices to be bus organized for shifts of more than three places with a single level device propagation delay time. The three-state outputs are controlled by a single buffered active-LOW output control $\overline{OE}$. When the output control is LOW, the data outputs will follow the selected data inputs. When the output control is HIGH, the data outputs offer a high-impedance to the data bus.

FUNCTIONAL DESCRIPTION

The logic equations describing the output shifting capability of the Am25S10 when the output control is LOW are:

$$Y_0 = \overline{S}_0\ \overline{S}_1\ I_0 + S_0\ \overline{S}_1\ I_{-1} + \overline{S}_0\ S_1\ I_{-2} + S_0\ S_1\ I_{-3}$$
$$Y_1 = \overline{S}_0\ \overline{S}_1\ I_1 + S_0\ \overline{S}_1\ I_0 + \overline{S}_0\ S_1\ I_{-1} + S_0\ S_1\ I_{-2}$$
$$Y_2 = \overline{S}_0\ \overline{S}_1\ I_2 + S_0\ \overline{S}_1\ I_1 + \overline{S}_0\ S_1\ I_0 + S_0\ S_1\ I_{-1}$$
$$Y_3 = \overline{S}_0\ \overline{S}_1\ I_3 + S_0\ \overline{S}_1\ I_2 + \overline{S}_0\ S_1\ I_1 + S_0\ S_1\ I_0$$

From these equations it is seen that each output is operationally equivalent to a four-input multiplexer with the inputs connected such that the select code generates successive one-bit shifts of the input data word. The logic diagram of Figure 2 shows the internal connection of each multiplexer with respect to the seven data inputs. Because of this internal connection scheme, several devices can be connected to perform shifts of 0, 1, 2, or 3 places on words of any length.

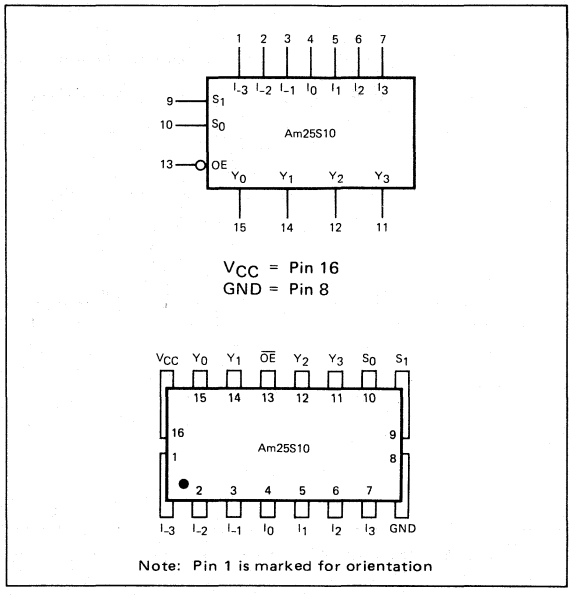


Figure 1. Logic Symbol and Connection Diagram.

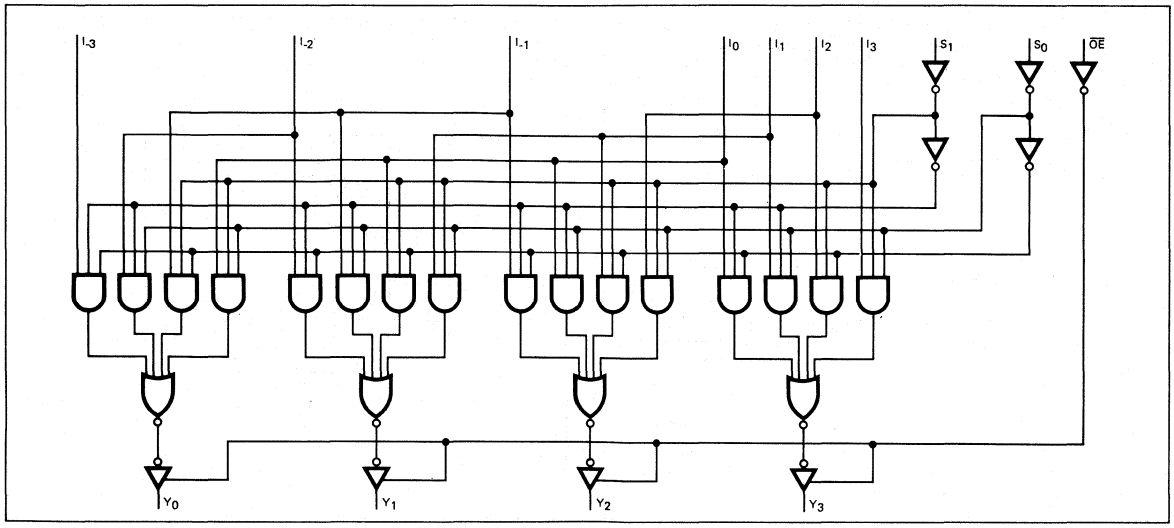


Figure 2. Logic Diagram of the Am25S10.

The operation of the Am25S10 is pictorially depicted in Figure 3. Here, the four shift positions of the data outputs with respect to the data inputs are shown via the dashed lines for the four possible select codes. Figure 4 shows a similiar operation only the notation now represents a seven-bit input word A_0 through A_6. The output code for each of the select field combinations applied to the S_0 and S_1 inputs is shown in the accompanying Function Table. In addition, the four outputs Y_0 through Y_3 can be forced to the high-impedance state by applying a HIGH to the "output control" input. This allows additional shifters to be cascaded on the same output lines, or the shifter array to be connected to a common data bus.

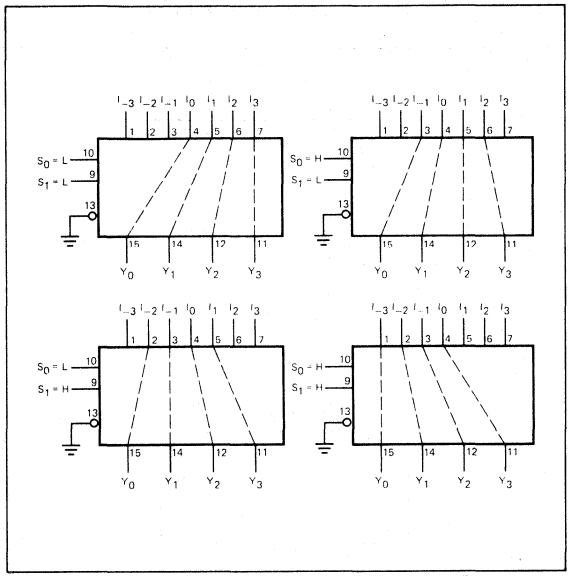
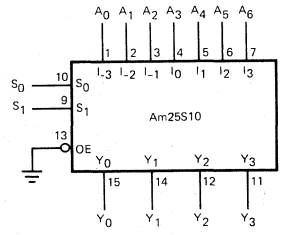


Figure 3. The Four Shift Positions of the Am25S10.



FUNCTION TABLE

S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	A_3	A_4	A_5	A_6
0	1	A_2	A_3	A_4	A_5
1	0	A_1	A_2	A_3	A_4
1	1	A_0	A_1	A_2	A_3

Positive Logic

Figure 4. The Am25S10 4-Bit Shifter Operation.

INPUT LOADING

The logic diagram of Figure 2 shows the input connection scheme for the seven data inputs of the Am25S10. Table I shows the number of multiplexer inputs connected to each data input as well as the expected an actual Unit Load weighting on each input.

TABLE I

Pin #	Data Input	Number of Multiplexer Inputs Connected	Expected Unit Loads	Actual Unit Loads
1	I_{-3}	1	1	1
2	I_{-2}	2	2	1.5
3	I_{-1}	3	3	1.5
4	I_0	4	4	1.5
5	I_1	3	3	1.5
6	I_2	2	2	1.5
7	I_3	1	1	1

Since the number of gate inputs for I_{-2}, I_{-1}, I_0, I_1 and I_2 data inputs is 2, 3, 4, 3, and 2 respectively, this could be expected to be the unit load fan-in for these data inputs. However, I_{IL} current sharing occurs internally with the select buffer outputs to reduce the external fan-in. Since a Schottky TTL unit load is defined as −2.0mA measured at 0.5V LOW, the maximum I_{IL} when measured at V_{IL} = 0.5V is −3mA or 1.5 STTL unit loads. As the measure voltage V_{IL} on these data inputs is decreased to 0V, the measured input current on I_{-2}, I_{-1}, I_0, I_1, and I_2 can increase to an I_{IL} maximum of −4, −6, −8, −6 and −4 mA respectively because of the decrease in current sharing with the internal select buffer outputs.

A plot of the typical input voltage versus input current for the data inputs is shown in Figure 5. This Figure shows the increased input current flow (negative current) as the input voltage is decreased. It also shows the effect of the input clamp diode as forward bias in applied.

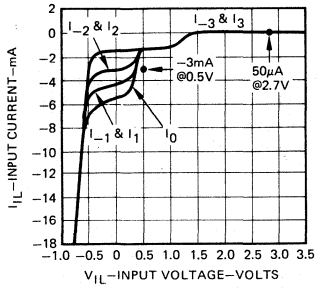
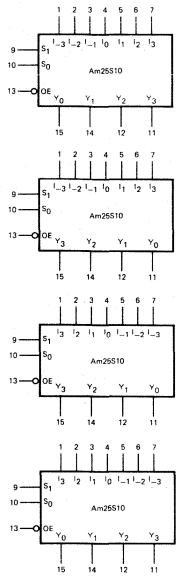


Figure 5. Typical Input Current Characteristics.

LOGIC EQUIVALENTS OF THE Am25S10

The Am25S10 exhibits several symmetrical properties that may be of advantage in some designs. These symmetrical properties involve the labeling of the inputs and outputs and the polarity of the select inputs. By relabeling the inputs in reverse order, labeling the outputs in reverse order, and considering the select inputs in positive logic (active-HIGH) or negative logic (active-LOW), eight logic equivalents for the device are possible. Figure 6 shows the operation of the device for the four combinations of input and output definitions for the positive logic notation while Figure 7 shows the operation of the device for the four combinations for the negative logic notation. The logic symbol for each set of definitions for the input pins and output pins is shown adjacent to the truth table.

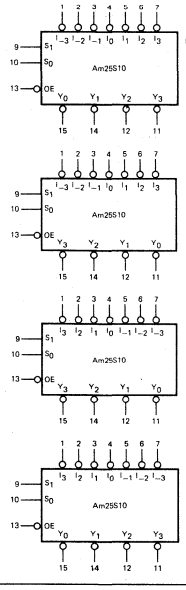
This relabeling of pins can provide the designer with some flexibility in printed circuit board layout. Likewise, the select code can be either positive logic or negative logic and the input data will be passed non-inverted. In some cases, the redefinition allows the designer to visualize shifting up versus shifting down for the same select code.



SELECT PINS		DATA INPUT PINS							DATA OUTPUT PINS			
9	10	1	2	3	4	5	6	7	11	12	14	15
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_3	Y_2	Y_1	Y_0
0	0	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
0	1	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	0	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	1	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
0	1	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	0	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	1	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_0	Y_1	Y_2	Y_3
0	0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0
0	1	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	0	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	1	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
0	0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0
0	1	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	0	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	1	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3

Positive Logic (HIGH = 1, LOW = 0) for the select inputs.

Figure 6. Four Possible Input and Output Combinations for the Positive Logic Definition.



SELECT PINS		DATA INPUT PINS							DATA OUTPUT PINS			
9	10	1	2	3	4	5	6	7	11	12	14	15
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_3	Y_2	Y_1	Y_0
0	0	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
0	1	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	0	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	1	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
0	1	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	0	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	1	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
0	0	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3
0	1	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	0	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	1	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_0	Y_1	Y_2	Y_3
0	0	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3
0	1	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	0	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	1	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0

Negative Logic (LOW = 1, HIGH = 0) for the select inputs.

Figure 7. Four Possible Input and Output Combinations for the Negative Logic Definition.

Am25S10 APPLICATIONS

The four-bit shifter is an ideal MSI element for high-speed shifting and scaling in digital systems. By suitable interconnection of the inputs and outputs, shifts of any number of places up or down can be made with a propagation delay of only one device. Shifting can be logical, with zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop. The three-state outputs can be used to increase the number of places shifted and also facilitate rapid data bus access in bus organized systems.

The Connection Diagram and Function Table of Figure 8 show a 16-bit word shifted up 0, 1, 2 or 3 places. In this example, the most significant bits (A_{13}, A_{14}, A_{15}) are discarded and logic zeroes are shifted in at the least significant end.

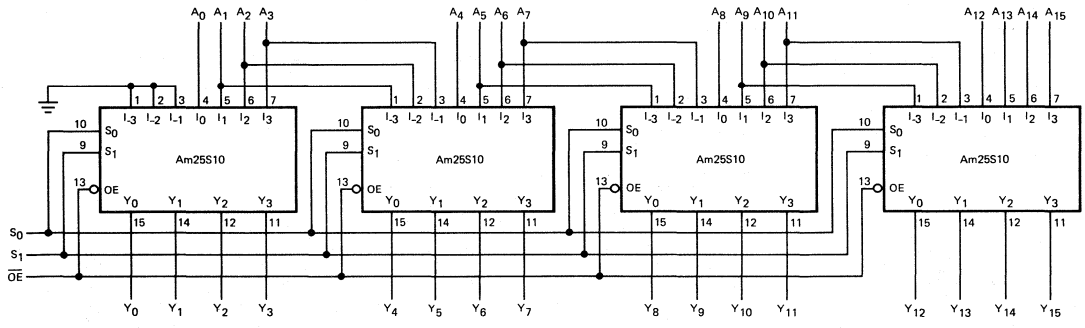
Figure 9 shows a Connection Diagram and Function Table for a 12-bit word shifted down 0, 1, 2 or 3 places. In this example, zeroes are shifted into the most significant bits and the least significant bits are discarded. Notice that one of the alternate definitions and pin assignments has been used to define the Am25S10.

A complete end-around barrel shift of 0, 1, 2, 3, 4, 5, 6 or 7 places is shown in Figure 10. In this configuration, the three-state capability of the outputs is used to connect one of two Am25S10's to the data output under the control of the S_2 and $\overline{S}_2$ select inputs. This technique can be expanded for longer word lengths by using one-of-four or one-of-eight decoders to control the active-LOW "output control" input.

A 13-bit two's complement scaler is shown in Figure 11. For this connection, the sign bit is pulled in at the most significant end and the least significant bits are truncated. Thus, the 13-bit two's complement binary output number is scaled to 1, 1/2, 1/4, or 1/8 of its input value.

A two-level 16-bit barrel shifter and its associated Function Table are shown in Figure 12. Only eight Am25S10's are required to perform this function. For clarity, the intermediate level of inputs and outputs have been labeled B_i. The sixteen-bit output word can be bus connected and controlled via the $\overline{OE}$ input.

Figure 13 demonstrates a unique way to convert a fixed point positive number to a floating-point mantisa and exponent. The priority encoder is used to determine the most significant bit position of the input word with a binary "1". The priority encoder output is a binary weighted code representing the number of places the input word is to be shifted up. This code controls the Am25S10 shifting array and shifts the input word such that the Y_7-bit of the mantisa is always a binary one (except for A = 0). The exponent is of the form 2^{-n} where n is the value of the binary weighted code from the priority encoder. Thus, the output of this functional block is of the form $Y2^{-n}$.

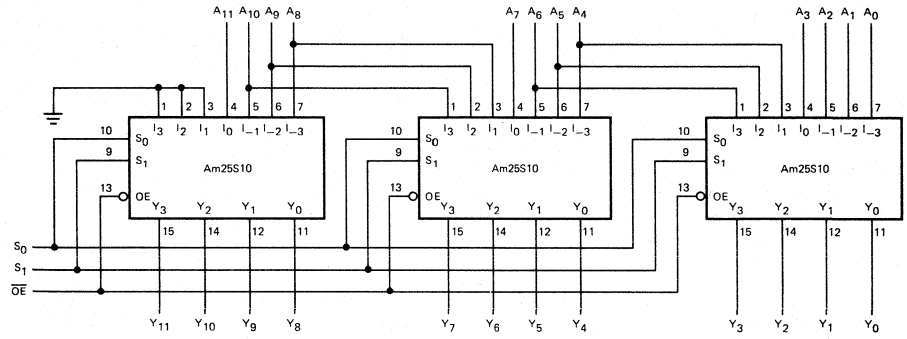


FUNCTION TABLE

S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
0	1	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}
1	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}
1	1	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}

Positive Logic

Figure 8. 16-Bit Shift-Up 0, 1, 2 or 3 Places.

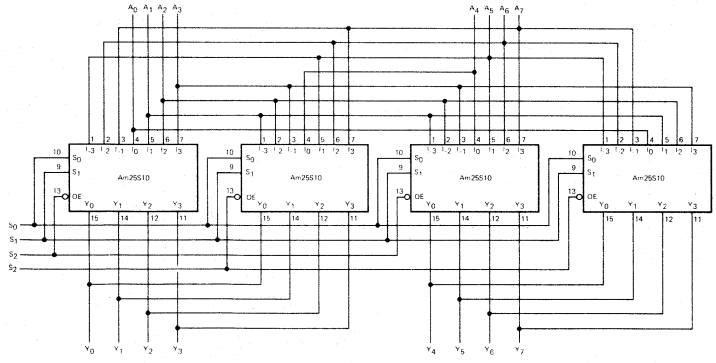


FUNCTION TABLE

S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}
0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}
0	1	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	0
1	0	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	0	0
1	1	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	0	0	0

Positive Logic (Alternate Definitions)

Figure 9. 12-Bit Shift-Down 0, 1, 2 or 3 Places.

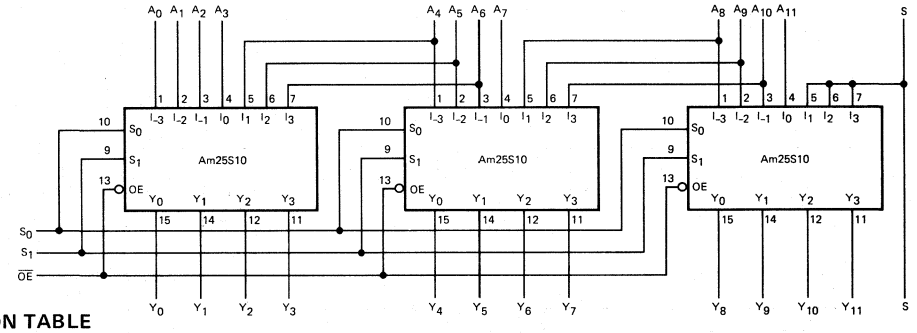


FUNCTION TABLE

S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
0	0	1	A_7	A_0	A_1	A_2	A_3	A_4	A_5	A_6
0	1	0	A_6	A_7	A_0	A_1	A_2	A_3	A_4	A_5
0	1	1	A_5	A_6	A_7	A_0	A_1	A_2	A_3	A_4
1	0	0	A_4	A_5	A_6	A_7	A_0	A_1	A_2	A_3
1	0	1	A_3	A_4	A_5	A_6	A_7	A_0	A_1	A_2
1	1	0	A_2	A_3	A_4	A_5	A_6	A_7	A_0	A_1
1	1	1	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_0

Positive Logic

Figure 10. Eight-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6 or 7 Places.

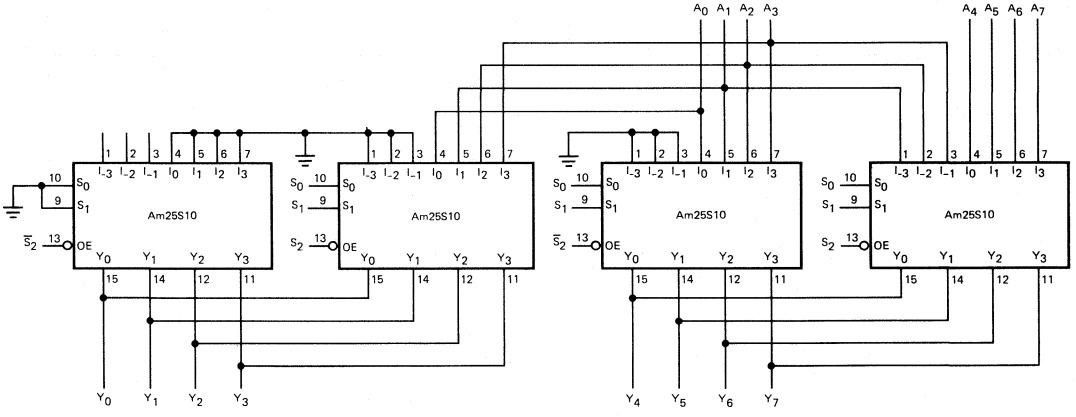


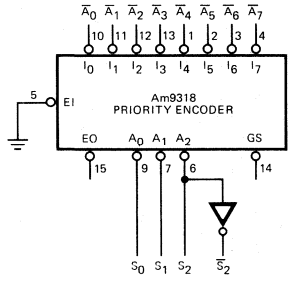
FUNCTION TABLE

SCALE	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	S
1/8	0	0	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S	S	S	S
1/4	0	1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S	S	S
1/2	1	0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S	S
1	1	1	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S

Positive Logic

Figure 11. 13-Bit 2's Complement Scaler.



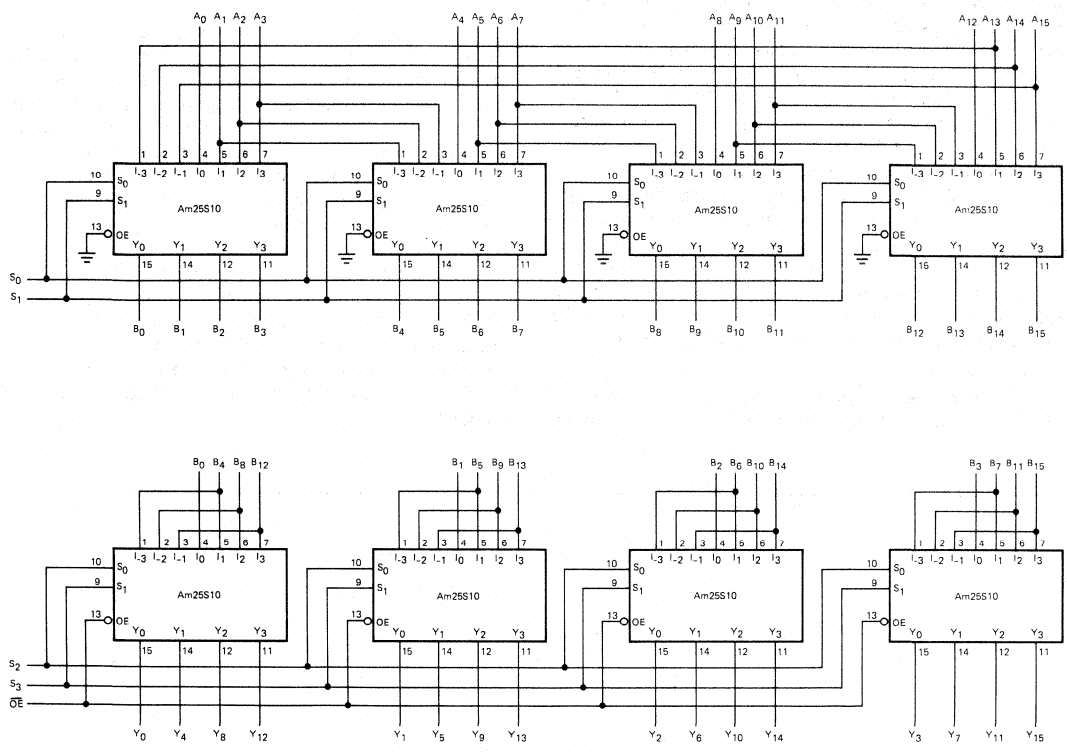


FUNCTION TABLE

EXPONENT			MANTISSA							
S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
0	0	1	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6
0	1	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5
0	1	1	0	0	0	A_0	A_1	A_2	A_3	A_4
1	0	0	0	0	0	0	A_0	A_1	A_2	A_3
1	0	1	0	0	0	0	0	A_0	A_1	A_2
1	1	0	0	0	0	0	0	0	A_0	A_1
1	1	1	0	0	0	0	0	0	0	A_0

Positive Logic

Figure 13. Binary Scaling to Give Mantissa and Exponent.



FUNCTION TABLE

S_3	S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
0	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
0	0	0	1	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}
0	0	1	0	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}
0	0	1	1	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}
0	1	0	0	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}
0	1	0	1	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}
0	1	1	0	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9
0	1	1	1	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8
1	0	0	0	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
1	0	0	1	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6
1	0	1	0	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5
1	0	1	1	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4
1	1	0	0	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3
1	1	0	1	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2
1	1	1	0	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1
1	1	1	1	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0

Positive Logic

Figure 12. Full 16-Bit Barrel Shifter.

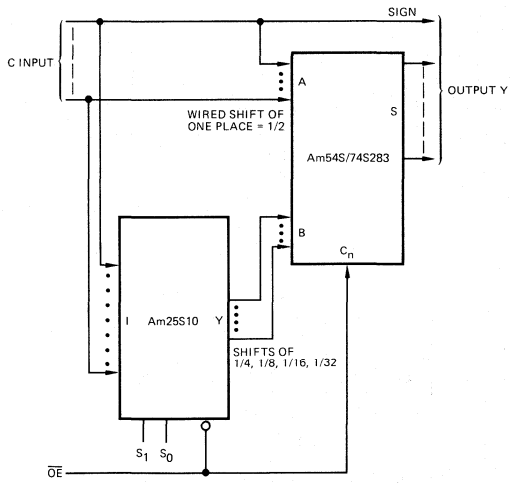
FIXED MULTIPLIERS

Digital systems requiring multiplication by a constant interger or constant fraction can make effective use of the Am25S10 if the constant must be varied over several values. By using four-bit shifters and high-speed adders, very high-speed "constant coefficient" or fixed multipliers can be built. The technique is shown diagrammatically in Figure 14. Here, the input word C is wired to the adder A inputs such that a shift of $\frac{1}{2}$ C is "built-in". The Am25S10 shifter is wired to the B inputs of the adder such that its four select states represent prescaling of $\frac{1}{4}$C, $\frac{1}{8}$C, $\frac{1}{16}$C, and $\frac{1}{32}$C of the C input word. If the $\overline{OE}$ input is used to disable the outputs (high impedance), the adder B inputs will assume the logical one state (HIGH). By adding a "one" at the adder carry input least significant end, the contribution of the B inputs to the sum output is zero and the adder A input will be passed to the output. Thus, the $\overline{OE}$ input can be used to generate a zero C value from the shifter.

Figure 15 shows the actual connection diagram for a 12-bit two's complement fixed multiplier using the scheme of Figure 14. The Y output weighting is the same as shown in the Function Table of Figure 14. The $\overline{OE}$ input is tied directly to the adder least significant C_n input to complete the shifter "zero" output function.

Figure 16 shows two shifter arrays used in conjunction with one adder. For the shifter A and shifter B select codes shown, twenty multiplication constants are realized with seventeen constants being unique. Other combinations could be used to realize different outputs. The combinations possible can be extended greatly by using multiple adders and multiple shifting arrays. For the example of Figure 16, the zero shifter output (high-impedance state) is used with only one shifter since only one C_n input is available.

This technique for fixed constant multipliers can be applied to two's complement, one's complement, sign-magnitude, or magnitude only arithmetic. In so doing, the sign must be handled appropriately and the adder output word size and number range must be considered. For the one's complement case, the all ones representation for zero must be handled separately.



FUNCTION TABLE

			4-BIT SHIFTER		A INPUT OF ADDER	OUTPUT Y
$\overline{OE}$	S_1	S_0	#SHIFTS	B INPUT OF ADDER		
0	0	0	Two	$\frac{1}{4}$C	$\frac{1}{2}$C	$\frac{3}{4}$C
0	0	1	Three	$\frac{1}{8}$C	$\frac{1}{2}$C	$\frac{5}{8}$C
0	1	0	Four	$\frac{1}{16}$C	$\frac{1}{2}$C	$\frac{9}{16}$C
0	1	1	Five	$\frac{1}{32}$C	$\frac{1}{2}$C	$\frac{17}{32}$C
1	X	X	Hi-Z	0C	$\frac{1}{2}$C	$\frac{1}{2}$C

Positive Logic

Figure 14. Parallel "Constant Coefficient" Multiplier Block Diagram and Function Table.

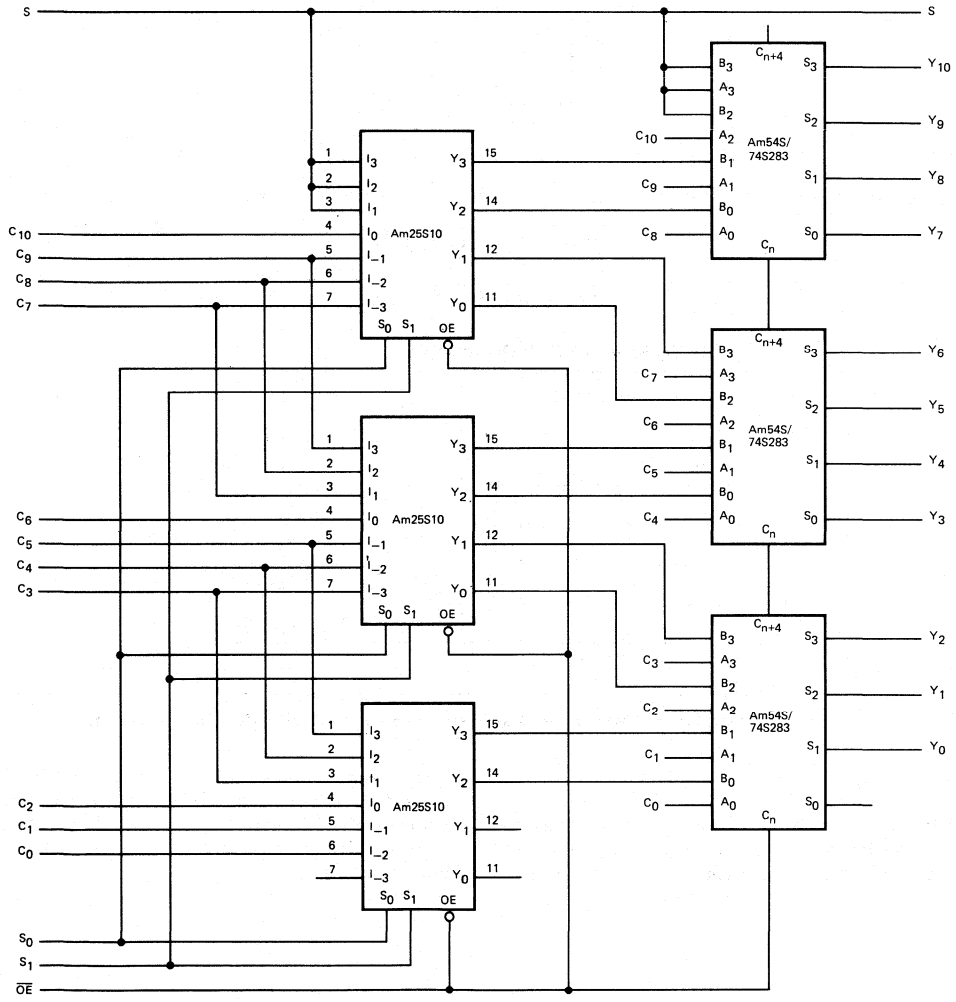
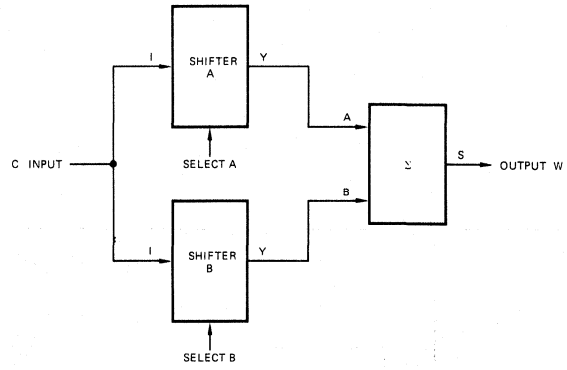


Figure 15. 12-Bit 2's Complement "Constant Coefficient" Multiplier.



SHIFTER A = $C, \frac{C}{2}, \frac{C}{4}, \frac{C}{8}$

SHIFTER B = $\frac{C}{4}, \frac{C}{8}, \frac{C}{16}, \frac{C}{32}, 0$

FIXED MULTIPLIER OUTPUT W

SHIFTER A \ SHIFTER B	$\frac{C}{4}$	$\frac{C}{8}$	$\frac{C}{16}$	$\frac{C}{32}$	0
C	$\frac{5}{4}C$	$\frac{9}{8}C$	$\frac{17}{16}C$	$\frac{33}{32}C$	C
$\frac{C}{2}$	$\frac{3}{4}C$	$\frac{5}{8}C$	$\frac{9}{16}C$	$\frac{17}{32}C$	$\frac{1}{2}C$
$\frac{C}{4}$	$\frac{1}{2}C$	$\frac{3}{8}C$	$\frac{5}{16}C$	$\frac{9}{32}C$	$\frac{1}{4}C$
$\frac{C}{8}$	$\frac{3}{8}C$	$\frac{1}{4}C$	$\frac{3}{16}C$	$\frac{5}{32}C$	$\frac{1}{8}C$

Figure 16. Two Shifter Arrays and One Adder Array in a Fixed Multiplier Connection.

CONCLUSION

The Am25S10 four-bit shifter is a new unique combinatorial logic element offering the system designer new shifting and scaling capability not previously available in a single package. The three-state output design of the Am25S10 provides increased flexibility in its use and the advanced Schottky construction offers minimum propagation delay. The device can be used to shift any number of bits any number of places; up, down or end-around.

Am25S18

Quad D Register With Standard And Three-State Outputs

3

Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am25S18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

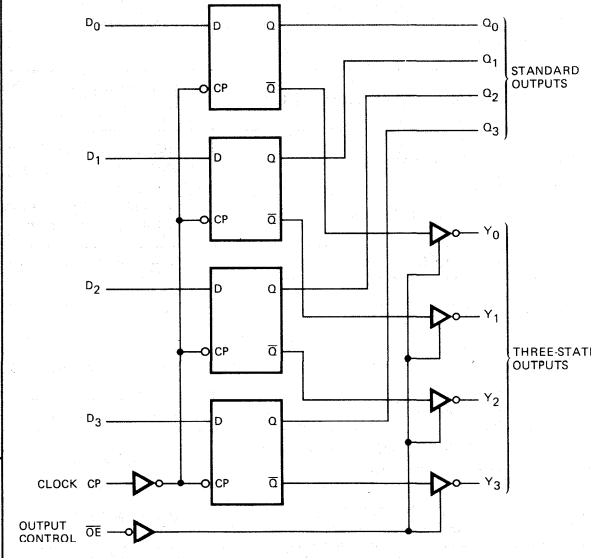
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25S18 is a 4-bit, high speed Schottky register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25S18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

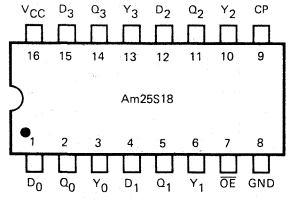
LOGIC DIAGRAM



ORDERING INFORMATION

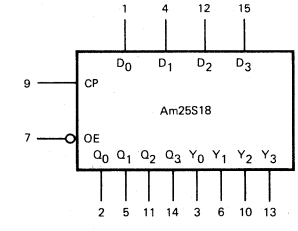
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25S18PC
Hermetic DIP	0°C to +70°C	AM25S18DC
Dice	0°C to +70°C	AM25S18XC
Hermetic DIP	–55°C to +125°C	AM25S18DM
Hermetic Flat Pak	–55°C to +125°C	AM25S18FM
Dice	–55°C to +125°C	AM25S18XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5
DC Output Current, Into Outputs	30m
DC Input Current	−30mA to +5.0m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S18XC T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am25S18XM T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1mA MIL	2.5	3.4		Volts
				I_{OH} = −1mA COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	µA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V, R_L = 280Ω)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output		C_L = 15pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)				6.0	9.0	ns
t_{PHL}					8.5	13	
t_{ZH}	Output Control to Output		C_L = 15pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			C_L = 5.0pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15pF	75	100		MHz

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

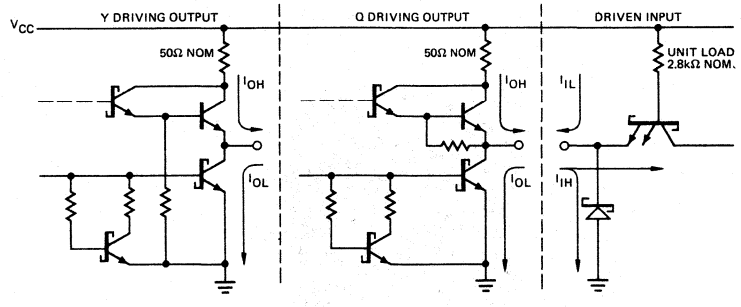
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

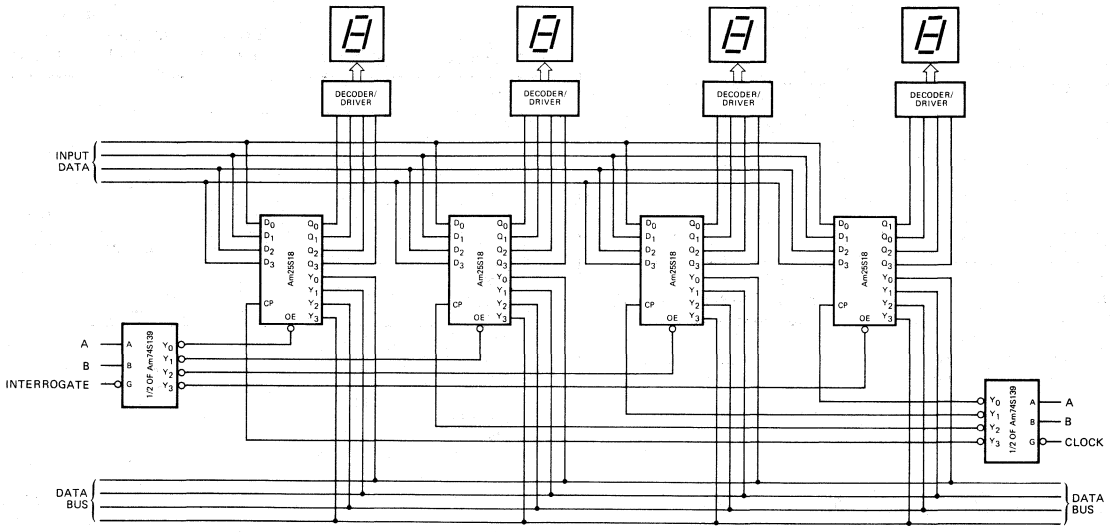
*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

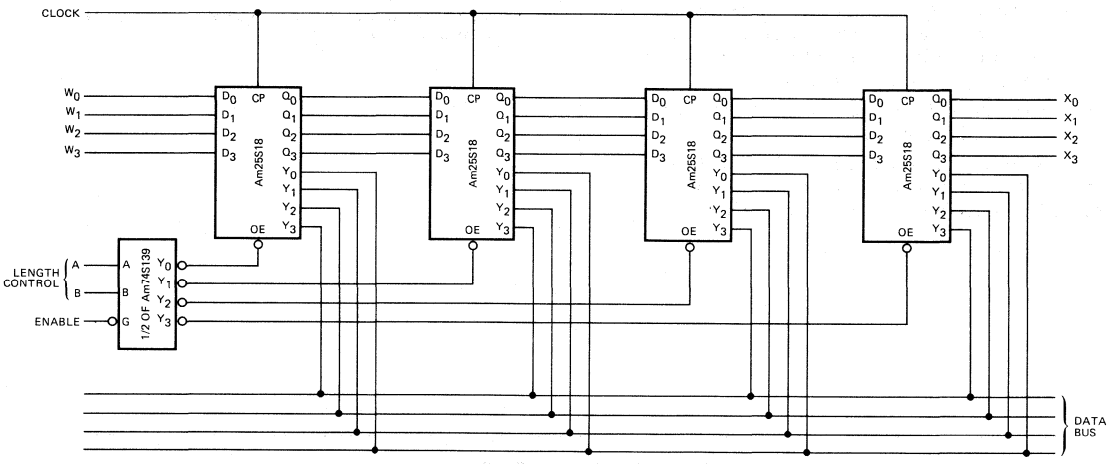


Note: Actual current flow direction shown.

APPLICATIONS

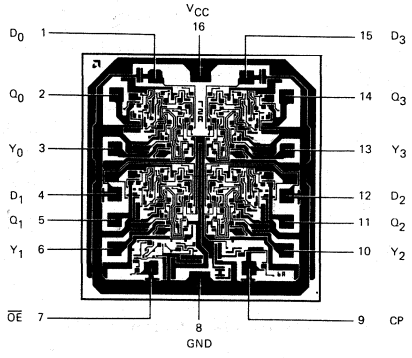


THE Am25S18 USED AS DISPLAY REGISTER WITH BUS INTERROGATE CAPABILITY.



THE Am25S18 AS A VARIABLE LENGTH (1, 2, 3 or 4 WORD) SHIFT REGISTER.

Metallization and Pad Layout



DIE SIZE
0.077" X 0.079"

Am25S240 • Am25S241 • Am25S244
Am54S/74S240 • Am54S/74S241 • Am54S/74S244
Octal Buffers/Line Drivers/Line Receivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Advanced Schottky processing
- Hysteresis at inputs improve noise margin
- PNP inputs reduce DC loading on bus lines
- V_{OL} of 0.55V at 64mA for COM'L; 48mA for MIL
- Data-to-output propagation delay times:
  - Inverting – 7.0ns max
  - Non-inverting – 9.0ns max
- Enable-to-output – 15.0ns max
- 100% reliability assurance testing in compliance with MIL-STD-883

Note

- Am25S240/241/244 have up to 40% lower I_{CC} than 54S/74S versions

FUNCTIONAL DESCRIPTION

These buffers/line drivers, used as memory-address drivers, clock drivers and bus oriented transmitters/receivers, provide improved PC board density. The outputs of the commercial temperature range versions have 64mA sink and 15mA source capability, which can be used to drive terminated lines down to 133Ω. The outputs of the military temperature range versions have 48mA sink and 12mA source current capability.

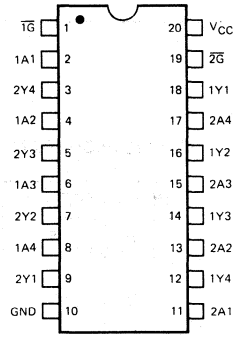
Featuring 0.2V minimum guaranteed hysteresis at each low-current PNP data input, they provide impoved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely.

The Am25S/54S/74S240, Am25S/54S/74S241 and Am25S/54S/74S244 have four buffers which are enabled from one common line, and the other four buffers are enabled from another common line. The Am25S/54S/74S240 is inverting, while the Am25S/54S/74S241 and Am25S/54S/74S244 present true data at the outputs.

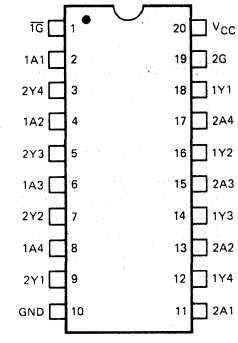
Am25S versions feature 30 to 60% lower I_{CC} – a significant reduction in system power consumption where multiple devices are used per system.

CONNECTION DIAGRAMS
Top Views

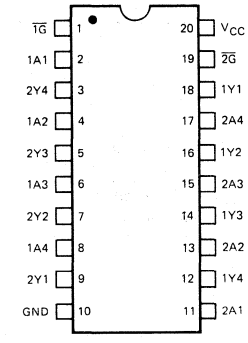
Am25S/54S/74S240



Am25S/54S/74S241



Am25S/54S/74S244



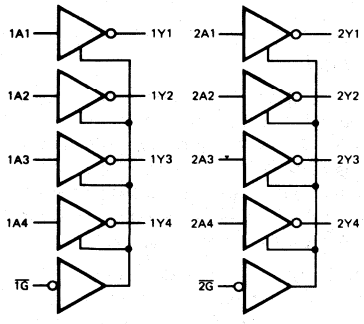
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

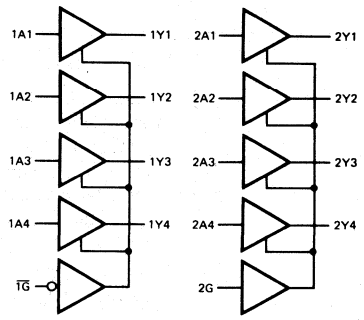
Package Type	Temperature Range	Order Number Am25S240/241/244	Am54S/74S240	Am54S/74S241	Am54S/74S244
Hermetic	−55 to +125°C	AM25S240/241/244DM	SN54S240J	SN54S241J	SN54S244J
Dice	−55 to +125°C	AM25S240/241/244XM	AM54S240X	AM54S241X	AM54S244X
Hermetic	0 to 70°C	AM25S240/241/244DC	SN74S240J	SN74S241J	SN74S244J
Molded	0 to 70°C	AM25S240/241/244PC	SN74S240N	SN74S241N	SN74S244N
Dice	0 to 70°C	AM25S240/241/244XC	AM74S240X	AM74S241X	AM74S244X

LOGIC DIAGRAMS

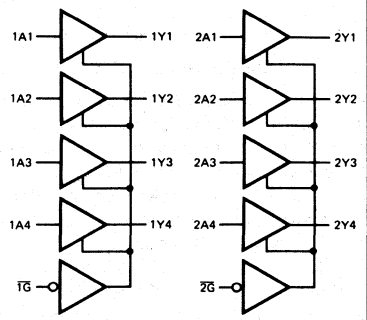
Am25S/54S/74S240



Am25S/54S/74S241



Am25S/54S/74S244



Note: All gates have input hysteresis.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current	150mA
DC Input Current	−30 to +5.0mA

FUNCTION TABLES

Am25S/54S/74S240

INPUTS		OUTPUT
G	A	Y
H	X	Z
L	H	L
L	L	H

Am25S/54S/74S241

INPUTS			OUTPUT
1G	2G	A	Y
H	L	X	Z
L	H	H	H
L	H	L	L

Am25S/54S/74S244

INPUTS		OUTPUT
G	A	Y
H	X	Z
L	H	H
L	L	L

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am25S/54S240/241/244 (MIL)	T_A = −55 to +125°C	V_{CC}(MIN) = 4.50V	V_{CC}(MAX) = 5.50V
Am25S/74S240/241/244 (COM'L)	T_A = 0 to 70°C	V_{CC}(MIN) = 4.75V	V_{CC}(MAX) = 5.25V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description			Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{IH}	High Level Input Voltage					2.0			Volts
V_{IL}	Low-Level Input Voltage							0.8	Volts
V_{IK}	Input Clamp Voltage			V_{CC} = MIN, I_I = −18mA				−1.2	Volts
	Hysteresis (V_{T+} − V_{T-})			V_{CC} = MIN		0.2	0.4		Volts
V_{OH}	High-Level Output Voltage			V_{CC} = MIN, V_{IL} = 0.8V	COM'L, I_{OH} = −1mA	2.7			Volts
					I_{OH} = −3mA	2.4	3.4		
				V_{CC} = MIN, V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
					COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage			V_{CC} = MIN, V_{IH} = 0.8V	MIL, I_{OL} = 48mA			0.55	Volts
					COM'L, I_{OL} = 64mA			0.55	
I_{OZH}	Off-State Output Current, High-Level Voltage Applied			V_{CC} = MAX, V_{IH} = 2.0V, V_{IL} = 0.8V	V_O = 2.4V			50	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied				V_O = 0.5V			−50	
I_I	Input Current at Maximum Input Voltage			V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	High-Level Input Current, Any Input			V_{CC} = MAX, V_{IH} = 2.7V				50	μA
I_{IL}	Low-Level Input Current		Any A	V_{CC} = MAX, V_{IL} = 0.5V				−400	μA
			Any G					−2.0	mA
I_{OS}	Short-Circuit Output Current (Note 3)			V_{CC} = MAX		−50		−225	mA
I_{CC}	Supply Current	Am54S/74S240	All Outputs HIGH	V_{CC} = MAX, Outputs open	MIL			123	mA
					COM'L			135	
			All Outputs LOW		MIL			145	
					COM'L			150	
			Outputs at Hi-Z		MIL			145	
					COM'L			150	
		Am54S/74S241 Am54S/74S244	All Outputs HIGH	V_{CC} = MAX, Outputs open	MIL			147	mA
					COM'L			160	
			All Outputs LOW		MIL			170	
					COM'L			180	
			Outputs at Hi-Z		MIL			170	
					COM'L			180	
		Am25S240	All Outputs HIGH	V_{CC} = MAX, Outputs open	MIL and COM'L		37	65	mA
			All Outputs LOW				59	90	
			Outputs at Hi-Z				69	105	
		Am25S241 Am25S244	All Outputs HIGH	V_{CC} = MAX, Outputs open	MIL and COM'L		37	65	mA
			All Outputs LOW				63	105	
			Outputs at Hi-Z				72	120	

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = +25°C)

Parameter	Description	Test Conditions	Am54S/74S240 Min	Am54S/74S240 Typ	Am54S/74S240 Max	Am54S/74S241/244 Min	Am54S/74S241/244 Typ	Am54S/74S241/244 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 50pF, R_L = 90Ω (Note 3)		4.5	7.0		6.0	9.0	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			4.5	7.0		6.0	9.0	ns
t_{ZL}	Output Enable Time to Low Level			10	15		10	15	ns
t_{ZH}	Output Enable Time to High Level			6.5	10		8.0	12	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0pF, R_L = 90Ω (Note 3)		10	15		10	15	ns
t_{HZ}	Output Disable Time from High Level			6.0	9.0		6.0	9.0	ns
t_{LZ}	Output Disable Time	C_L = 50pF, R_L = 90Ω (Note 3)			18			18	ns
t_{HZ}									

Am25S ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE

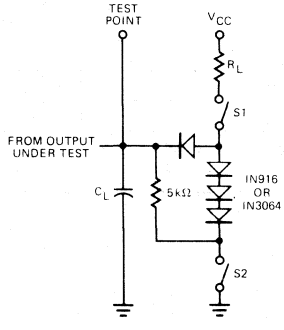
Parameter	Description	Am25S240 COM'L T_A = 0 to 70°C, V_{CC} = 5.0V ±5% Min	Am25S240 COM'L Max	Am25S240 MIL T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Min	Am25S240 MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay Data Input to Output		7.5		9	ns	C_L = 50pF, R_L = 90Ω
t_{PHL}			7		9		
t_{ZL}	Output Enable Time to LOW		16		18	ns	
t_{ZH}	Output Enable Time to HIGH		13		13		
t_{LZ}	Output Disable Time from LOW		16		18	ns	C_L = 5.0pF, R_L = 90Ω
t_{HZ}	Output Disable Time from HIGH		10		12		

Am25S ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE

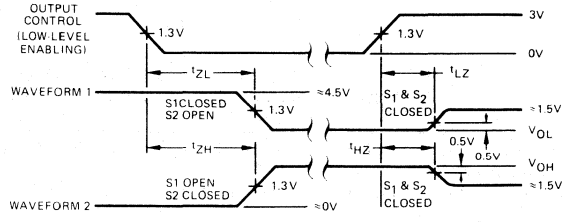
Parameter	Description	Am25S241/244 COM'L T_A = 0 to 70°C, V_{CC} = 5.0V ±5% Min	Am25S241/244 COM'L Max	Am25S241/244 MIL T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Min	Am25S241/244 MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay Data Input to Output		10.5		12	ns	C_L = 50pF, R_L = 90Ω
t_{PHL}			10.5		12		
t_{ZL}	Output Enable Time to LOW		16*		18*	ns	
t_{ZH}	Output Enable Time to HIGH		13*		13*		
t_{LZ}	Output Disable Time from LOW		16*		18*	ns	C_L = 5.0pF, R_L = 90Ω
t_{HZ}	Output Disable Time from HIGH		10*		12*		

*Note: Am25S241, add 3ns for 2G enable.

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



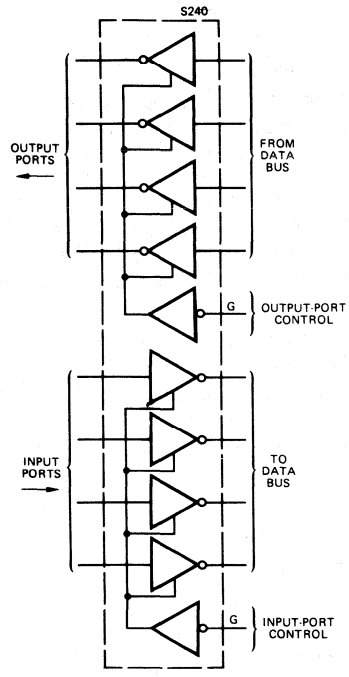
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



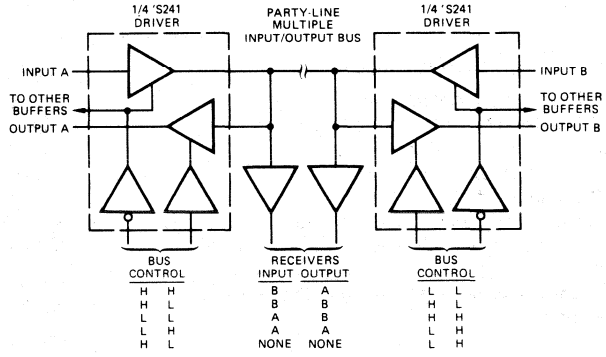
Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.

APPLICATIONS

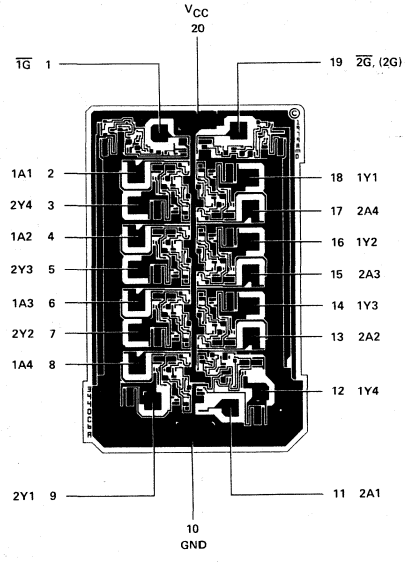
INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS AND RECEIVERS



Metallization and Pad Layout



DIE SIZE 0.059" X 0.091"

Am25S373 • Am54S/74S373
Am25S533 • Am54S/74S533

Octal Latches with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 8-bit, high-speed parallel latches
- Am25S/54S/74S373 has non-inverting inputs
- Am25S/54S/74S533 has inverting inputs
- V_{OL} = 0.5V (max) at I_{OL} = 20mA
- Am25S versions with I_{OL} = 32mA
- Hysteresis on latch enable input for improved noise margin
- 3-state outputs interface directly with bus organized systems
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

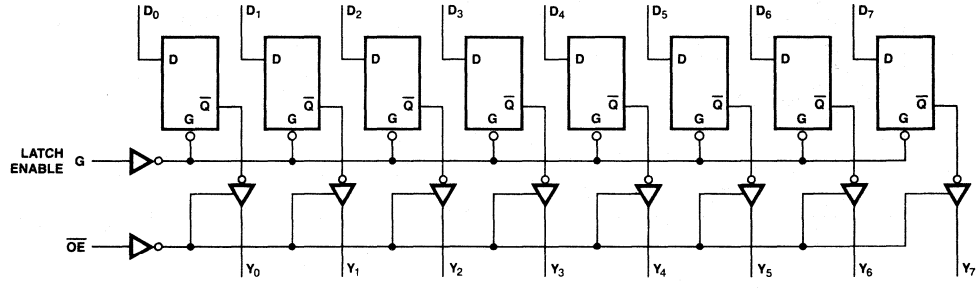
The Am25S/54S/74S373 and Am25S/54S/74S533 are octal latches with 3-state outputs for bus organized system applications. The latches appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

The 'S373 presents non-inverted data at the outputs while the 'S533 is inverting.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

Am25S373 and Am25S533 versions are also available offering V_{OL} = 0.5V (max) at I_{OL} = 32mA.

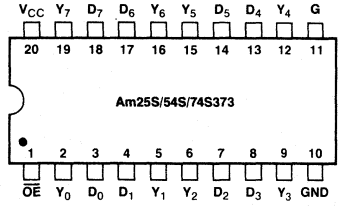
LOGIC DIAGRAM
Am25S/54S/74S373



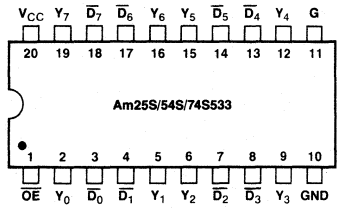
Inputs D_0 through D_7 are inverted on the Am25S/54S/74S533.

BLI-222

CONNECTION DIAGRAMS – Top Views



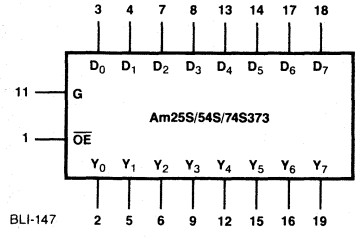
BLI-145



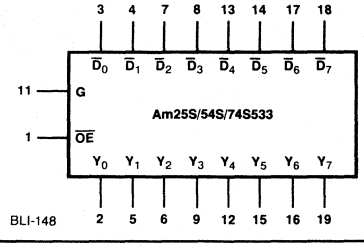
BLI-146

Note: Pin 1 is marked for orientation.

LOGIC SYMBOLS



BLI-147



BLI-148

V_{CC} = Pin 20
GND = Pin 10

Am25S373 • Am25S533
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am25S373/533XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am25S373/533XM, DM	T_A = −55 to +125°C	V_{CC} = 4.50 to 5.50V
Am25S373/533FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
				COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.45	Volts
				I_{OL} = 32mA			.5	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current		V_{CC} = MAX	V_O = 0.5V			−50	μA
				V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	'S373	V_{CC} = MAX			105	160	mA
		'S533				110	168	

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ORDERING INFORMATION

Package Type	Temperature Range	Am25S373 Order Number	Am54S/74S373 Order Number	Am25S533 Order Number	Am54S/74S533 Order Number
Molded DIP	0 to 70°C	AM25S373PC	SN74S373N	AM25S533PC	SN74S533N
Hermetic DIP	0 to 70°C	AM25S373DC	SN74S373J	AM25S533DC	SN74S533J
Dice	0 to 70°C	AM25S373XC	SN74S373X	AM25S533XC	SN74S533X
Hermetic DIP	−55 to +125°C	AM25S373DM	SN54S373J	AM25S533DM	SN54S533J
Hermetic Flat Pak	−55 to +125°C	AM25S373FM	SN54S373W	AM25S533FM	SN54S533W
Dice	−55 to +125°C	AM25S373XM	SN54S373X	AM25S533XM	SN54S533X

Am54S/74S373 • Am54S/74S533
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am54S/74S373/533XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am54S/74S373/533XM, DM	T_A = −55 to +125°C	V_{CC} = 4.50 to 5.50V
Am54S/74S373/533FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
				COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs	MIL			0.8	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current		V_{CC} = MAX	V_O = 0.5V			−50	μA
				V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	'S373	V_{CC} = MAX			105	160	mA
		'S533				110	168	

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

FUNCTION TABLES

Am25S/54S/74S373

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	D_i	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	L	Transparent
L	H	H	L	H	
L	L	X	NC	NC	Latched

Am25S/54S/74S533

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	$\overline{D_i}$	Q_i	$\overline{Y_i}$	
H	X	X	X	Z	Hi-Z
L	H	L	H	H	Transparent
L	H	H	L	L	
L	L	X	NC	NC	Latched

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

Am25S/54S/74S373

D_i The latch data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i The 3-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

Am25S/54S/74S533

$\overline{D_i}$ The latch inverting data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

$\overline{Y_i}$ The 3-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the inverted outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

Am25S/54S/74S373
SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25S/54S/74S Min	Typ	Max	Units	Test Conditions
t_{PLH}	Enable to Output		7	14	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			12	18	ns	
t_{PLH}	Data Input to Output		5	9	ns	
t_{PHL}			9	13	ns	
$t_s(H)$	HIGH Data to Enable	0			ns	
$t_s(L)$	LOW Data to Enable	0			ns	
$t_h(H)$	HIGH Data to Enable	10			ns	
$t_h(L)$	LOW Data to Enable	10			ns	
t_{pwH}	Enable Pulse Width	6			ns	
t_{pwL}		7.3			ns	
t_{ZH}	$\overline{OE}$ to Y_i		8	15	ns	
t_{ZL}			11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i		6	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}			8	12	ns	

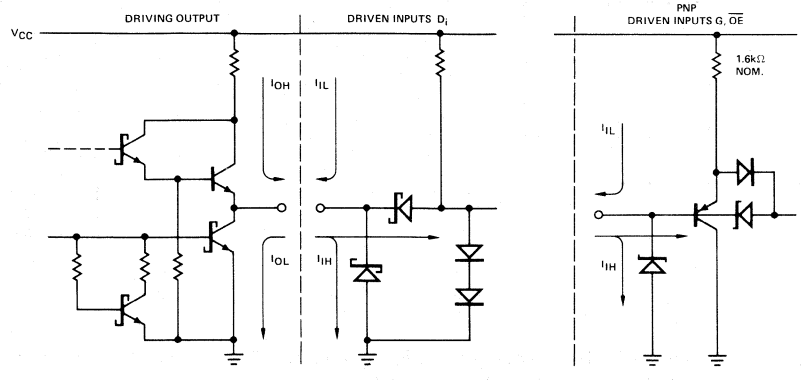
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25S/54S/74S533
SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25S/54S/74S Min	Typ	Max	Units	Test Conditions
t_{PLH}	Enable to Output		17	24	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			19	26	ns	
t_{PLH}	Data Input to Output		10	14	ns	
t_{PHL}			14	20	ns	
$t_s(H)$	HIGH Data to Enable	0			ns	
$t_s(L)$	LOW Data to Enable	0			ns	
$t_h(H)$	HIGH Data to Enable	10			ns	
$t_h(L)$	LOW Data to Enable	10			ns	
t_{pwH}	Enable Pulse Width	6			ns	
t_{pwL}		7.3			ns	
t_{ZH}	$\overline{OE}$ to Y_i		8	15	ns	
t_{ZL}			11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i		6	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}			8	10	ns	

Am25S • Am54S/74S
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

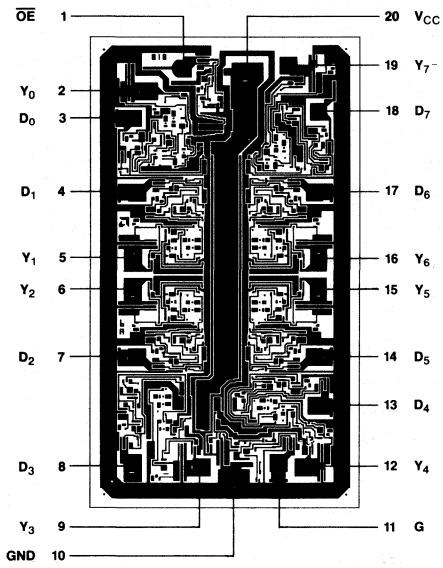


Note: Actual current flow direction shown.

BLI-149

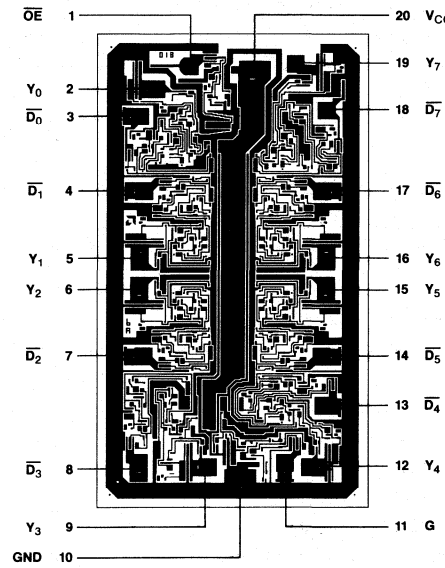
Metallization and Pad Layouts

Am25S/54S/74S373



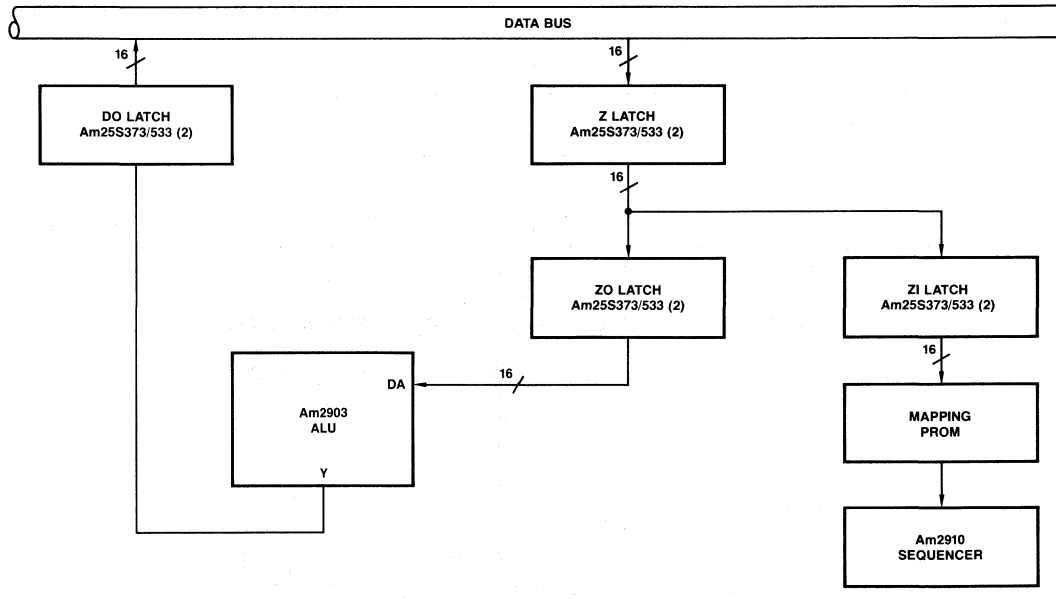
DIE SIZE 0.066" X 0.119"

Am25S/54S/74S533



DIE SIZE 0.066" X 0.119"

APPLICATION



Transparent Latches are used in high performance CPU designs. The Z Latch configuration shown provides overlapped fetch of machine instructions and operand data.

BLI-150

Am25S374 • Am54S/74S374
Am25S534 • Am54S/74S534

Octal Registers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high-speed parallel registers
- Am25S/54S/74S374 has non-inverting inputs
- Am25S/54S/74S534 has inverting inputs
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- V_{OL} = 0.5V (max) at I_{OL} = 20mA
- Am25S versions with I_{OL} = 32mA
- High-speed – Clock to output 11ns typical
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

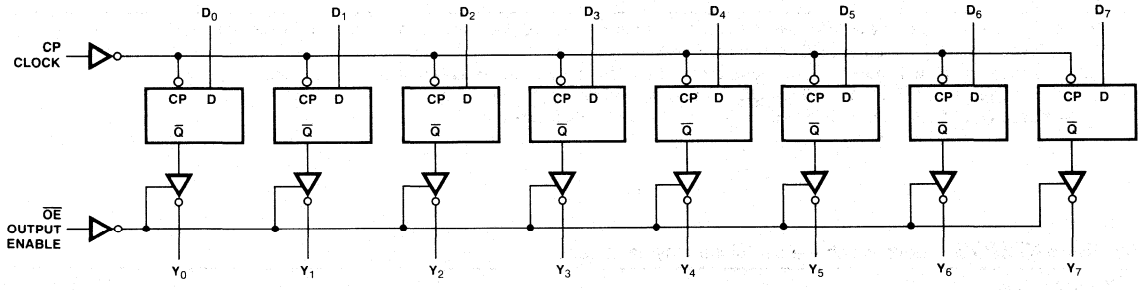
The Am25S/54S/74S374 and Am25S/54S/74S534 are eight-bit registers built using high-speed Schottky technology. The registers consist of eight D-type flip-flops with a buffered common clock and a buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

Am25S374 and Am25S534 versions are also available offering V_{OL} = 0.5V (max) at I_{OL} = 32mA.

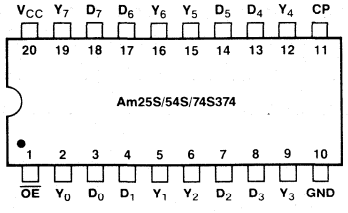
LOGIC DIAGRAM
Am25S/54S/74S374

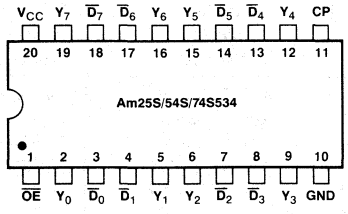


Inputs D_0 through D_7 are inverted on the Am25S/54S/74S534.

BLI-051

CONNECTION DIAGRAMS – Top Views

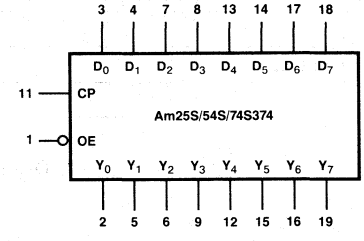


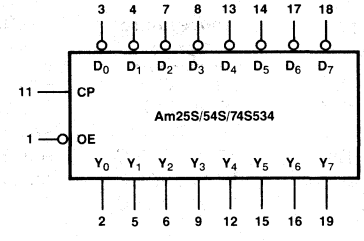


Note: Pin 1 is marked for orientation.

BLI-052

LOGIC SYMBOLS





BLI-053

V_{CC} = Pin 20
GND = Pin 10

Am25S374 • Am25S534
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am25S374/534XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am25S374/534XM, DM	T_A = −55 to +125°C	V_{CC} = 4.50 to 5.50V
Am25S374/534FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.45	Volts
			I_{OL} = 32mA			.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0,5V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			90	140	mA

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. 'S374 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.
   'S534 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ORDERING INFORMATION

Package Type	Temperature Range	Am25S374 Order Number	Am54S/74S374 Order Number	Am25S534 Order Number	Am54S/74S534 Order Number
Molded DIP	0 to 70°C	Am25S374PC	SN74S374N	Am25S534PC	SN74S534N
Hermetic DIP	0 to 70°C	Am25S374DC	SN74S374J	Am25S534DC	SN74S534J
Dice	0 to 70°C	Am25S374XC	SN74S374X	Am25S534XC	SN74S534X
Hermetic DIP	−55 to +125°C	Am25S374DM	SN54S374J	Am25S534DM	SN54S534J
Hermetic Flat Pak	−55 to +125°C	Am25S374FM	SN54S374W	Am25S534FM	SN54S534W
Dice	−55 to +125°C	Am25S374XM	SN54S374X	Am25S534XM	SN54S534X

Am54S/74S374 • Am54S/74S534
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am54S/74S374/534XC, DC, PC	T_A = 0 to +70°C	V_{CC} = 4.75 to 5.25V
Am54S/74S374/534XM, DM	T_A = −55 to +125°C	V_{CC} = 4.50 to 5.50V
Am54S/74S374/534FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.8	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.5V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			90	140	mA

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. 'S374 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.
   'S534 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs ('S374, non-inverting).

$\overline{D_i}$ The D flip-flop data inputs ('S534, inverting).

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Y_i The register three-state outputs ('S374, non-inverting).

$\overline{OE}$ Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

FUNCTION TABLE

Function	Inputs				Internal	Outputs
	$\overline{OE}$	Clock	'S374 D_i	'S534 $\overline{D_i}$	Q_i	Y_i
Hi-Z	H	L	X	X	NC	Z
	H	H	X	X	NC	Z
LOAD REGISTER	L	↑	L	H	L	L
	L	↑	H	L	H	H
	H	↑	L	H	L	Z
	H	↑	H	L	H	Z

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance
↑ = LOW-to-HIGH transition

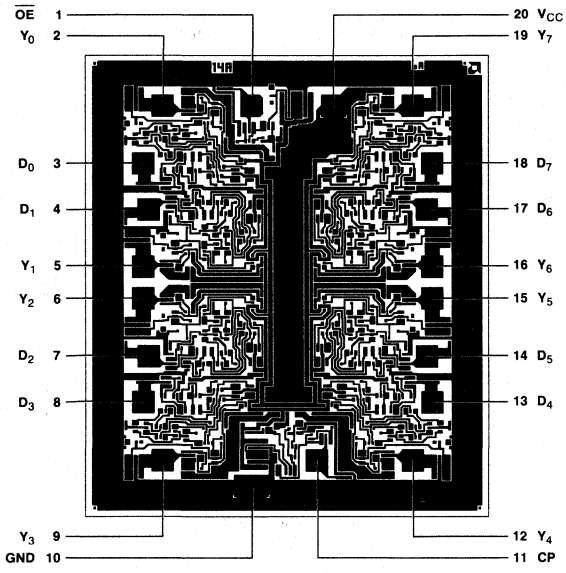
Am25S/54S/74S374/534
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Am25S/54S/74S Min	Typ	Max	Units	Test Conditions
t_{PLH}	Clock to Output, Y_i			8	15	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}				11	17	ns	
t_{ZH}	$\overline{OE}$ to Y_i			8	15	ns	
t_{ZL}				11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i			5	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}				7	12	ns	
t_{PW}	Clock Pulse Width	HIGH	6			ns	C_L = 15pF, R_L = 280Ω
		LOW	7.3			ns	
t_S	Data to Clock		5			ns	
t_H			2			ns	
f_{max}	Maximum Clock Frequency (Note 1)		75	100		MHz	

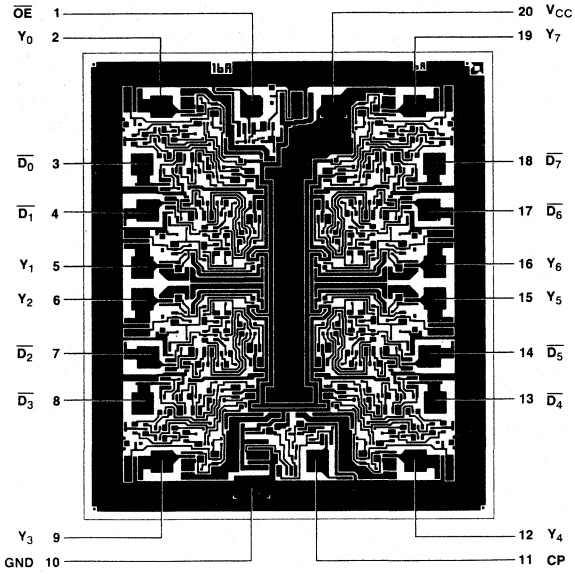
Note: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Metallization and Pad Layouts

Am25S/54S/74S374

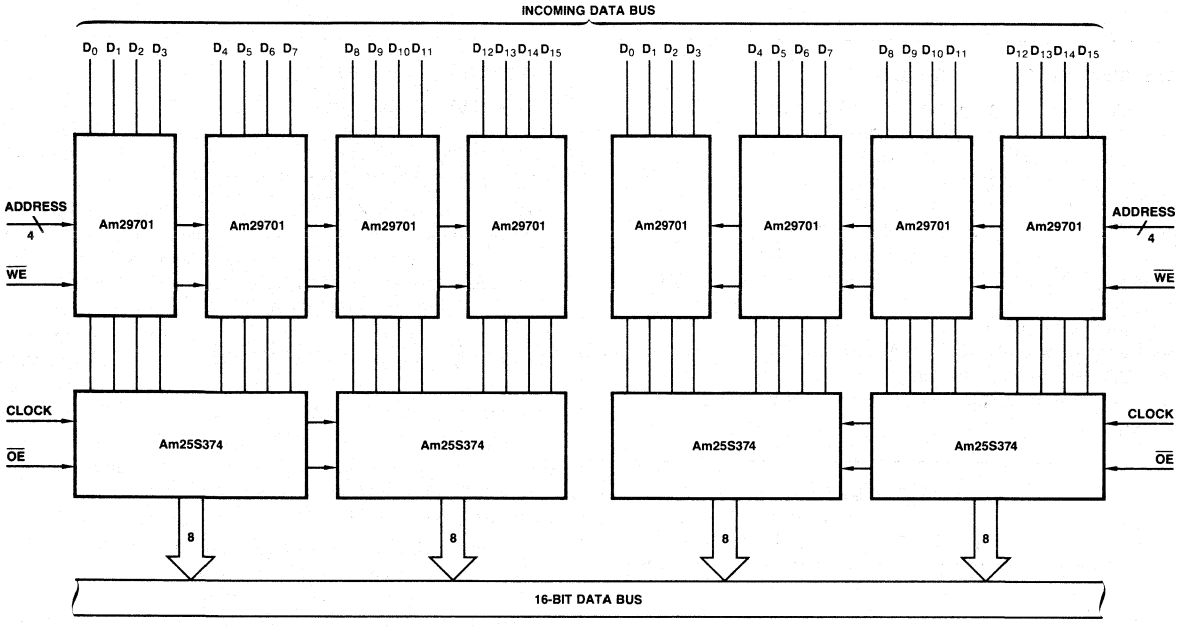


Am25S/54S/74S534



DIE SIZE 0.096" X 0.083"

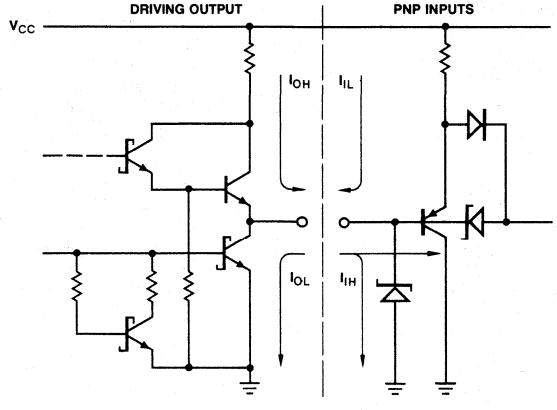
APPLICATION



Dual 16-word by 16-bit non-inverting high-speed data buffer.

BLI-054

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI-055

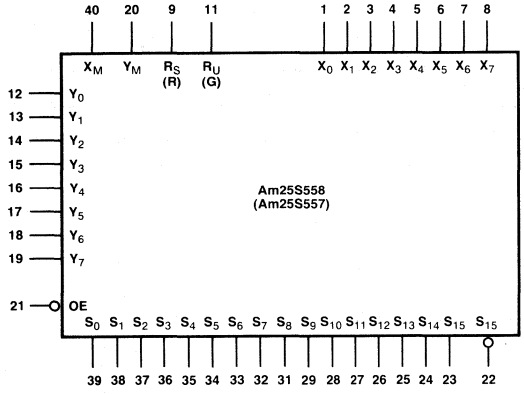
Am25S557 • Am25S558

Eight-Bit by Eight-Bit Combinatorial Multiplier

DISTINCTIVE CHARACTERISTICS

- Multiplies two 8-bit numbers – 16-bit output
- Combinatorial – no clocks required
- Full 8 x 8 multiply in 45ns typ.
- Cascades to 16 x 16 in 110ns typ.
- Expandable to multiples of 8 bits
- MSB and $\overline{\text{MSB}}$ outputs for easy expansion
- Unsigned, two's complement or mixed operands
- Implements common rounding algorithms with additional logic
- Three-state outputs
- Transparent 16-bit latch in Am25S557
- Industry standard pin-outs
- 100% product assurance screening to MIL-STD-883 requirements

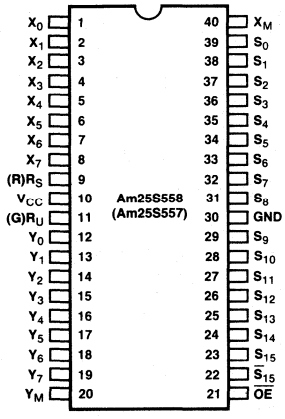
LOGIC SYMBOL



V_{CC} = Pin 10
GND = Pin 30

BLI-035

CONNECTION DIAGRAM



Pin assignments shown are for Am25S558. G and R shown in parentheses are pin assignments for Am25S557.

BLI-036

FUNCTIONAL DESCRIPTION

The Am25S557 and Am25S558 are high-speed, combinatorial, 8 x 8-bit multipliers. Both use an array of full adders to form and add partial products in a single unclocked operation, resulting in a 16-bit parallel output product.

Mode control inputs X_M and Y_M allow the multiplier to accept either unsigned or two's complement numbers from either respective input to provide an unsigned or signed output. The mode control lines are held LOW for unsigned input words and HIGH for two's complement.

The Am25S557 and Am25S558 are easily expandable to longer work lengths. Both S_{15} and $\overline{S}_{15}$ are available to allow expansion in either signed or unsigned modes without external inverters. In the 16-bit by 16-bit configuration (32-bit output) the typical multiply time is 110ns.

Both configurations offer three-state output flexibility and the Am25S557 adds a 16-bit transparent latch between the multiplier array and the three-state output buffers (including $\overline{S}_{15}$).

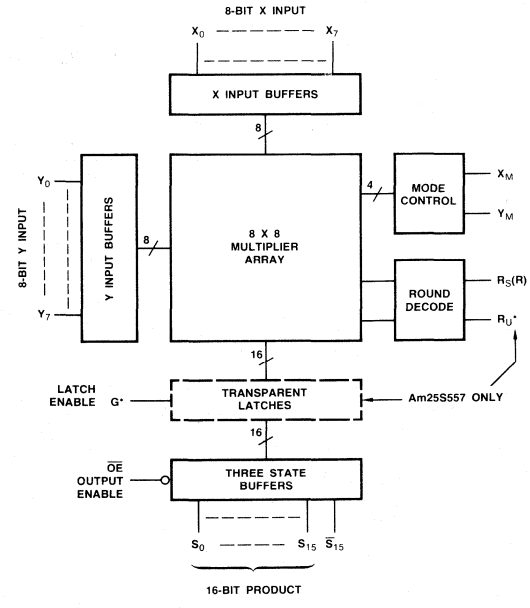
Rounding provisions for 8-bit truncated output configurations are particularly optimized for maximum flexibility. The Am25S557 internally develops proper rounding for either signed or unsigned numbers by combining rounding input R with X_M, Y_M, $\overline{X}_M$ and $\overline{Y}_M$ as follows:

$R_U = \overline{X}_M \cdot \overline{Y}_M \cdot R$ = Unsigned Rounding input to 2^7 adder.

$R_S = (X_M + Y_M)\ R$ = Signed Rounding input to 2^6 adder.

Since the Am25S558 does not require the use of pin 9 for the latch enable input, (G), R_S and R_U are brought out separately.

LOGIC DIAGRAM



*Pin 11 is G for Am25S557 and R_U for Am25S558.

BLI-037

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)
MIL T_C = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	V_{IL} = 0.8V, V_{IH} = 2.0V	I_{OH} = −2.0mA	2.4	3.0		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	V_{IL} = 0.8V, V_{IH} = 2.0V, I_{OL} = 8.0mA			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.8	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V					100	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	V_O = 0.5V				−100	µA
			V_O = 2.4V				+100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−20		−90	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.					280	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test with pin 21 at 4.5V, all other input pins at GND, all outputs open Am25S557 conditions the same except initialize with G (pin 11) at 4.5V, then GND.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am25S557 SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

		Am25S COM'L T_A = 0 to 70°C, V_{CC} = 5V ±5%			Am25S MIL T_A = −55 to +125°C, V_{CC} = 5V ±10%				
Parameters	Description	Min	Typ	Max	Min	Typ	Max	Units	Test Conditions
t_{PD}	X_i, Y_i to S_0 to S_7		45	60		55	70	ns	C_L = 30pF, R_L = 560Ω (See test figures)
t_{PD}	X_i, Y_i to S_8 to S_{15} or $\overline{S}_{15}$		50	80		60	90	ns	
t_s	X_i, Y_i to G Set-up Time	65			75			ns	
t_h	X_i, Y_i to G Hold Time	−5			−5			ns	
t_{PD}	G to S_i		30	45		30	50	ns	
t_{PW}	Latch Enable Pulse Width	25	15		30	15		ns	
t_{PHZ}	$\overline{OE}$ to S_0 to S_{15}		15	30		15	40	ns	
t_{PHZ}	$\overline{OE}$ to $\overline{S}_{15}$		25	40		25	50	ns	
t_{PLZ}	$\overline{OE}$ to S_i		15	30		15	40	ns	
t_{PZH}	$\overline{OE}$ to S_i		20	35		20	40	ns	
t_{PZL}	$\overline{OE}$ to S_i		20	35		20	40	ns	

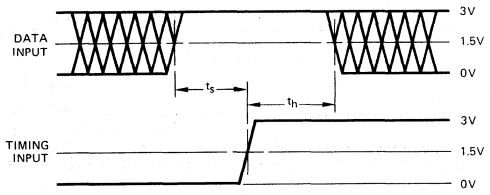
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, subgroup 9.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

		Am25S COM'L T_A = 0 to 70°C, V_{CC} = 5V ±5%			Am25S MIL T_A = −55 to +125°C, V_{CC} = 5V ±10%				
Parameters	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
t_{PD}	X_i, Y_i to S_0 to S_7		35	55		35	65	ns	C_L = 30pF, R_L = 560Ω (See test figures)
t_{PD}	X_i, Y_i to S_8 to S_{15} or $\overline{S}_{15}$		55	75		55	85	ns	
t_{PHZ}	$\overline{OE}$ to S_0 to S_{15}		15	30		15	40	ns	
t_{PHZ}	$\overline{OE}$ to $\overline{S}_{15}$		25	40		25	50	ns	
t_{PLZ}	$\overline{OE}$ to S_i		15	30		15	40	ns	
t_{PZH}	$\overline{OE}$ to S_i		20	35		20	40	ns	
t_{PZL}	$\overline{OE}$ to S_i		20	35		20	40	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, subgroup 9.

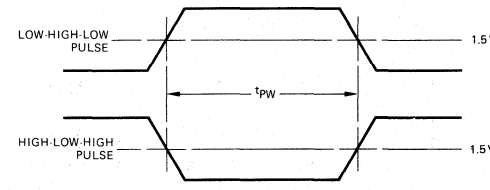
SET-UP AND HOLD TIMES



BLI-057

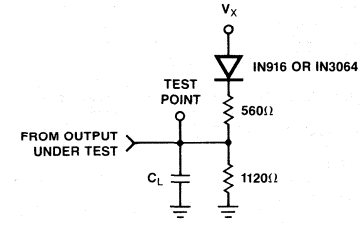
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

PULSE WIDTH



BLI-058

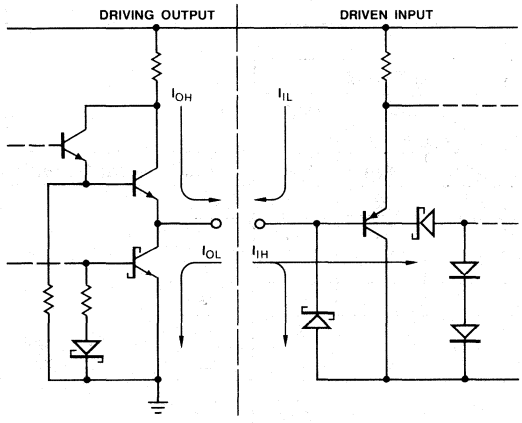
LOAD TEST CIRCUIT



BLI-059

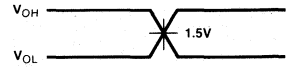
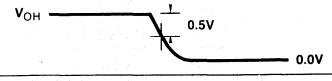
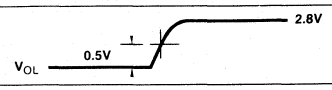
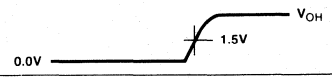
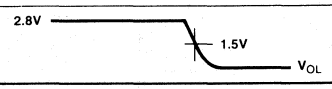
C_L Includes probe and jig capacitance.

Am25S557 • Am25S558 INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



BLI-038

TEST WAVEFORMS

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	5.0V	
t_{PHZ}	0.0V	
t_{PLZ}	5.0V	
t_{PZH}	0.0V	
t_{PZL}	5.0V	

DEFINITION OF TERMS

X_0-X_7	Multiplicand 8-bit data inputs
Y_0-Y_7	Multiplier 8-bit data inputs
X_M, Y_M	Mode control inputs for each data word; LOW for unsigned data and HIGH for two's complement data
S_0-S_{15}	Product 16-bit output
$\overline{S_{15}}$	Inverted MSB for expansion
R_S, R_U	Rounding inputs for signed and unsigned data, respectively (Am25S558 only)
G	Transparent Latch Enable (Am25S557 only)
$\overline{OE}$	Three-state enable for S_0-S_{15} outputs
R	Rounding input for signed or unsigned data (combined internally with X_M, Y_M in Am25S557 only)

MODE CONTROL INPUTS

Operating Mode	Input Data		Mode Control Inputs	
	X_0-X_7	Y_0-Y_7	X_M	Y_M
UNSIGNED	UNSIGNED	UNSIGNED	L	L
MIXED	UNSIGNED	2's COMP	L	H
	2's COMP	UNSIGNED	H	L
SIGNED	2's COMP	2's COMP	H	H

ROUNDING INPUTS

Am25S557

Inputs			Adds	
X_M	Y_M	R	2^7	2^6
L	L	H	YES	NO
L	H	H	NO	YES
H	L	H	NO	YES
H	H	H	NO	YES
X	X	L	NO	NO

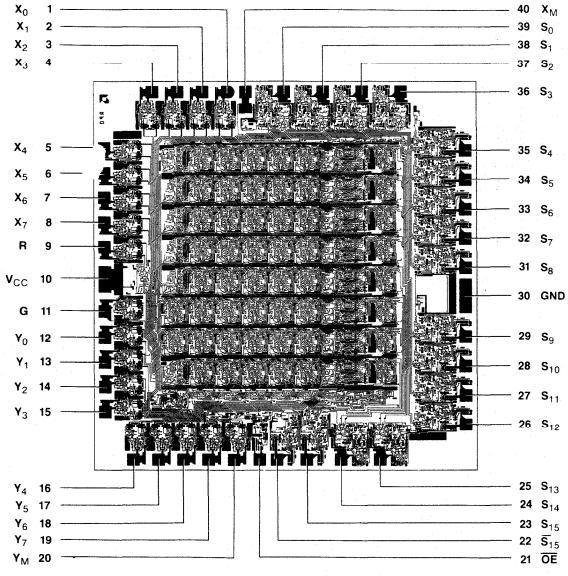
Am25S558

Inputs		Adds		Normally Used With	
R_U	R_S	2^7	2^6	X_M	Y_M
L	L	NO	NO	X	X
L	H	NO	YES	$X_M + Y_M = H$	
H	L	YES	NO	L	L
H	H	YES	YES	*	*

* Most rounding applications require a HIGH level for R_U or R_S, but not both.

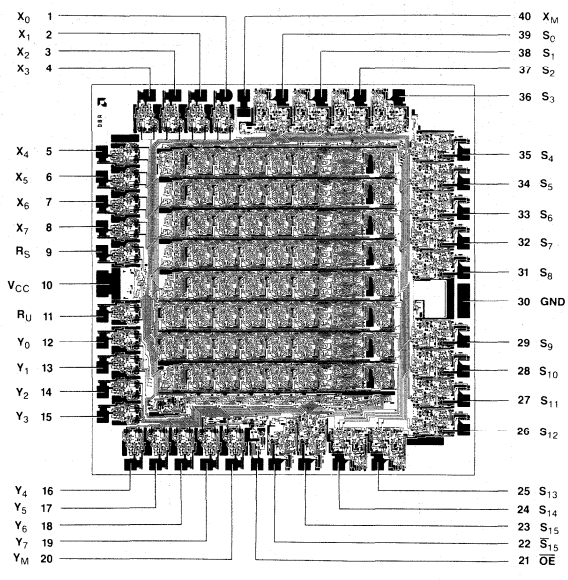
Metallization and Pad Layouts

Am25S557



DIE SIZE 0.171" X 0.165"

Am25S558



DIE SIZE 0.171" X 0.165"

APPLICATION

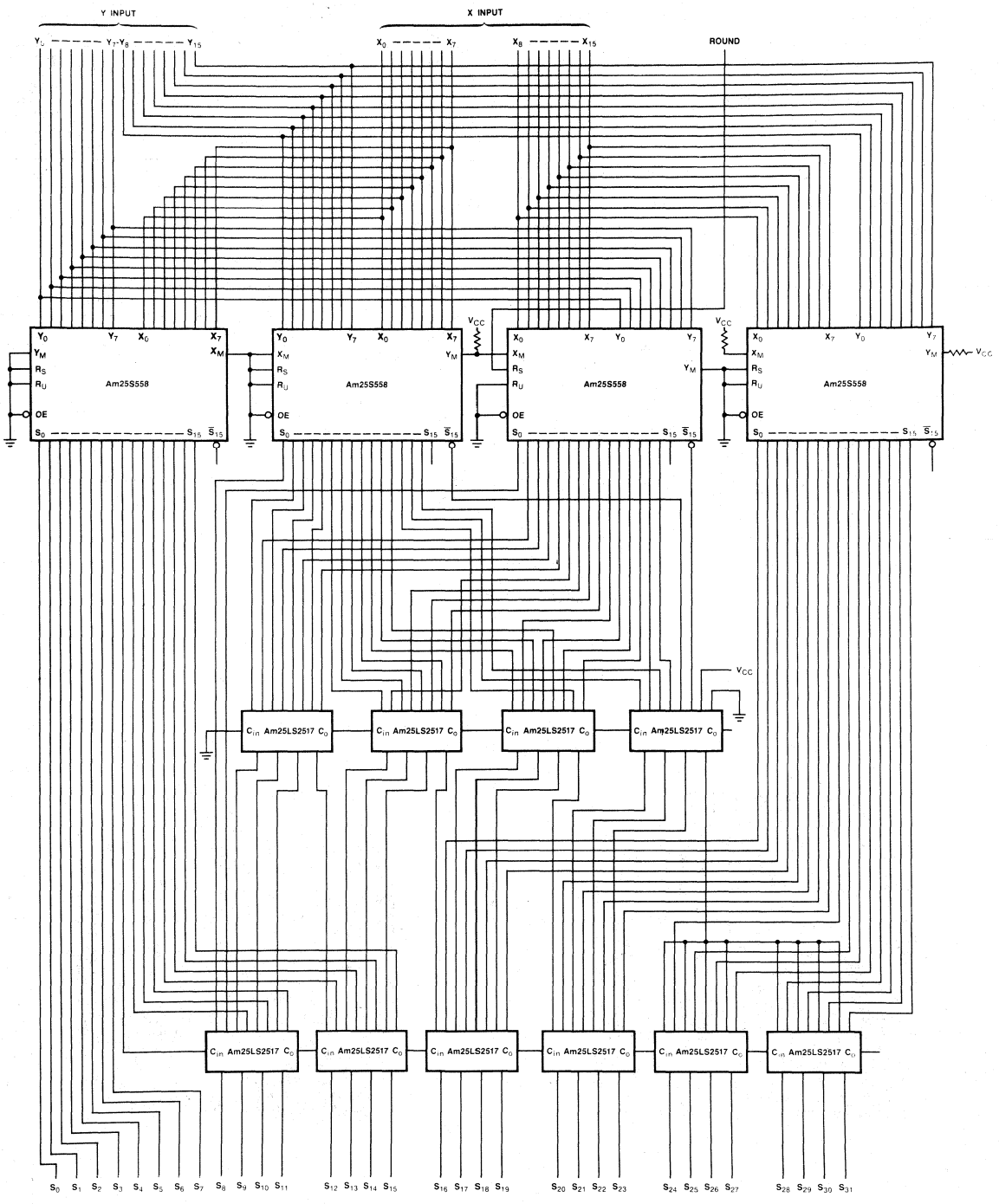
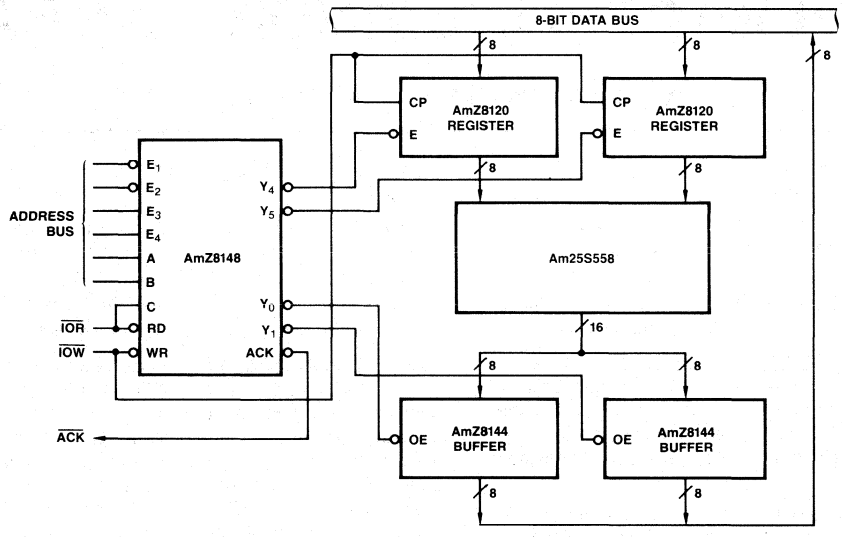


Figure 2. High-Speed 16 x 16 2's Complement Multiplication.

BLI-040

I/O MAPPED INTERFACE WITH MOS MICROPROCESSOR



BLI-060

ORDERING INFORMATION

Package Type	Temperature Range	Am25S557 Order Number	Am25S558 Order Number
Hermetic DIP	0°C to +70°C	AM25S557DC	AM25S558DC
	−55°C to +125°C	AM25S557DM	AM25S558DM

Am25S557 • Am25S558 MULTIPLIERS in EXPANDED ARRAYS

By Bernie New and David Anderson

GENERAL DESCRIPTION

The Am25S557 and Am25S558 are high-speed, combinatorial, 8 x 8-bit multipliers. Both use an array of gated full adders to form and add simultaneously the partial products necessary to generate a parallel product.

Both devices have two Mode Control inputs X_m and Y_m. These controls allow multiplying any of the four combinations of unsigned or two's complement numbers.

The availability of $\overline{S}_{15}$ (inverted MSB) and the capability of operating with either signed or unsigned inputs means the Am25S557 and Am25S558 can be easily expanded to larger array sizes which can similarly multiply signed or unsigned numbers.

In addition to the three-state output flexibility of both devices the Am25S557 adds a transparent latch between the multiplier array and the output buffers.

Both multipliers incorporate rounding provisions; both use a standard 40-pin package; and both are available in commercial or military version.

INTRODUCTION

There are various methods of implementing large number multiplication by using the Am25S557 and Am25S558 multipliers. In high-speed applications a parallel array of multipliers will generate an output product in the shortest time. However, this approach also requires a large parts count. A partial parallel expansion sacrifices some speed for a reduced parts count, while a single multiplier performing repetitive multiplications requires the smaller number of parts but is slow when multiplying large numbers.

The Am25S557 includes a transparent product output latch useful in pipelined applications (Figure 1). In such an application, the result of a current multiply may be held for use by other parts of the system while the next multiply is already in progress.

This application note explains how to implement both parallel and partial parallel expansion to form large multiplier arrays using the Am25S557 or Am25S558 as the basic building block. A brief discussion on multiplier arithmetic is first presented to clarify operation of the part. For a complete functional description see the Am25S557/558 data sheet.

ARITHMETIC

Mode control inputs X_m and Y_m (Figure 1) allow the multiplier to accept either unsigned or two's complement numbers at either X or Y input. These controls are necessary to tell the part how to interpret the input data since the multiplier can't tell from the number alone. If either input is in two's complement form, the result will necessarily be two's complement. Only if both operands are unsigned will the product be unsigned.

For example, the binary number 11111111 may be interpreted as 255 or −1 depending on the number convention used – unsigned or two's complement. Similarly, 11111110 is 254 or −2. The mode controls tell the multiplier which one is appropriate.

If these inputs are used, the following four interpretations are possible:

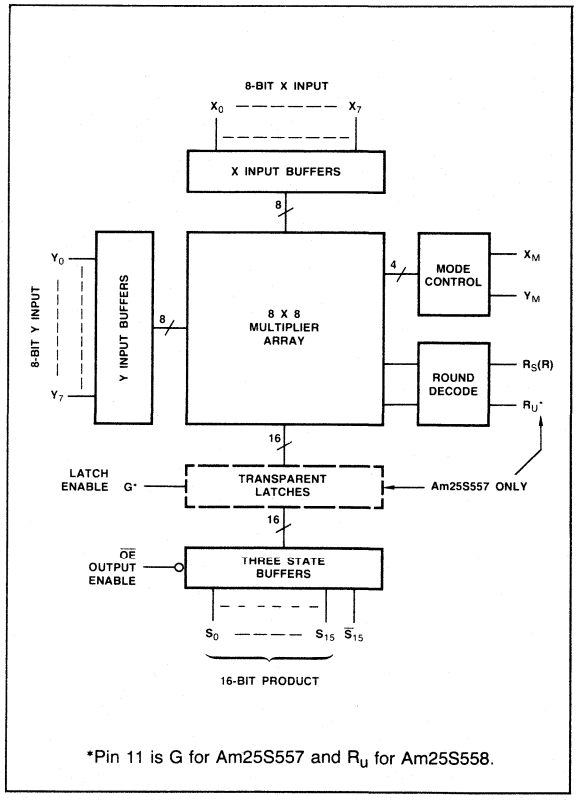
255 x 254	= +64770,	1111110100000010 (unsigned)
(−1) x 254	= −254,	1111111100000010 (2's complement)
255 x (−2)	= −510,	1111111000000010 (2's complement)
(−1) x (−2)	= +2,	0000000000000010 (2's complement)

All four of these different answers are correct.

Two round controls (R_S and R_U) are provided on the Am25S558. R_S indicates signed number rounding and R_U indicates unsigned number rounding. In signed number rounding a bit is added with the same weight as S_6. This allows $S_{14\text{-}7}$ to be used as the rounded 8-bit output (Figure 2). In unsigned multiplication, R_U adds a bit with the weight of S_7. $S_{15\text{-}8}$ may then be used as the 8-bit unsigned output (Figure 3). The Am25S557 internally develops the appropriate rounding control R_S or R_U by combining rounding input R with X_m and Y_m as follows:

$$R_U = \overline{X_m} \bullet \overline{Y_m} \bullet R$$
$$R_S = (X_m + Y_m) \bullet R$$

This frees a pin for use as the latch enable (G).



*Pin 11 is G for Am25S557 and R_U for Am25S558.

Figure 1. Logic Diagram

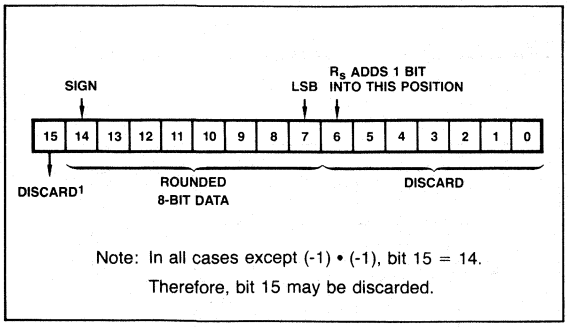


Figure 2. Rounding 16-Bit Signed Number for 8-Bit Signed Output Data

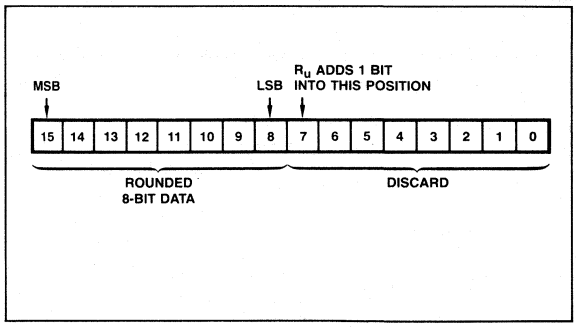


Figure 3. Rounding 16-Bit Unsigned Number for 8-Bit Unsigned Output Data

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PARALLEL EXPANSION

The Am25S558 is specifically designed for ease of expansion. To multiply 8n bits by 8m bits requires n • m multiplications. These may either be performed successively in a single multiplier or n • m multipliers may be used in parallel. A combination of the two approaches, partial parallel expansion, is also possible. A 24 x 24-bit unsigned product using parallel multipliers can be fabricated as follows:

1. Split each of the 24-bit inputs into 8-bit groups. X would split into XA, XB, XC where
   $XA_{0-7} = X_{16-23}$
   $XB_{0-7} = X_{8-15}$
   $XC_{0-7} = X_{0-7}$

   The relationship between X and the groups is
   $X = 2^{16} XA + 2^{8} XB + XC$

2. Treating Y in the same way
   $Y = 2^{16} YA + 2^{8} YB + YC$

3. The required multiplication is
   $XY = (2^{16} XA + 2^{8} XB + XC) \cdot (2^{16} YA + 2^{8} YB + YC)$
   $= 2^{32} XA \cdot YA + 2^{24} XA \cdot YB + 2^{16} XA \cdot YC$
   $+ 2^{24} XB \cdot YA + 2^{16} XB \cdot YB + 2^{8} XB \cdot YC$
   $+ 2^{16} XC \cdot YA + 2^{8} XC \cdot YB + XC \cdot YC$

   This requires nine multiplies.

4. Shift the partial products to weight them with the appropriate power of 2 and sum them.

Slower, low-cost systems can be implemented with a single multiplier but the fastest approach uses nine multipliers in a parallel array (Figure 4).

A signed 24 by 24-bit multiplier is configured basically the same way, but consideration must be given to which of the 8-bit groups are signed or unsigned. In the 24-bit word, the sign is weighted negatively and the other bits are weighted positively. In the 8-bit groups only XA and YA have negatively weighted most significant bits (MSBs); the other groups are all positive (unsigned). It follows, therefore, the XA and YA are signed two's complement numbers and XB, XC, YB and YC are positive unsigned numbers.

When generating the partial products, the mode controls must be connected appropriately. If either or both of the groups multiplied to form a partial product are a signed number, then the partial product is also a signed number and must be sign extended in any addition.

Partial Parallel Expansion

Another way to perform multiplications of numbers with more than 8 bits is to use partial parallel expansion. Here the multiplier array is expanded for only one operand. The following example constructs a 32 x 32-bit multiplier using a four-step sequence of 8 x 32 multiplies. An 8 by 32-bit multiply is performed using four Am25S558s (Figure 5).

X is split into XA, XB, XC, XD where

$XA = X_{24-31}$
$XB = X_{16-23}$
$XC = X_{8-15}$
$XD = X_{0-7}$

The relationship between them is

$$X = 2^{24}XA + 2^{16}XB + 2^{8}XC + XD$$

Y is treated the same way

$$Y = 2^{24}YA + 2^{16}YB + 2^{8}YC + YD$$

In this example the multiplier array can only accept 8 bits on the Y inputs. Therefore, the partial Y operands are applied to the multiplier array sequentially. The multiplication performed at each step is as follows:

Sequence

St1	$YD \cdot (2^{24}XA + 2^{16}XB + 2^{8}XC + XD)$
St2	$2^{8}YC \cdot (2^{24}XA + 2^{16}XB + 2^{8}XC + XD)$
St3	$2^{16}YB \cdot (2^{24}XA + 2^{16}XB + 2^{8}XC + XD)$
St4	$2^{24}YA \cdot (2^{24}XA + 2^{16}XB + 2^{8}XC + XD)$

The partial products from each step are next shifted to weight them with the appropriate power of 2. They are then summed to form the final 64-bit product (Figure 6).

Multiplexing

For extremely fast 8 x 8 multiplication, two or more Am25S558s may be multiplexed as shown in Figure 7. Input latches hold both the X and Y input data for each multiplier until a combinatorial product output is generated. The product from each multiplier is multiplexed onto the output bus, using the three-state enable control, $\overline{OE}$, on the multiplier.

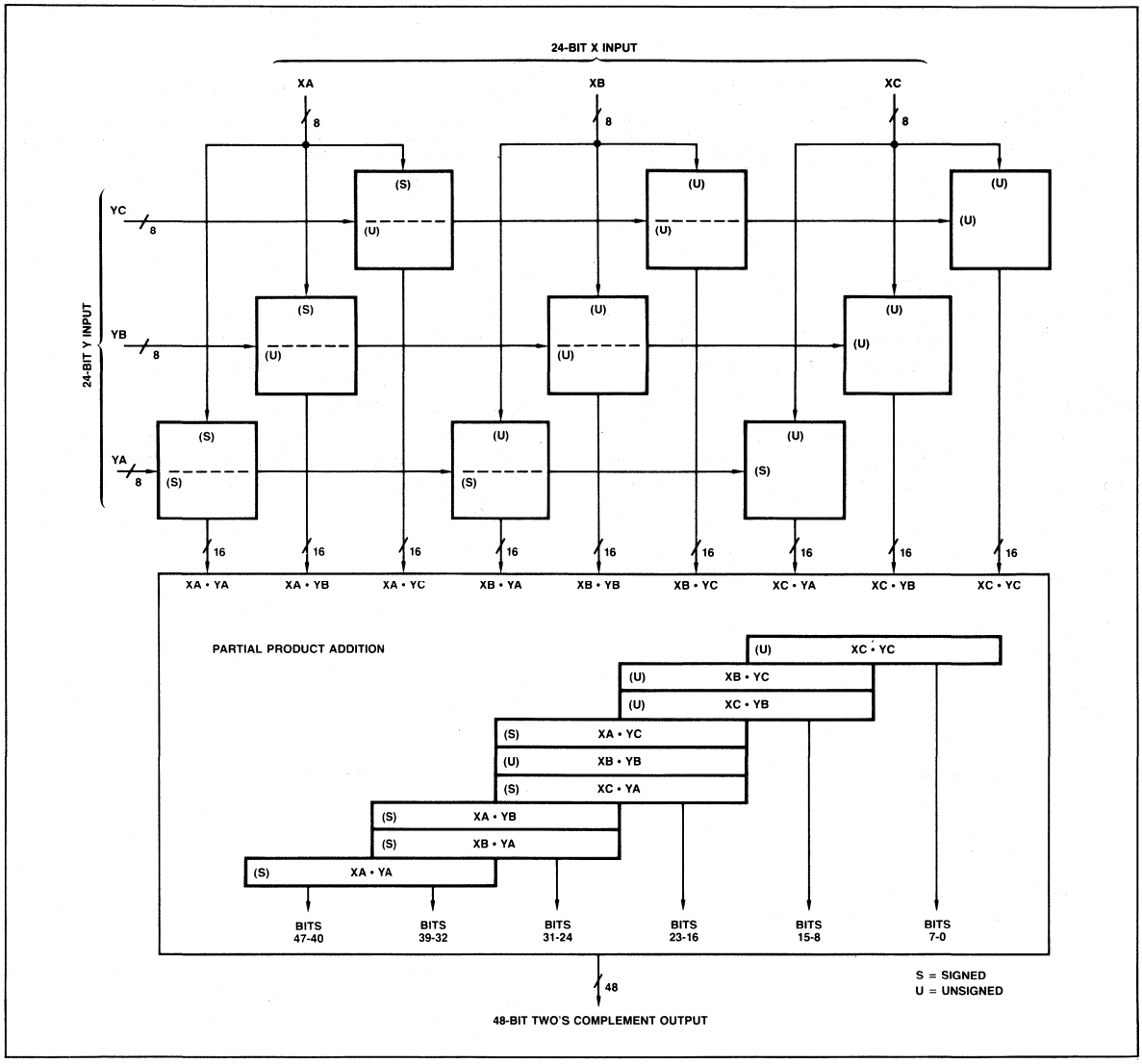
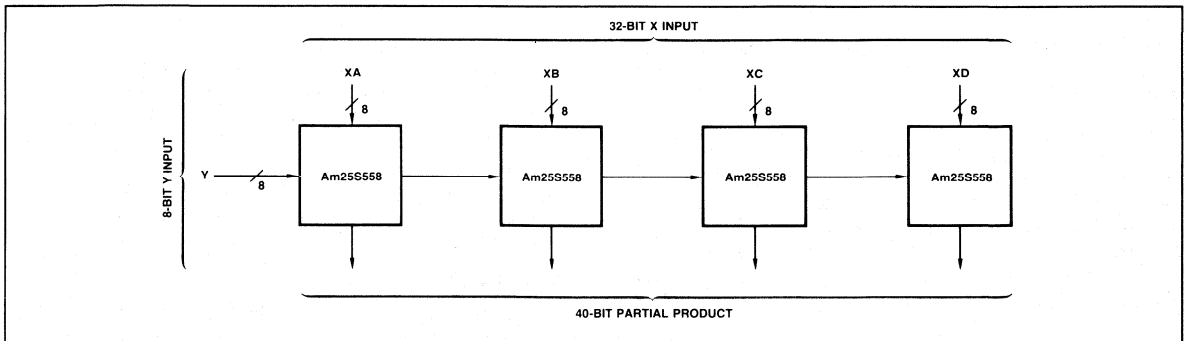


Figure 4. Two's Complement 24-Bit by 24-Bit Multiplier Array



The Y 8-bit partial operands YA, YB, YC, YD are loaded and multiplied by the entire 32-bit operand X in four steps to obtain a full 64-bit product.

Figure 5. 32 x 32-Bit Multiplier Array Partial Parallel Expansion

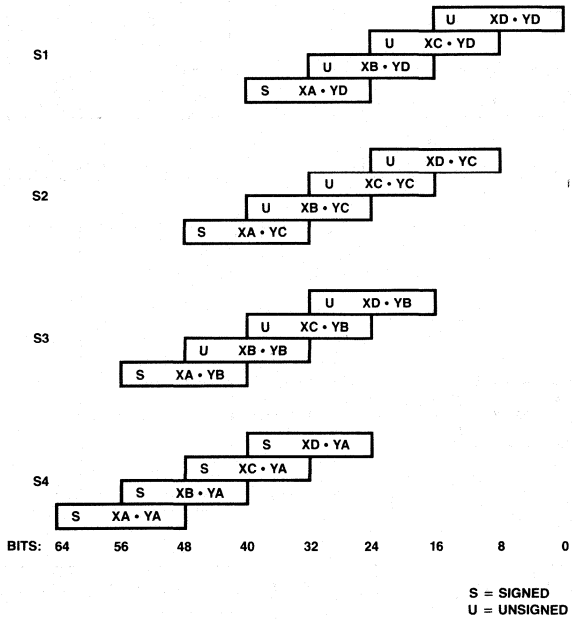


Figure 6. 32 x 32-Bit Serial/Parallel Expansion

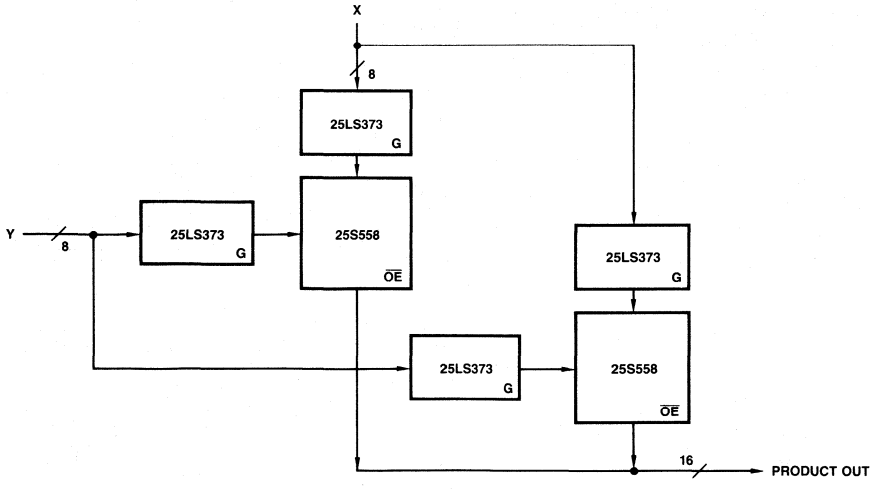


Figure 7. High-Speed Multiplexed 8 x 8-Bit Multiplication

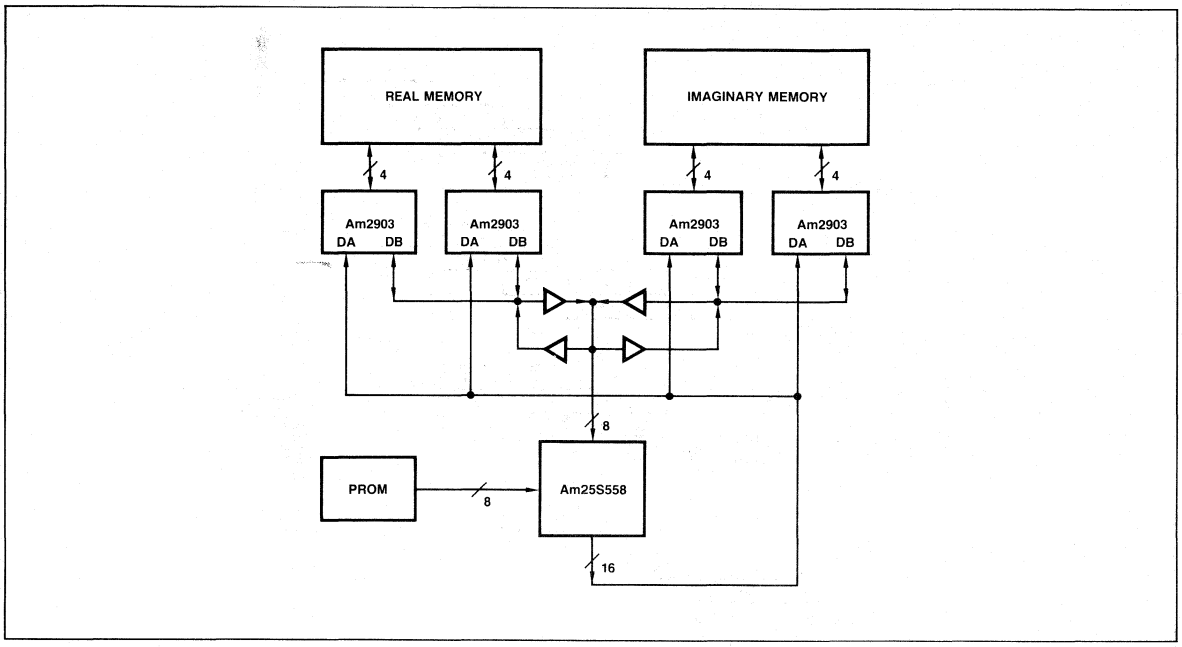


Figure 8. Block Diagram of a High-Performance Signal Processing System

Application

In many signal processing algorithms such as fast Fourier transforms (FFTs), finite impulse response (FIR) and infinite impulse response (IIR) digital filters, there is a need to perform fast repetitive multiplication. For off-line or low bandwidth applications, these computations could be performed in a general-purpose computer or even microcomputer. However, in any high-performance system, a dedicated, or at least an optimized processor must be constructed. Only microprogrammed, bipolar bit-slice devices provide the speed and flexibility necessary for such a processor.

Figure 8 is a block diagram of a typical high-performance system. The diagram shows how two pairs of Am2903s can be used in conjunction with a single Am25S558 Multiplier. The real or imaginary data may be entered into the multiplier, multiplied by a real or imaginary constant from the PROM and returned to the real or imaginary ALU as appropriate. The link between the DB ports also allows for a simple transfer of data which represents a multiplication by $\sqrt{-1}$.

Data Communications Interface Index

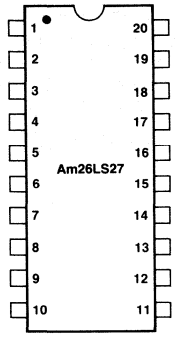
Am26LS27 • Am26LS28

Dual EIA RS-aaa Party Line Transceivers

Am26LS27 FEATURES

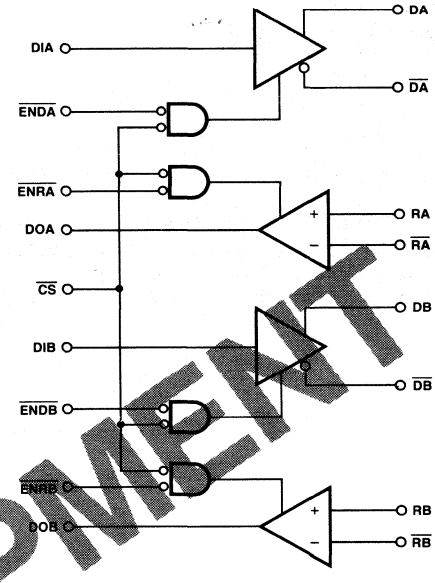
- Dual EIA RS-aaa party line transceiver
- 5MHz max. baud rate
- Drives dual terminated twisted pair line with up to 32 transceivers on line
- Output short circuit protected to V_{CM} limits
- High Z output at V_{CC} = max. and zero
- Separate enable gating for serial applications

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

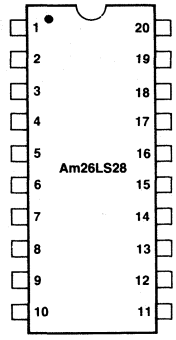
Am26LS27 LOGIC DIAGRAM



Am26LS28 FEATURES

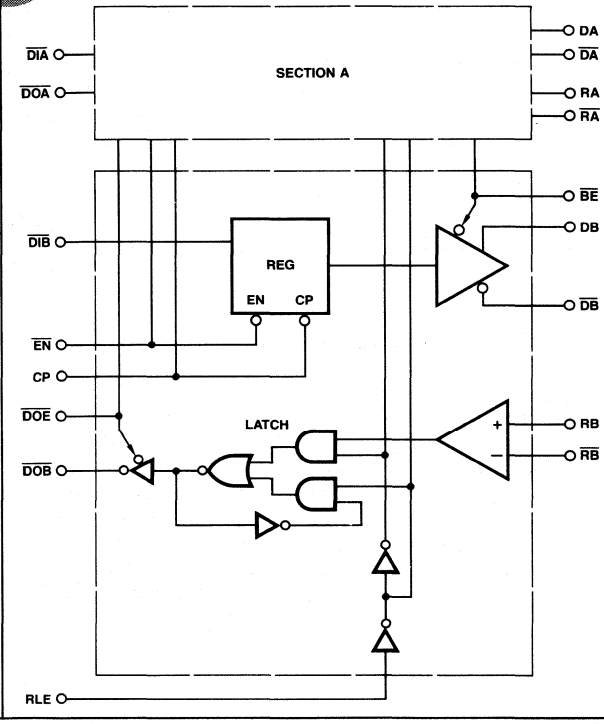
- Dual EIA RS-aaa party line transceiver
- 5MHz max. baud rate
- Drives dual terminated twisted pair line with up to 32 transceivers on line
- Output short circuit protected to V_{CM} limits
- High Z output at V_{CC} = max. and zero
- Latch on inputs and outputs with common enables for parallel application
- Three-state receiver outputs with common enable

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am26LS28 LOGIC DIAGRAM



Am26LS29

Quad Three-State Single Ended RS-423 Line Driver

DISTINCTIVE CHARACTERISTICS

- Four single ended line drivers in one package for maximum package density
- Output short-circuit protection
- Individual rise time control for each output
- High capacitive load drive capability
- Low I_{CC} and I_{EE} power consumption (26mW/driver typ.)
- Meets all requirements of RS-423
- Three-state outputs for bus oriented systems
- Outputs do not clamp line with power off or in hi-impedance state over entire transmission line voltage range of RS-423
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

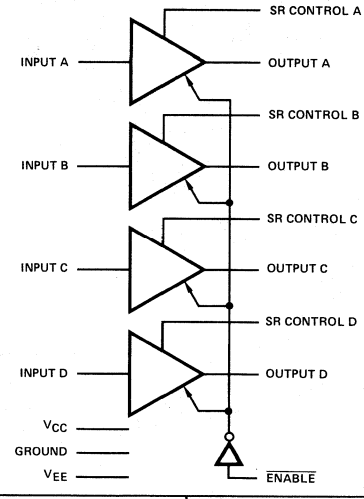
The Am26LS29 is a quad single ended line driver, designed for digital data transmission. The Am26LS29 meets all the requirements of EIA Standard RS-423 and Federal STD 1030. It features four buffered outputs with high source and sink current, and output short circuit protection.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS29 has three-state outputs for bus oriented systems. The outputs in the hi-impedance state will not clamp the line over the transmission line voltage of RS-423. A typical full duplex system would use the Am26LS29 line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS29 line drivers with only one enabled at a time and all others in the three-state mode.

The Am26LS29 is constructed using advanced low-power Schottky processing.

LOGIC DIAGRAM



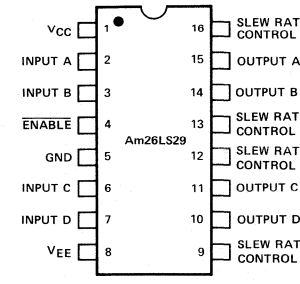
BLI-001

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM26LS29DM
Hermetic Flat Pak	−55°C to +125°C	AM26LS29FM
Dice	−55°C to +125°C	AM26LS29XM
Hermetic DIP	0°C to +70°C	AM26LS29DC
Molded DIP	0°C to +70°C	AM26LS29PC
Dice	0°C to +70°C	AM26LS29XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

BLI-004

BSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

orage Temperature	−65°C to +150°C
ıpply Voltage	
V+	7.0V
V−	−7.0V
ıwer Dissipation	600mW
put Voltage	−0.5 to +15.0V
ıtput Voltage (Power Off)	±15V
ead Soldering Temperature (10 seconds)	300°C

LECTRICAL CHARACTERISTICS over the operating temperature range

he following conditions apply unless otherwise specified:

m26LS29XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V +10, -5\%, V_{EE} = -5.0V -10, +5\%$
m26LS29XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%, V_{EE} = -5.0V \pm 5\%$

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)C CHARACTERISTICS over the operating temperature range (Notes 1 and 2)

'arameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_O	Output Voltage	$R_L = \infty$ (Note 3)	$V_{IN} = 2.4V$	4.0	4.4	6.0	Volts
$\overline{V_O}$			$V_{IN} = 0.4V$	−4.0	−4.4	−6.0	Volts
V_T	Output Voltage	$R_L = 450\Omega$	$V_{IN} = 2.4V$	3.6	4.1		Volts
$\overline{V_T}$			$V_{IN} = 0.4V$	−3.6	−4.1		Volts
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Output Unbalance	$\lvert V_{CC} \rvert = \lvert V_{EE} \rvert$, $R_L = 450\Omega$			0.02	0.4	Volts
I_{X^+}	Output Leakage Power Off	$V_{CC} = V_{EE} = 0V$	$V_O = 10V$		2.0	100	μA
I_{X^-}			$V_O = -10V$		−2.0	−100	μA
I_{S^+}	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 2.4V$		−70	−150	mA
I_{S^-}			$V_{IN} = 0.4V$		60	150	mA
I_{Slew}	Slew Control Current	$V_{SLEW} = V_{EE} + 0.9V$			±110		μA
I_{CC}	Positive Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			−10	−22	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX.	$V_O = 10V$		2.0	100	μA
			$V_O = -10V$		−2.0	−100	μA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1.0	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12mA$				−1.5	Volts

otes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9V minimum and −3.9V minimum at −55°C.

AC CHARACTERISTICS

$V_{CC} = 5.0V$, $V_{EE} = -5.0V$, $T_A = 25°C$

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
t_r	Rise Time	$R_L = 450\Omega$, $C_L = 500pF$, Fig. 1	$C_C = 50pF$		3.0		μs
			$C_C = 0pF$		120	300	ns
t_f	Fall Time	$R_L = 450\Omega$, $C_L = 500pF$, Fig. 1	$C_C = 50pF$		3.0		μs
			$C_C = 0pF$		120	300	ns
Src	Slew Rate Coefficient	$R_L = 450\Omega$, $C_L = 500pF$, Fig. 1			.06		μs/pF
t_{LZ}	Output Enable to Output	$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$, Fig. 2			180	300	ns
t_{HZ}					250	350	
t_{ZL}		$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$, Fig. 2			250	350	
t_{ZH}					180	300	

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

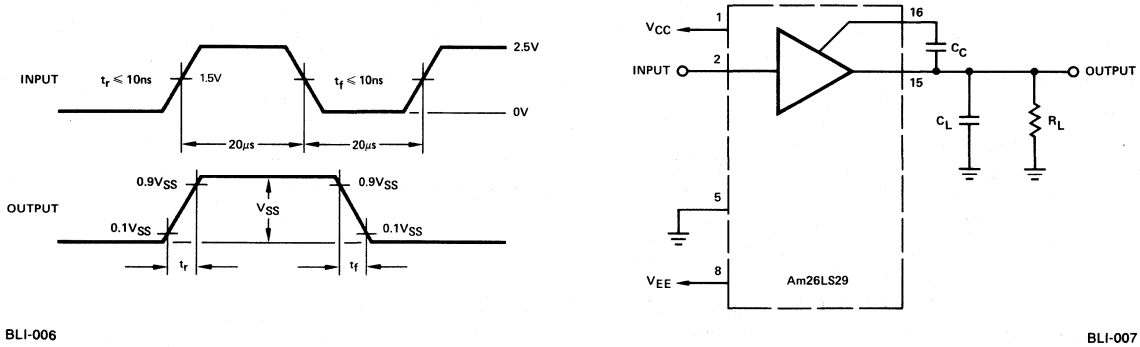


Figure 1. Rise Time Control.

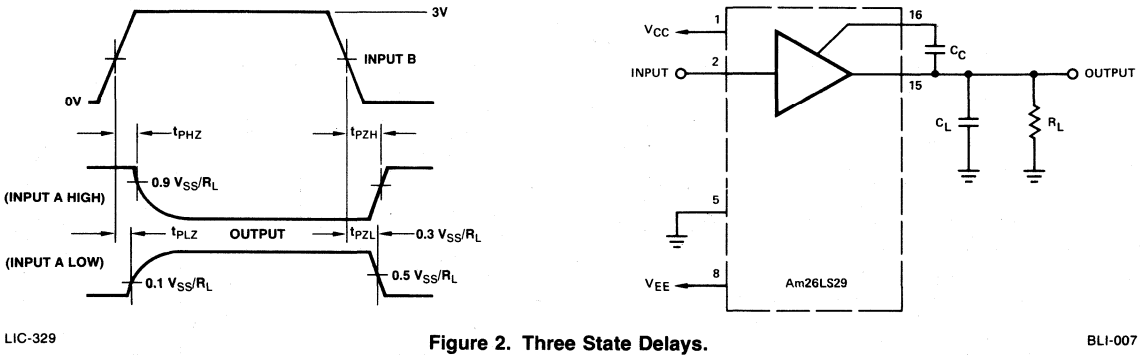
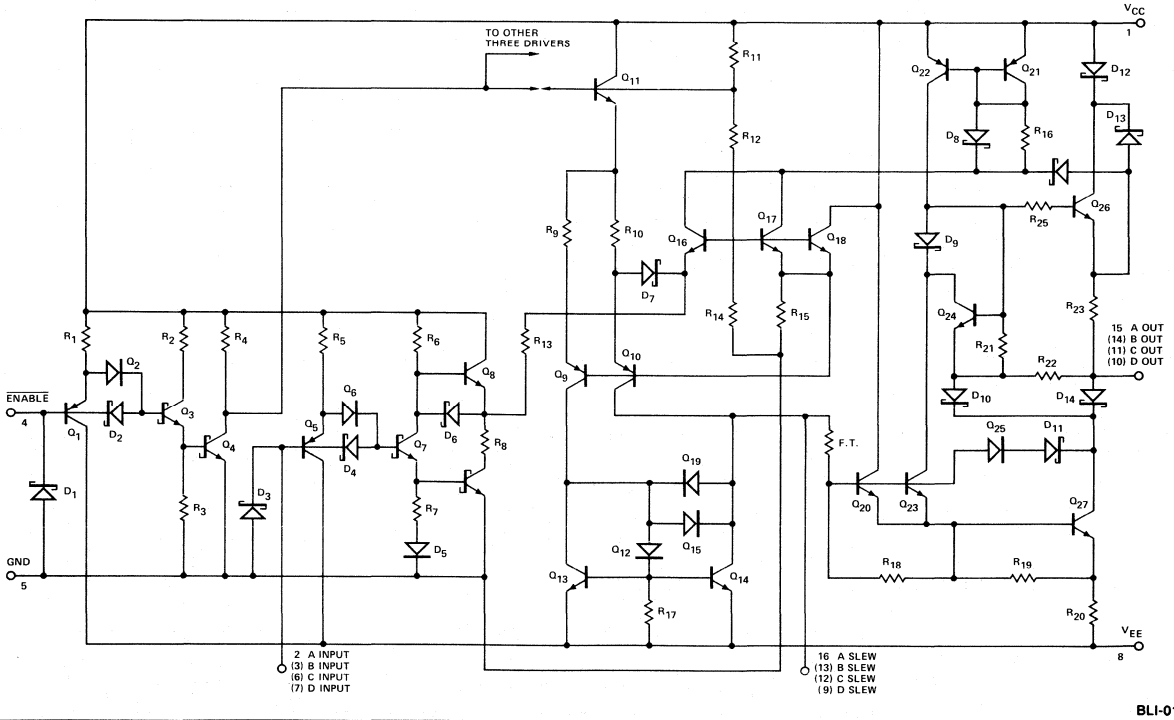
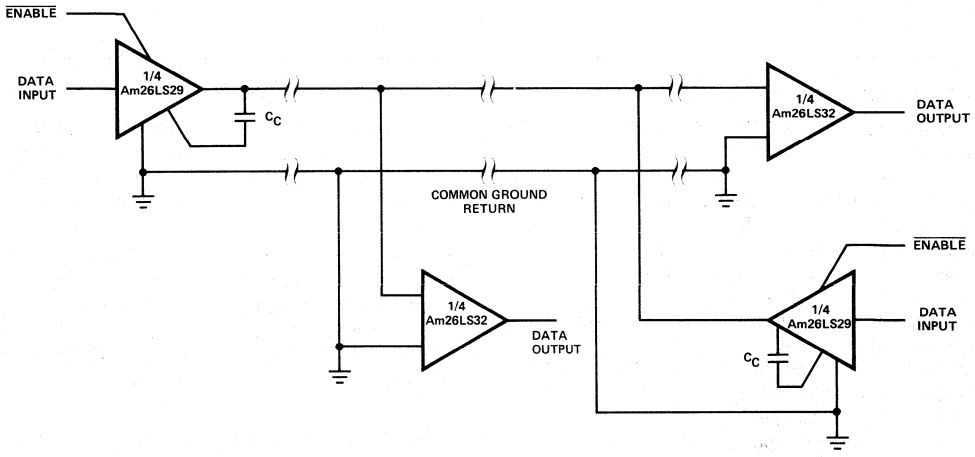


Figure 2. Three State Delays.

Am26LS29 EQUIVALENT CIRCUIT

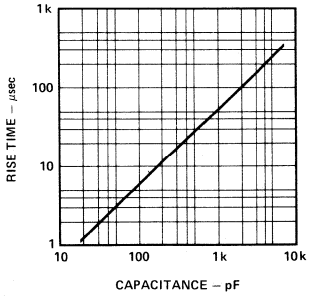


TYPICAL APPLICATION



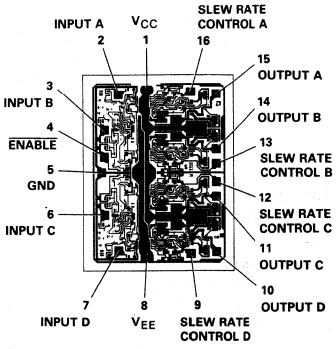
BLI-012

Slew Rate (Rise or Fall Time) Versus External Capacitor



BLI-010

Metallization and Pad Layout



DIE SIZE 0.070" X 0.094"

Am26LS30

Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver

DISTINCTIVE CHARACTERISTICS

- Dual RS-422 line driver or quad RS-423 line driver
- Driver outputs do not clamp line with power off or in hi-impedance state
- Individually three-state drivers when used in differential mode
- Low I_{CC} and I_{EE} power consumption
  - RS-422 differential mode 35mW/driver typ.
  - RS-423 single-ended mode 26mW/driver typ.
- Individual slew rate control for each output
- 50Ω transmission line drive capability (RS-422 into virtual ground)
- Low current PNP inputs compatible with TTL, MOS and CMOS
- High capacitive load drive capability
- Exact replacement for DS16/3691
- Advanced low power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am26LS30 is a line driver designed for digital data transmission. A mode control input provides a choice of operation either as two differential line drivers which meet all of the requirements of EIA Standard RS-422 or four independent single-ended RS-423 line drivers.

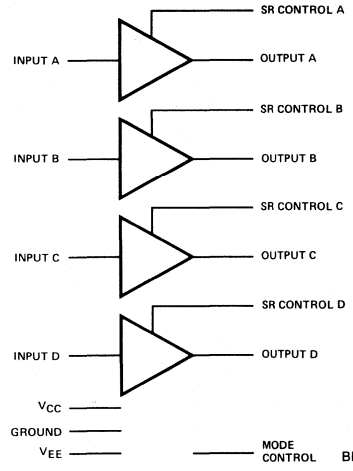
In the differential mode the outputs have individual three-state controls. In the hi-impedance state these outputs will not clamp the line over a common mode transmission line voltage of ±10V. A typical full duplex system would be the Am26LS30 differential line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS30 differential drivers.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS30 is constructed using Advanced Low Power Schottky processing.

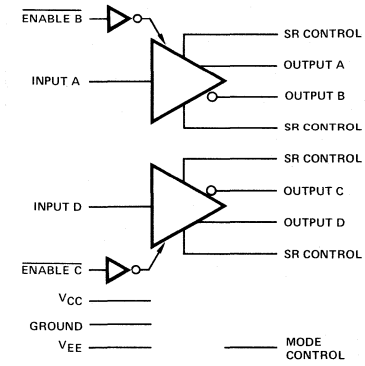
LOGIC DIAGRAMS

Logic for Am26LS30 with Mode Control HIGH (RS-423)



BLI-002

Logic for Am26LS30 with Mode Control LOW (RS-422)

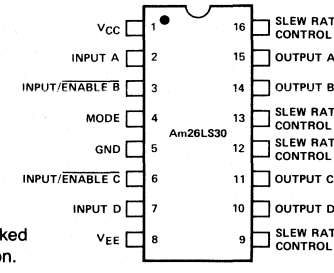


BLI-003

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM26LS30DM
Hermetic Flat Pak	−55°C to +125°C	AM26LS30FM
Dice	−55°C to +125°C	AM26LS30XM
Hermetic DIP	0°C to +70°C	AM26LS30DC
Molded DIP	0°C to +70°C	AM26LS30PC
Dice	0°C to +70°C	AM26LS30XC

CONNECTION DIAGRAM – Top View



Note:
Pin 1 is marked for orientation.

BLI-005

;SOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

rage Temperature	−65°C to +150°C
ɔply Voltage	
V+	7.0V
V−	−7.0V
ver Dissipation	600mW
ɹut Voltage	−0.5 to +15.0V
tput Voltage (Power Off)	±15V
ɜd Soldering Temperature (10 seconds)	300°C

.ECTRICAL CHARACTERISTICS over the operating temperature range

e Following Conditions Apply Unless Otherwise Specified:

ɹ26LS30XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = GND$

ɹ26LS30XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = GND$

ʎ RS-422 Connection, Mode Voltage = 0.8V

ɔ CHARACTERISTICS over the operating temperature range

arameters	Description	Test Conditions (Note 3)		Min.	Typ. (Note 1)	Max.	Units
V_O	Differential Output Voltage, $V_{A,B}$	$R_L = \infty$	$V_{IN} = 2.0V$		3.6	6.0	Volts
$\overline{V_O}$			$V_{IN} = 0.8V$		−3.6	−6.0	Volts
V_T	Differential Output Voltage, $V_{A,B}$	$R_L = 100\Omega$	$V_{IN} = 2.0V$	2.0	2.4		Volts
$\overline{V_T}$			$V_{IN} = 0.8V$	−2.0	−2.4		Volts
V_{OS}, $\overline{V_{OS}}$	Common Mode Offset Voltage	$R_L = 100\Omega$			2.5	3.0	Volts
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	$R_L = 100\Omega$			0.005	0.4	Volts
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common Mode Offset Voltage	$R_L = 100\Omega$			0.005	0.4	Volts
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	$R_L = 100\Omega$		4.0	4.8		Volts
V_{CMR}	Output Voltage Common Mode Range	$V_{\overline{ENABLE}} = 2.4V$		±10			Volts
I_{XA}	Output Leakage Current	$V_{CC} = 0V$	$V_{CMR} = 10V$			100	μA
I_{XB}			$V_{CMR} = -10V$			−100	μA
I_{OX}	Off State (High Impedance) Output Current	V_{CC} = MAX.	$V_{CMR} \leq 10V$			100	μA
			$V_{CMR} \geq -10V$			−100	μA
I_{SA}, I_{SB}	Output Short Circuit Current	$V_{IN} = 2.4V$	$V_{OA} = 6.0V$		80	150	mA
			$V_{OB} = 0V$		−80	−150	mA
		$V_{IN} = 0.4V$	$V_{OA} = 0V$		−80	−150	mA
			$V_{OB} = 6.0V$		80	150	mA
I_{CC}	Supply Current				18	30	mA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1.0	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12mA$				−1.5	Volts

AC CHARACTERISTICS

ΞIA RS-422 Connection, $V_{CC} = 5.0V$, $V_{EE} = GND$, Mode = 0.4V, $T_A = 25°C$

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_r	Differential Output Rise Time	Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_f	Differential Output Fall Time	Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_{PDH}	Output Propagation Delay	Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_{PDL}	Output Propagation Delay	Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_{LZ}	Output Enable to Output	$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$, Fig. 3		180	300	ns
t_{HZ}				250	350	
t_{ZL}		$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$, Fig. 3		250	350	
t_{ZH}				180	300	

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = GND$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-422 where applicable.
3. R_L connected between each output and its complement.

ELECTRICAL CHARACTERISTICS over the operating temperature range

The following conditions apply unless otherwise specified:

Am26LS30XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = -5.0V \pm 10\%$
Am26LS30XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = -5.0V \pm 5\%$
RS-423 Connection, Mode Voltage $\geq 2.0V$

DC CHARACTERISTICS over the operating temperature range (Notes 1 and 2)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_O	Output Voltage	$R_L = \infty$, (Note 3) $\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$	$V_{IN} = 2.4V$	4.0	4.4	6.0	Volts
$\overline{V_O}$			$V_{IN} = 0.4V$	−4.0	−4.4	−6.0	Volts
V_T	Output Voltage	$R_L = 450\Omega$, $\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$	$V_{IN} = 2.4V$	3.6	4.1		Volts
$\overline{V_T}$			$V_{IN} = 0.4V$	−3.6	−4.1		Volts
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output Unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, $R_L = 450\Omega$			0.02	0.4	Volts
I_X^+	Output Leakage Power Off	$V_{CC} = V_{EE} = 0V$	$V_O = 6.0V$		2.0	100	μA
I_X^-			$V_O = -6.0V$		−2.0	−100	μA
I_S^+	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 2.4V$		−80	−150	mA
I_S^-			$V_{IN} = 0.4V$		80	150	mA
I_{Slew}	Slew Control Current	$V_{SLEW} = V_{EE} + 0.9V$			±140		μA
I_{CC}	Positive Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			−10	−22	mA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1.0	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12mA$				−1.5	Volts

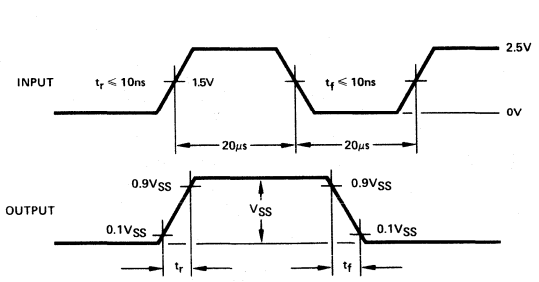
Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9V minimum and −3.9V minimum at −55°C.

AC CHARACTERISTICS

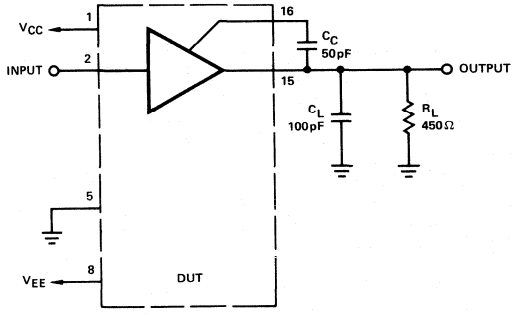
RS-423 Connection, $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, Mode = 2.4V, $T_A = 25°C$

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
t_r	Rise Time	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$	$C_C = 50pF$		3.0		μs
			$C_C = 0$		120	300	ns
t_f	Fall Time	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$	$C_C = 50pF$		3.0		μs
			$C_C = 0$		120	300	ns
Src	Slew Rate Coefficient	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$			.06		μs/pF
t_{PDH}	Output Propagation Delay	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0$			180	300	ns
t_{PDL}	Output Propagation Delay	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0$			180	300	ns

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS FOR EIA RS-423 CONNECTION



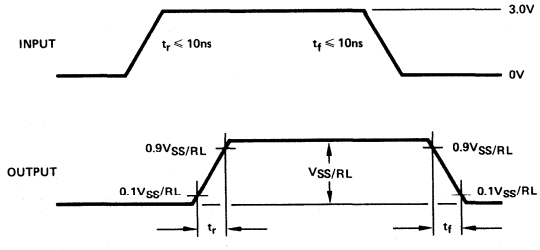
BLI-006



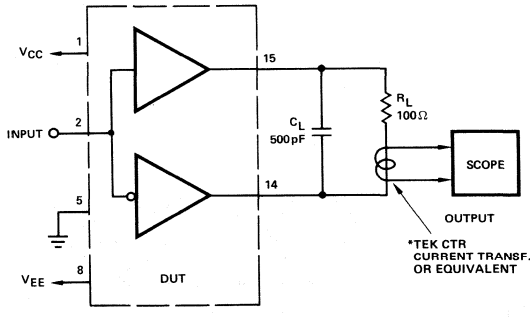
BLI-007

Figure 1. Rise Time Control for RS-423.

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUIT FOR RS-422 CONNECTION



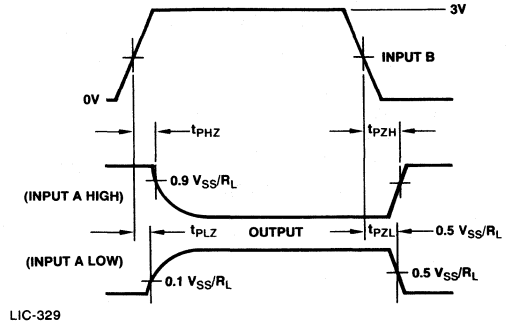
BLI-008



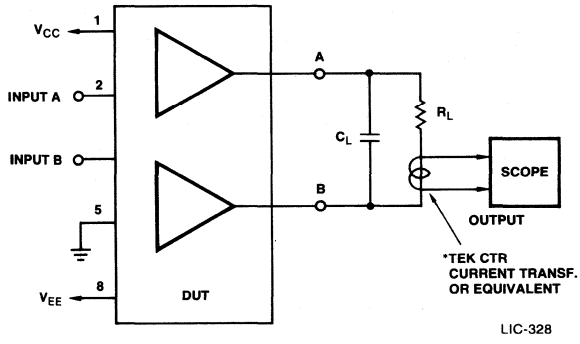
BLI-009

*Current probe is the easiest way to display a differential waveform.

Figure 2.



LIC-329



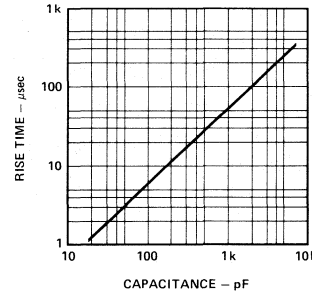
LIC-328

Figure 3. Three-State Delays.

Am26LS30 FUNCTION TABLE

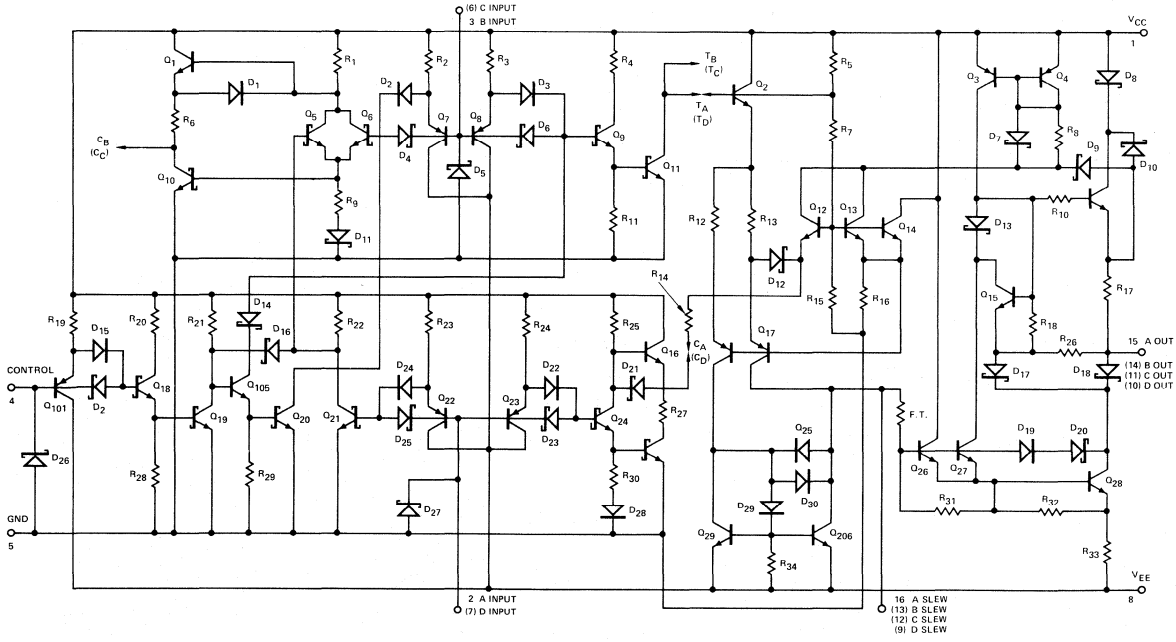
MODE	INPUTS		OUTPUTS	
	A(D)	B(C)	A(D)	B(C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Slew Rate (Rise or Fall Time) Versus External Capacitor



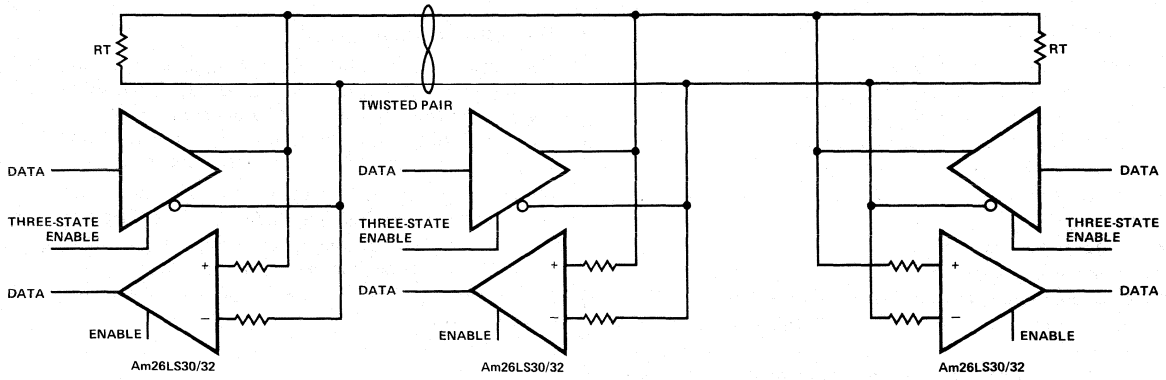
BLI-010

Am26LS30 EQUIVALENT CIRCUIT



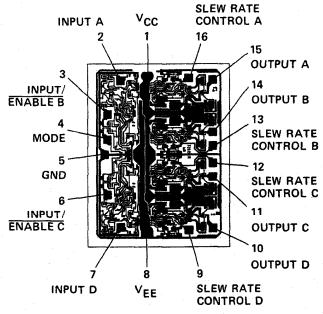
BLI-020

TYPICAL APPLICATION



BLI-032

Metallization and Pad Layout



DIE SIZE 0.070" X 0.094"

Am26LS31

Quad High Speed Differential Line Driver

DISTINCTIVE CHARACTERISTICS

- Output skew — 2.0ns typical
- Input to output delay — 12ns
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

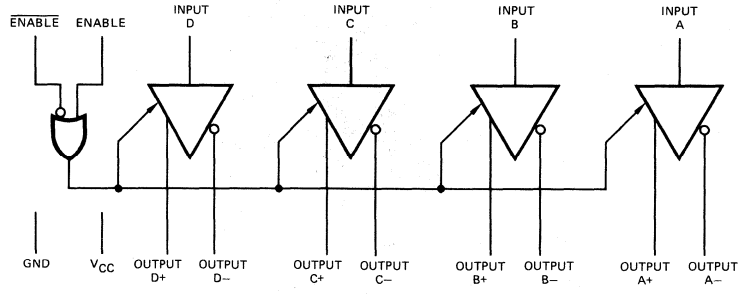
FUNCTIONAL DESCRIPTION

The Am26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. Is is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

LOGIC DIAGRAM

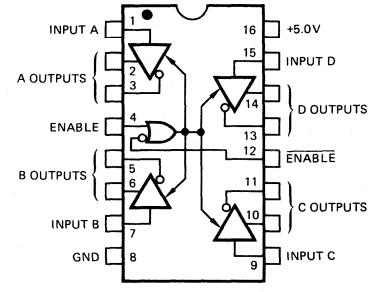


LIC-352

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM26LS31DM
Flat Pak	–55°C to +125°C	AM26LS31FM
Dice	–55°C to +125°C	AM26LS31XM
Hermetic DIP	0°C to +70°C	AM26LS31DC
Molded DIP	0°C to +70°C	AM26LS31PC
Dice	0°C to +70°C	AM26LS31XC

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.

LIC-353

ɜSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

ɔply Voltage	7.0V
ɔut Voltage	7.0V
tput Voltage	5.5V
ɔrage Temperature Range	−65°C to +150°C

⌊ECTRICAL CHARACTERISTICS over the operating temperature range

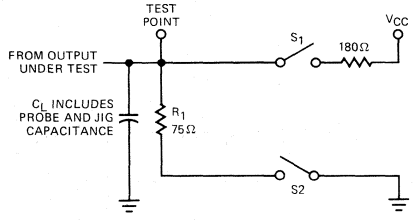
e following conditions apply unless otherwise specified:

ɔ26LS31XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5V \pm 10\%$
ɔ26LS31XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 5\%$

rameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −20mA		2.5	3.2		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 20mA			0.32	0.5	Volts
V_{IH}	Input HIGH Voltage	V_{CC} = Min.		2.0			Volts
V_{IL}	Input LOW Voltage	V_{CC} = Max.				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4V			−0.20	−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V			0.5	20	μA
I_I	Input Reverse Current	V_{CC} = Max., V_{IN} = 7.0V			0.001	0.1	mA
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.5V		0.5	20	μA
			V_O = 0.5V		0.5	−20	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = 18mA			−0.8	−1.5	Volts
I_{SC}	Output Short Circuit Current	V_{CC} = Max.		−30	−60	−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., all outputs disabled			60	80	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
SKEW	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			23	35	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			17	30	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			35	45	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			30	40	ns

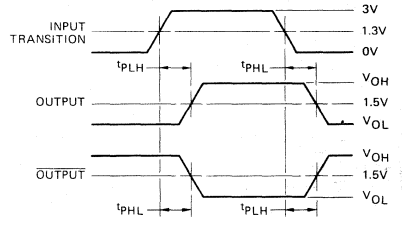
ɔtes: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.
2. C_L = 30pF, V_{IN} = 1.3V to V_{OUT} = 1.3V, V_{PULSE} = 0V to +3.0V, See Below.

AC LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



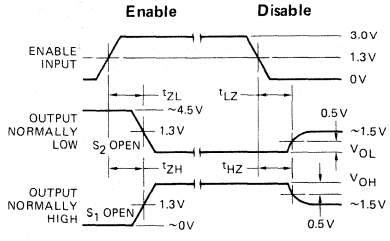
LIC-354

PROPAGATION DELAY (Notes 1 and 3)



LIC-355

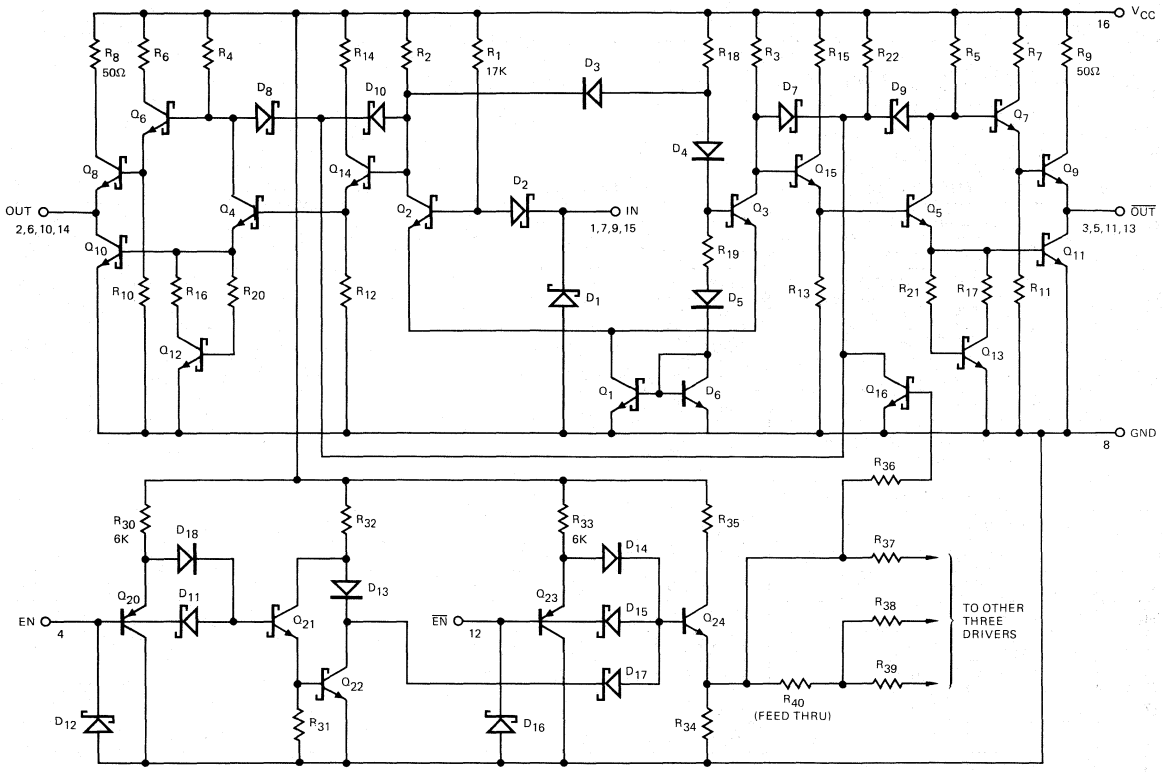
ENABLE AND DISABLE TIMES (Notes 2 and 3)



LIC-356

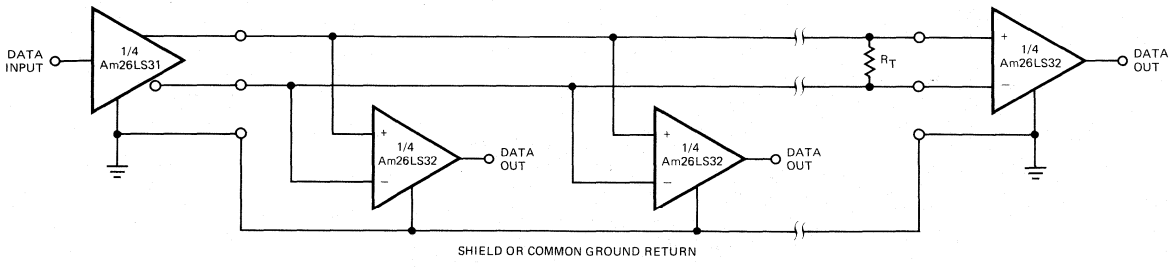
Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

EQUIVALENT CIRCUIT (1/4 Am26LS31)



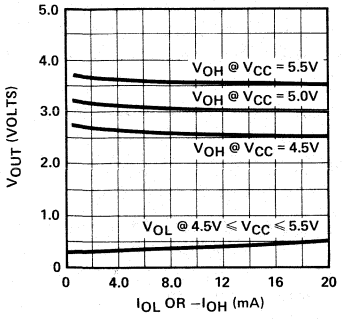
BLI-023

TYPICAL APPLICATION



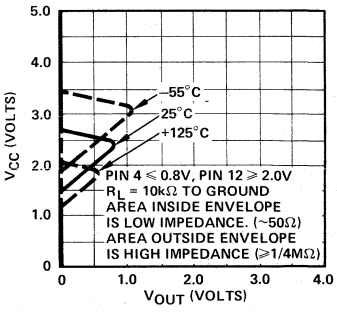
LIC-357

Guaranteed V_{OH} and V_{OL} (T_A = –55°C to +125°C)



LIC-358

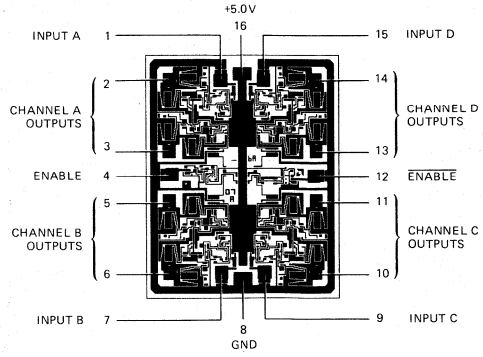
V_{OUT} Versus V_{CC}



LIC-359

4

Metallization and Pad Layout



DIE SIZE 0.067" X 0.084"

Am26LS32 • Am26LS33

Quad Differential Line Receivers

DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
- ±0.2V sensitivity over the input voltage range on Am26LS32; ±0.5V sensitivity on Am26LS33
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Fail safe input-output relationship. Output always high when inputs are open.
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.
- Propagation delay 17ns typical
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

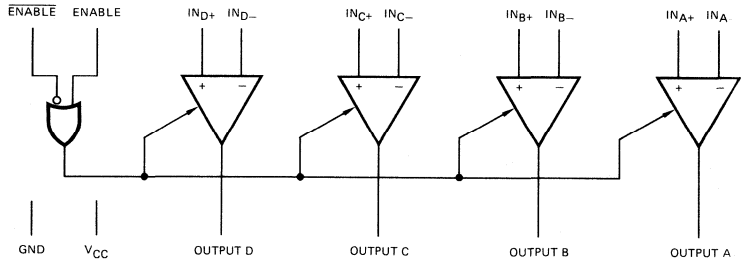
The Am26LS32 features an input sensitivity of 200mV over the input voltage range of ±7V.

The Am26LS33 features an input sensitivity of 500mV over the input voltage range of ±15V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

LOGIC DIAGRAM



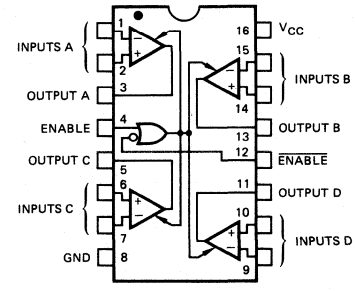
BLI-024

ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32 Order Number	Am26LS33 Order Number
Hermetic DIP	−55°C to +125°C	AM26LS32DM	AM26LS33DM
Flat Pak	−55°C to +125°C	AM26LS32FM	AM26LS33FM
Dice	−55°C to +125°C	AM26LS32XM	AM26LS33XM
Hermetic DIP	0°C to +70°C	AM26LS32DC	AM26LS33DC
Molded DIP	0°C to +70°C	AM26LS32PC	AM26LS33PC
Dice	0°C to +70°C	AM26LS32XC	AM26LS33XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-360

3SOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

pply Voltage	7.0V
mmon Mode Range	±25V
fferential Input Voltage	±25V
able Voltage	7.0V
tput Sink Current	50mA
orage Temperature Range	−65°C to +165°C

ECTRICAL CHARACTERISTICS Over the operating temperature range

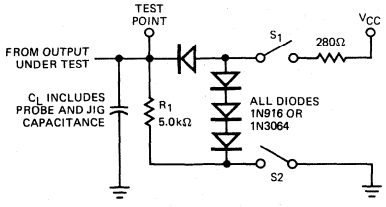
ıe following conditions apply unless otherwise specified:

n26LS32XM, Am26LS33XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$
n26LS32XC, Am26LS33XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

rameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	Am26LS32, $-7V \leq V_{CM} \leq +7V$	−0.2	±0.06	+0.2	Volts
			Am26LS33, $-15V \leq V_{CM} \leq +15V$	−0.5	±0.12	+0.5	
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +15V$, Other Input $-15V \leq V_{IN} \leq +15V$				2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15V$, Other Input $-15V \leq V_{IN} \leq +15V$				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $\Delta V_{IN} = +1.0V$	COM'L	2.7	3.4		Volts
		$V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., $\Delta V_{IN} = -1.0V$	$I_{OL} = 4.0mA$			0.4	Volts
		$V_{\overline{ENABLE}} = 0.8V$	$I_{OL} = 8.0mA$			0.45	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min., $I_{IN} = -18mA$				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	$V_O = 2.4V$			20	μA
			$V_O = 0.4V$			−20	
I_{IL}	Enable LOW Current	$V_{IN} = 0.4V$			−0.2	−0.36	mA
I_{IH}	Enable HIGH Current	$V_{IN} = 2.7V$			0.5	20	μA
I_I	Enable Input High Current	$V_{IN} = 5.5V$			1	100	μA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, V_{CC} = Max., $\Delta V_{IN} = +1.0V$		−15	−50	−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA
V_{HYST}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5.0V$, $V_{CM} = 0V$			30		mV
t_{PLH}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{PHL}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{LZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			20	30	ns
t_{HZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			15	22	ns
t_{ZL}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns
t_{ZH}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns

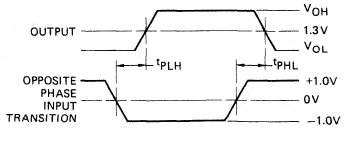
lote: 1. All typical values are $V_{CC} = 5.0V$, $T_A = 25°C$.

LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



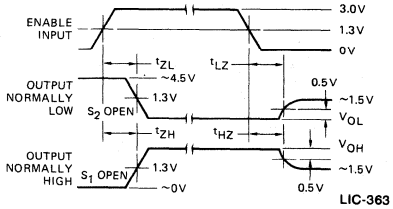
LIC-361

PROPAGATION DELAY (Notes 1 and 3)



LIC-362

ENABLE AND DISABLE TIMES (Notes 2 and 3)



LIC-363

Notes:

1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 15ns$; $t_f \leq 6.0ns$.

Am26LS32B

Quad Differential Line Receiver

DISTINCTIVE CHARACTERISTICS

- ± 100mV sensitivity over V_{IN} range of 0V to 5V
- ± 200mV sensitivity over V_{CM} range
- −7V to +12V input voltage range − differential or common mode
- Guaranteed input voltage hysteresis limits
  - 80mV minimum
  - 200mV maximum
- 3V maximum open circuit input voltage
- Three-state outputs disabled during power-up and power down
- Maximum guarantees for t_{PD} skew
- All AC and DC parameters guaranteed over COM'L and MIL operating temperature ranges
- Single +5V supply
- Advanced low-power Schottky processing
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

The Am26LS32B is a quad line receiver designed to meet the requirements of RS-422 and RS-423, CCITT V.10 and V.11, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

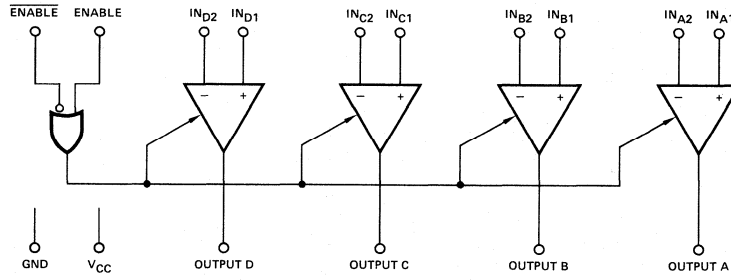
The Am26LS32B features an input sensitivity of 200mV over the common mode input voltage range of −7V to + 12V.

The Am26LS32B is the first device in the Am26LS32 configuration to guarantee minimum hysteresis and propagation delay skew while maintaining better propagation delay guarantees than the Am26LS32. This allows a more critical analysis of performance in high noise environments and better performance in terms of signal quality, resulting in better system performance.

The Am26LS32B provides an enable and disable function common to all four receivers. It features three-state outputs with 24mA sink capability and incorporates a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32B is constructed using Advanced Low-Power Schottky processing.

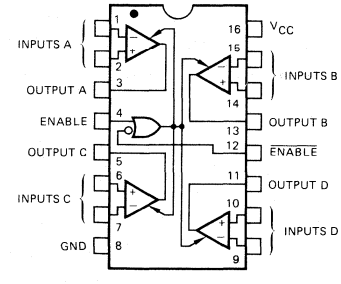
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32B Order Number
Hermetic DIP	−55 to +125°C	AM26LS32BDM
Flat Pak	−55 to +125°C	AM26LS32BFM
Dice	−55 to +125°C	AM26LS32BXM
Hermetic DIP	0 to +70°C	AM26LS32BDC
Molded DIP	0 to +70°C	AM26LS32BPC
Dice	0 to +70°C	AM26LS32BXC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	−65 to +165°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

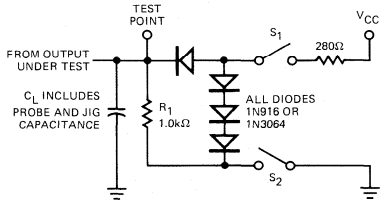
The following conditions apply unless otherwise specified:

Am26LS32XM (MIL) T_A = −55 to +125°C V_{CC} = 5.0V ± 10%
Am26LS32XC (COM'L) T_A = 0 to +70°C V_{CC} = 5.0V ± 5%

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	$0 \le V_{CM} \le +5V$	−100	±60	100	mV
			$-7V \le V_{CM} \le +12V$	−200		200	
V_{HYST}	Input Hysteresis			80	120	200	mV
V_{IOC}	Open Circuit Input Voltage			2.0		3.0	Volts
R_{IN}	Input Resistance	$-15V \le V_{CM} \le +15V$ (One input AC ground)		6.0	10		kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +15V, Other Input $-15V \le V_{IN} \le +15V$				2.3	mA
I_{IN}	Input Current (Under Test)	V_{IN} = −15V, Other Input $-15V \le V_{IN} \le +15V$				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min, Δ V_{IN} = +1.0V, $V_{\overline{ENABLE}}$ = 0.8V	I_{OH} = −12mA	2.0			Volts
			I_{OH} = −1mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = Min, Δ V_{IN} = −1.0V, $V_{\overline{ENABLE}}$ = 0.8V	I_{OH} = 16mA			0.4	Volts
			I_{OL} = 24mA			0.5	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			50	μA
			V_O = 0.4V			−50	
I_{IL}	Enable LOW Current	V_{IN} = 0.4V				−0.36	mA
I_{IH}	Enable HIGH Current	V_{IH} = 2.7V				20	μA
I_I	Input HIGH Current	V_{IN} = 5.5V				100	μA
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, Δ V_{IN} = +1.0V		−30	−65	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled			52	70	mA

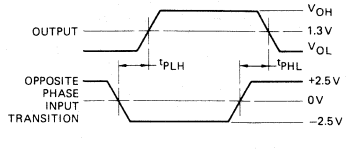
Note: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.

LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



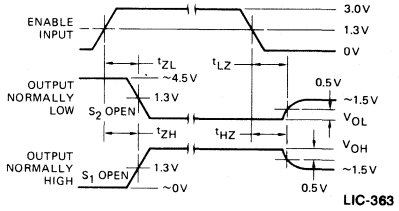
LIC-361

PROPAGATION DELAY (Notes 1 and 3)



LIC-362

ENABLE AND DISABLE TIMES (Notes 2 and 3)



LIC-363

Notes: 1. Diagram shown for Enable LOW.
2. S_1 and S_2 of Load Cricuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

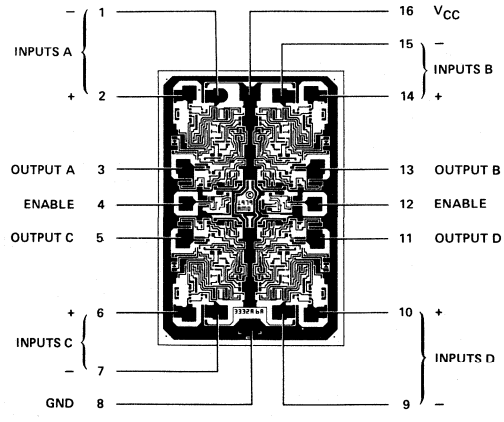
Parameters	Description	Min	Typ	Max	Units	Test Conditions
t_{PLH}	Propagation Delay, Input to Output		16	21	ns	C_L = 50pF See test circuit
t_{PHL}			17	21	ns	
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$		1.5	3.0	ns	
t_{ZL}	Output Enable Time, ENABLE to Output		16	22	ns	
t_{ZH}			10	16	ns	
t_{LZ}	Output Disable Time, ENABLE to Output		11	18	ns	C_L = 5pF See test circuit
t_{HZ}			13	18	ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Am26LS32B COM'L T_A = 0 to +70°C V_{CC} = 5.0V ± 10% Min	Am26LS32B COM'L Max	Am26LS32B MIL T_A = −55 to +125°C V_{CC} = 5.0V ± 10% Min	Am26LS32B MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay, Input to Output		26		26	ns	C_L = 50pF See test circuit
t_{PHL}			26		26	ns	
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$		4.0		4.0	ns	
t_{ZL}	Output Enable Time, ENABLE to Output		33		33	ns	
t_{ZH}			22		22	ns	
t_{LZ}	Output Disable Time, ENABLE to Output		27		27	ns	C_L = 5pF See test circuit
t_{HZ}			27		27	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" X 0.084"

USE OF THE Am26LS29, 30, 31 and 32 QUAD DRIVER/RECEIVER FAMILY IN EIA RS-422 AND 423 APPLICATIONS

By David A. Laws and Roy J. Levy

INTRODUCTION

Today's high-performance data processing systems demand significantly faster data communications rates than are possible with the EIA RS-232 specifications in use for the past ten years.

Two new standards prepared by the Electronic Industries Association address this need. EIA RS-423 is an unbalanced, bipolar voltage specification designed to interface with RS-232C, while greatly enhancing its operation. It permits the communication of digital information over distances of up to 2000 feet and at data rates of up to 300 Kilobaud. EIA RS-422 is a balanced voltage digital interface for communicaton of digital data over distances of 4000 feet or data rates of up to 10 megabaud.

Advanced Micro Devices has developed a family of monolithic Low-power Schottky quad line drivers and receivers to meet the requirements of these specifications.

The Am26LS29 and 30 line drivers and the Am26LS32 receiver meet all requirements of RS-423 while the Am26LS31 differential line driver and the Am26LS32 receiver meet the requirements of RS-422.

A second receiver element, the Am26LS33 is available for use in high common mode noise environments, exceeding the common mode voltage requirements of RS-422 and RS-423.

This application note reviews the use of these devices in implementing the new standards. Emphasis is given to the EIA RS-422 balanced interface.

EIA STANDARD SPECIFICATIONS

Two basic forms of operation are available for transmission of digital data over interconnecting lines. These are the single ended and differential techniques.

The single-ended form uses a single conductor to carry the signal with the voltage referenced to a single return conductor. This may also be the common return for other signal conductors. Figure 1a.

The single-ended form is the simplest way to send data as it requires only one signal line per circuit. This simplicity, however, is often offset by the inability of this form to allow discrimination between a valid signal produced by the driver, and the sum of the driver signal plus externally induced noise signals.

A solution to some of the problems inherent in the single-ended form of operation is offered by the differential form of operation. Figure 1b. This consists of a differential driver (essentially two single-ended drivers with one driver always producing the complementary output signal level to the other driver), a twisted pair transmission line and a differential line receiver. The driver signal appears as a differential voltage to the line receiver, while the noise signals appear as a common mode signal. The two signals, therefore, can be discriminated by a line receiver with a sufficient common mode voltage operating range.

The Electronic Industries Association, EIA, has defined a number of specifications standardizing the interface between data terminal equipment and data circuit terminating equipment based on both single-ended and differential operation.

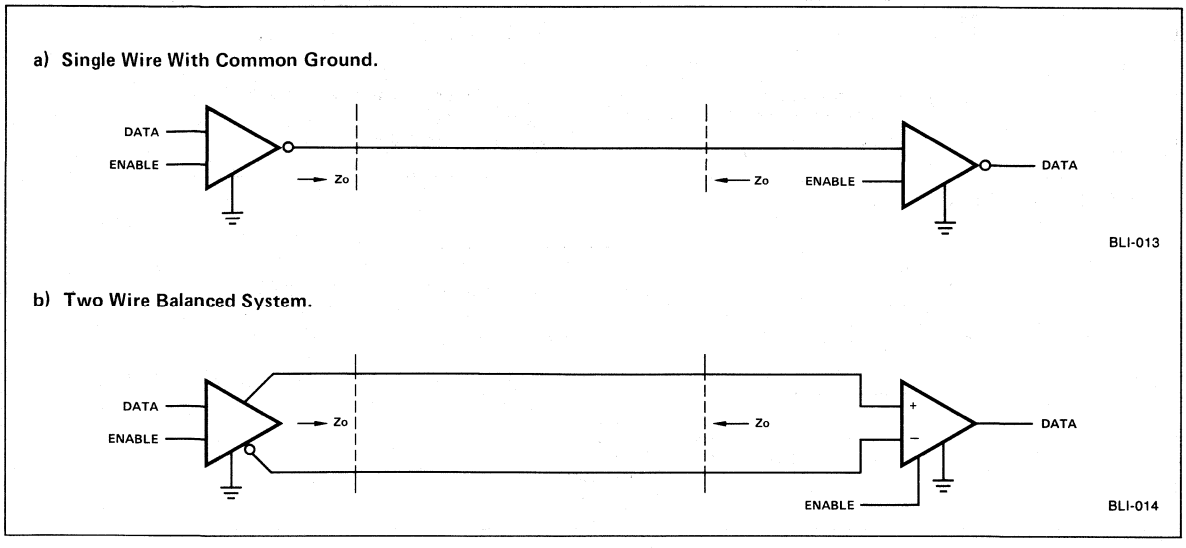


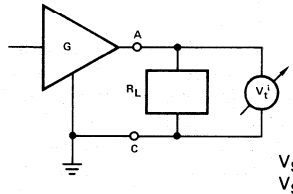
Figure 1. Data Communication Techniques.

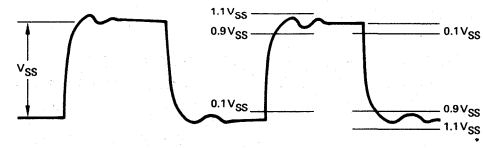
The most widely used standard for interfacing between data terminal equipment and data communications equipment today, is EIA RS-232C, issued in August 1969. The RS-232C electrical interface is a single-ended, bipolar-voltage, unterminated circuit. This specification is for serial binary data interchange over short distances (up to 50 feet) at low rates (up to 20 Kilobaud). It is a protocol standard as well as an electrical standard, specifying hand shaking signals and functions between terminal and the communications equipment. As already noted, single-ended circuits are susceptible to all forms of electromagnetic interference. Noise and cross talk susceptibility are proportional to length and bandwidth. RS-232C places restrictions on both. It limits slew rate of the drivers (30V/μs) to control radiated emission on neighboring circuits and allows bandwidth limiting on the receivers to reduce susceptibility to cross talk. The length and slew rate limits can adequately control reflections on unterminated lines, and the length and bandwidth limits are more than adequate to reduce susceptibility to noise.

Like EIA RS-232C, the new EIA RS-423 is also a single-ended, bipolar-voltage unterminated circuit. It extends the distance and data rate capabilities of this technique to distances of up to 4000 feet at data rates of 3000 baud, or at higher rates of up to 300 Kilobaud over a maximum distance of 40 feet.

EIA RS-422 is a differential, balanced voltage interface capable of significantly higher data rates over longer distances. It can accommodate rates of 100 Kilobaud over a distance of 4000 feet or rates of up to 10 megabaud. These performance improvements stem from the advantages of a balanced configuration which is isolated from ground noise currents. It is also immune to fluctuating voltage potentials between system ground references and to common mode electromagnetic interference. Figure 2 compares the driver output waveforms for the three EIA standard configurations, while Table I compares the key characteristics required by drivers and receivers intended for these applications. Since RS-232C has been in use for many years, RS-422 and 423 parameter values have been selected to facilitate an orderly transition from existing designs to new equipment.

a) EIA RS-232C Generator Output.

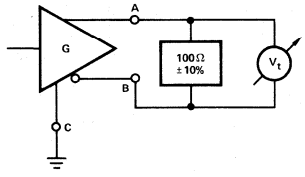


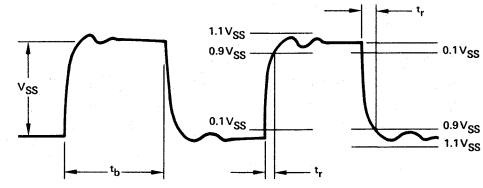


$V_{SS} = |V_t - \overline{V}_t|$
V_{SS} = Difference in steady state voltages
R_L = 3KΩ to 7KΩ
V_{SS} min. = ±5V; V_{SS} max. = ±25V

BLI-015

b) EIA RS-422 Generator Output.



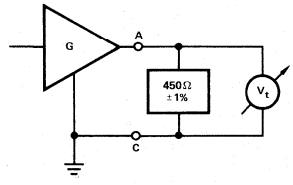


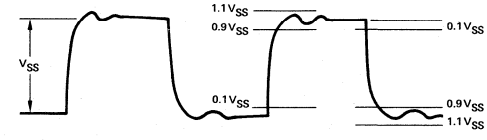
t_D = Time duration of the unit interval at the applicable modulation rate
$t_r \leq 0.1t_D$ when $t_D \geq 200ns$
$t_r \leq 20ns$ when $t_D < 200ns$

V_{SS} = Difference in steady state voltages
$V_{SS} = |V_t - \overline{V}_t|$
V_{SS} min. = 2V; V_{SS} max. = 6V

BLI-016

c) EIA RS-423 Generator Output.





$V_{SS} = |V_t - \overline{V}_t|$
V_{SS} = Difference in steady state voltages
V_{SS} min. = ±3.6V; V_{SS} max. = ±6V

BLI-017

Figure 2. Driver Output Waveforms.

TABLE I
KEY PARAMETERS OF EIA SPECIFICATIONS

Characteristics	EIA RS-232C	EIA RS-423	EIA RS-422	Units
Form of Operation	Single Ended	Single Ended	Differential	
Max. cable length	50	2000	4000	Feet
Max. data rate	20K	300K	10M	Baud
Driver output voltage, open circuit*	±25	±6	6 volts between outputs	Volts (Max.)
Driver output voltage, Loaded output*	±5 to ±15	±3.6	2 volts between outputs	Volts (Min.)
Driver output resistance power off	Ro = 300Ω	100μA between −6 to +6V	100μA between +6 and −.25V	Min.
Driver output short circuit current I_{SC}	±500	±150	±150	mA (Max.)
Driver output slew rate	30 V/μsec Max.	Slew rate must be controlled based upon cable length and modulation rate	No control necessary	
Receiver input resistance R_{in}	3K to 7K	≥4K	≥4K	Ω
Receiver input thresholds	−3 to +3	−0.2 to +0.2	−0.2 to +0.2	Volts (Max.)
Receiver input voltage	−25 to +25	−12 to +12	−12 to +12	Volts (Max.)

*± indicates polarity switched output.

INTEGRATED CIRCUIT CHARACTERISTICS

Most semiconductor manufacturers offer integrated circuits designed to satisfy the old RS-232C standard. A number of them have designs in progress to meet the new EIA specifications. Products available from Advanced Micro Devices to meet these needs are shown in Table II.

The Am26LS29, 30, 31 and 32 are a family of quad drivers and receivers designed specifically to meet the new EIA standards. These products utilize Low-Power Schottky technology to incorporate four drivers or four receivers, together with control logic, in the standard 16-pin package outlines.

The Am26LS29/30 and the Am26LS32 are driver and receiver pairs designed to implement the single-ended EIA RS-423 standard. The Am26LS31 is a differential line driver designed for use with the Am26LS32 receiver in a differential mode to meet EIA RS-422.

Am26LS29 AND Am26LS30 QUAD RS-423 LINE DRIVERS

The Am26LS29 and 30 consist of four single-ended line drivers designed to meet or exceed the requirements of RS-423. The buffered driver outputs are provided with sufficient source and sink current capability to drive 50 ohm to a virtual ground transmission line and high capacitive loads. The Am26LS29 has a three-state output control while the Am26LS30 has a Mode Control input that allows it to operate as a dual RS-422 driver (with suitable power supply changes), Figure 3.

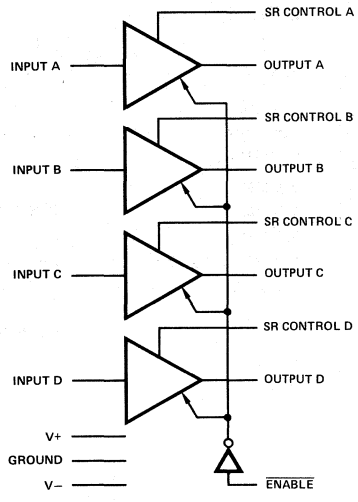
Each of the four driver inputs, as well as the $\overline{\text{Enable}}$/Mode Control input is a PNP Low-Power Schottky input for reduced input loading, one-half the normal fan-in. Since there are two inverters from each input to output, the driver is non-inverting. When operating in the RS-423 mode, the Am26LS29 and 30 require both +5V and −5V nominal value power supplies. This allows the outputs to swing symmetrically about ground – producing a true bipolar output. The Mode Control (Pin 4) of the Am26LS30 should be HI or tied to

TABLE II
ADVANCED MICRO DEVICES' EIA COMPATIBLE DEVICES

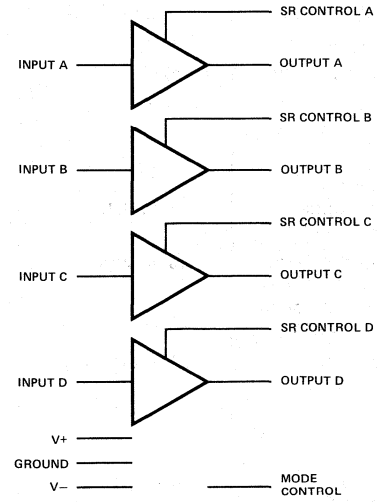
EIA Standard	Drivers	Receivers
RS-232C	Am1488 Quad Driver	Am1489, 1489A Quad Receivers with response control pin
	Am9616 Triple Driver with logic control	Am9617 Triple Receiver with optional hysteresis
	Am2616 Quad Driver also specified for CCITT V.24 and MIL-188C	Am2617 Quad Receiver specified over MIL range
RS-422	Am26LS31 Quad Differential with three-state control gating	Am26LS32 Quad Differential Driver single-ended Receiver
RS-423	Am26LS29 Quad Driver with three-state output Am26LS30 Quad Driver with slew rate control	Am26LS32 Quad single-ended/ Differential Receiver

a) Logic Diagrams

Am26LS29



Am26LS30
RS-423 Operation (Mode Control HIGH)



b) Circuit Diagram for Am26LS30

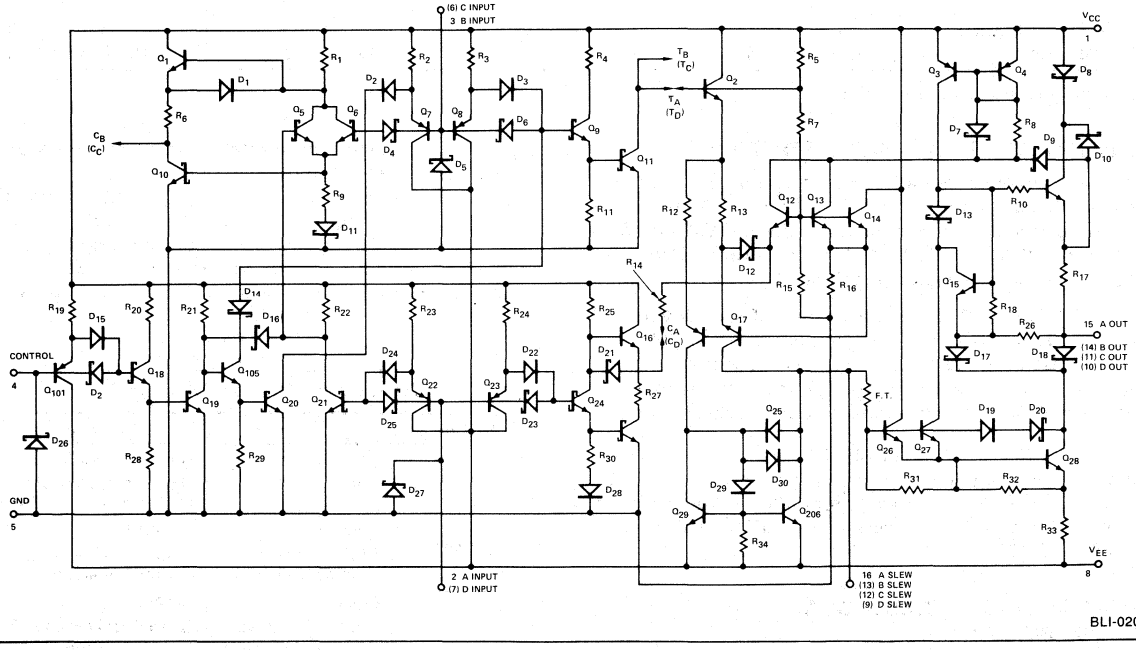


Figure 3. Am26LS29 and Am26LS30 Drivers.

V_{CC}. Each output is designed to drive the RS-423 load of 50 ohms with an output voltage equal or greater than +3.6 volts in the HI state and −3.6 volts in the LO state. Each output is current limited to 150mA max. in either logic state. A Slew Rate control pin is brought out separately for each output to allow output ramp rate (rise and fall time) control. This provides suppression of near end cross talk to other receivers in the cable. Connecting a capacitor from this node to that driver's respective output will produce a ramp (10% to 90%) of 50ns typical for each picofarad of capacitance in that capacitor. RS-423 establishes recommended ramp rates versus length of line driven and modulation rate, Figure 4.

The Am26LS30 can be used at low data rates as a dual EIA RS-422 driver with three-state outputs by connecting the V_{EE} supply and the mode control input to ground.

Am26LS31 QUAD RS-422 DRIVER

The Am26LS31 is a quad differential line driver designed to meet the RS-422 specification while operating with a single +5 volt supply. A common enable and disable function controls all four drivers, Figure 5. The driver features high speed, de-skewed differential outputs with typical propagation delays of 12ns and residual skew of 2ns. Both differential line outputs are designed for three-state operation to allow two-way half duplex and multiplex, data bus applications.

Table III is a summary of the essential requirements of the RS-422 standard. Section A describes the key characteristics satisfied by the Am26LS31 driver.

The balanced differential line driver consists of two halves, each of which is similar to a Low-power Schottky TTL gate with equal source and sink current capability. The two halves are emitter coupled in a differential input configuration. One side of the input circuit is tied to a fixed TTL bias threshold and the other side is tied to a sink diode in normal DTL/TTL fashion. This configuration offers complementary outputs with very low skew, dependent only upon component matching, a necessity to meet RS-422.

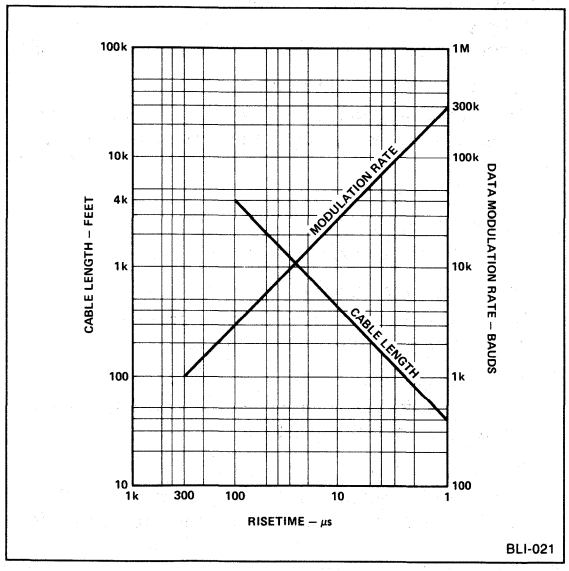


Figure 4. Data Modulation Rate or Cable Length Versus Risetime for EIA RS-423.

The circuit diagram of the driver is shown in Figure 6. The emitter-coupled input circuit is formed by Q2 and Q3, which are biased by a current source. This source is a current mirror, formed by Q1 which supplies the current, and D6 which is diode connected transistor matched to Q1. The fixed bias for Q3, formed by D5 and D6, is $2V_{BE}$. A $2V_{BE}$ bias, less the D2 Schottky diode drop, provides the normal Low-power Schottky TTL threshold, V_{IL} = 0.7V. R19 provides a boost to 0.8V for a full 400mV TTL noise margin. The differential outputs of the emitter coupled stage, A and $\overline{A}$, drive emitter followers Q14 and Q15, which provide the required speed and matching characteristics. The emitter followers, drive phase splitters Q4 and Q5, which in turn drive totem-pole outputs. The outputs at the line interface are of standard Low-power Schottky TTL configuration, except that circuit values are modified to provide high sourcing capability. The outputs are designed to source or sink 20mA each, so that they can generate a voltage of at least 2.0V across a 100 ohm load, as required by RS-422. Additional circuitry has been included to make the line outputs three-state for two-way bus applications. The Am26LS31 meets the RS-422 requirement that the driver not load the line in the powered down condition ($I_X \leq 100\mu A$) or if the power supply to that device should fail.

Am26LS32 QUAD RS-422 AND 423 RECEIVER

The Am26LS32 is a quad line receiver which, operating from a single 5 volt supply, can be used in either differential or single-ended modes to satisfy RS-422 and 423 applications respectively. A complementary enable and disable feature, similar to that on the driver, controls all four receivers, Figure 7. The device's three-state outputs, which can sink 8mA, incorporate a fail-safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 meets the receiver input specification of Table III, a 200mV threshold sensitivity with common mode rejection exceeding the supply line potentials, (greater than 7 volts). The same design feature of the input circuit which provides the common mode rejection also insures excellent power supply ripple rejection, which is important when switching the high currents involved in a system's interfaces. Furthermore, unlike operational amplifiers, where the DC common mode and power supply rejection ratios roll off with open loop gain, the full rejection capability of this line receiver is maintained at high frequencies. The receiver hysteresis of typically 30mV, provides differential noise immunity. Signals received on long lines can have slow transition times, and without hysteresis, a small amount of noise around the switching threshold can cause errors in the receiver output.

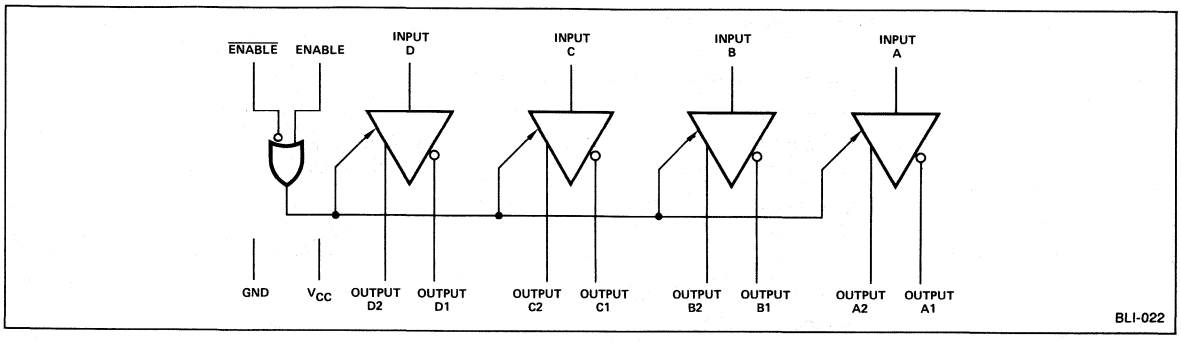


Figure 5. Am26LS31 Logic Diagram.

TABLE III
SUMMARY OF EIA RS-422 STANDARD FOR A BALANCED DIFFERENTIAL INTERFACE

A. Line Driver

Open Circuit Voltage (either logic state)
- Differential: $|V_{do}| \leq 6.0V$
- Common Mode: $|V_{cmo}| \leq 3.0V$

Differential Output Voltage (across 100 ohm load)
- Either logic state: $|V_d| \geq \max(0.5V_{do}, 2.0V)$

Output Impedance
- Either logic state: $R_G \leq 100$ ohms

Mark-Space Level Symmetry (across 100 ohm load)
- Differential: $|V_{dS}| - |V_{dM}| \leq 0.4V$
- Common Mode: $|V_{cmS}| - |V_{cmM}| \leq 0.4V$

Output Short Circuit Current (to ground)
- Either Output: $|I_{SC}| \leq 150mA$

Output Leakage Current (power off)
- Voltage Range: $-0.25V \leq V_x \leq +6.0V$
- Either Output at V_x: $|I_X| \leq 100\mu A$

Rise and Fall Times (across 100 ohm load)
- T = Baud Interval: $(t_r, t_f) \leq \max(0.1T, 20ns)$

Ringing (across 100 ohm load)

Definitions

$V_{dSS} = V_d$ (steady state)

$V_{SS} = V_{dS} - V_{dM}$ (steady state)

Limits (either logic state)
- Percentage: $|V_d - V_{dSS}| \leq 0.1V_{SS}$
- Absolute: $2.0V \leq |V_d| \leq 6.0V$

B. Line Receiver

Signal Voltage Range
- Differential: $|V_d| \leq 6.0V$
- Common Mode: $|V_{cM}| \leq 7.0V$

Single-Ended Input Current (power ON or OFF)
- Either Input at V_x: $|V_x| = 10V$
- Other Input Grounded: $|I_V| \leq 3.25mA$

Single-Ended Input Bias Voltage (other input grounded)
- Either Input Open Circuit: $|V_B| \leq 3.0V$

Single-Ended Input Impedance (other input grounded)
- Either Input: $R_L \geq 4000$ ohms

Differential Threshold Sensitivity
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$
- Either Logic State: $|V_T| \leq 200mV$

Absolute Maximum Input Voltage
- Differential: $|V_d| \leq 12V$
- Single-Ended: $|V_x| \leq 10V$

Input Balance (threshold shift)
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$

Differential Threshold (500 ohms in series with each input)
- Either Logic State: $|V_t| \leq 400mV$

Termination (optional)
- Total Load Resistance (differential): $R_T > 90$ ohms

Multiple Receivers (bus applications)

Up to 10 receivers allowed. Differential threshold sensitivity of 200mV must be maintained.

Hysteresis (optional)

As required for applications with slow rise/fall time at receiver, to control oscillations.

Fail Safe (optional)

As required by application to provide a steady MARK or SPACE condition under open connector or driver power OFF condition.

C. Interconnecting Cable

Type

Twisted Pair Wire or Flat Cable Conductor Pair

Conductor Size
- Copper Wire (solid or stranded): 24 AWG or larger
- Other (per conductor): R ≤ 30 ohms/1000 ft.

Capacitance
- Mutual Pair: C ≤ 20pF/ft.
- Stray: C ≤ 40pF/ft.

Pair-to-Pair Cross Talk (balanced)
- Attenuation at 150KHz: A ≥ 40dB

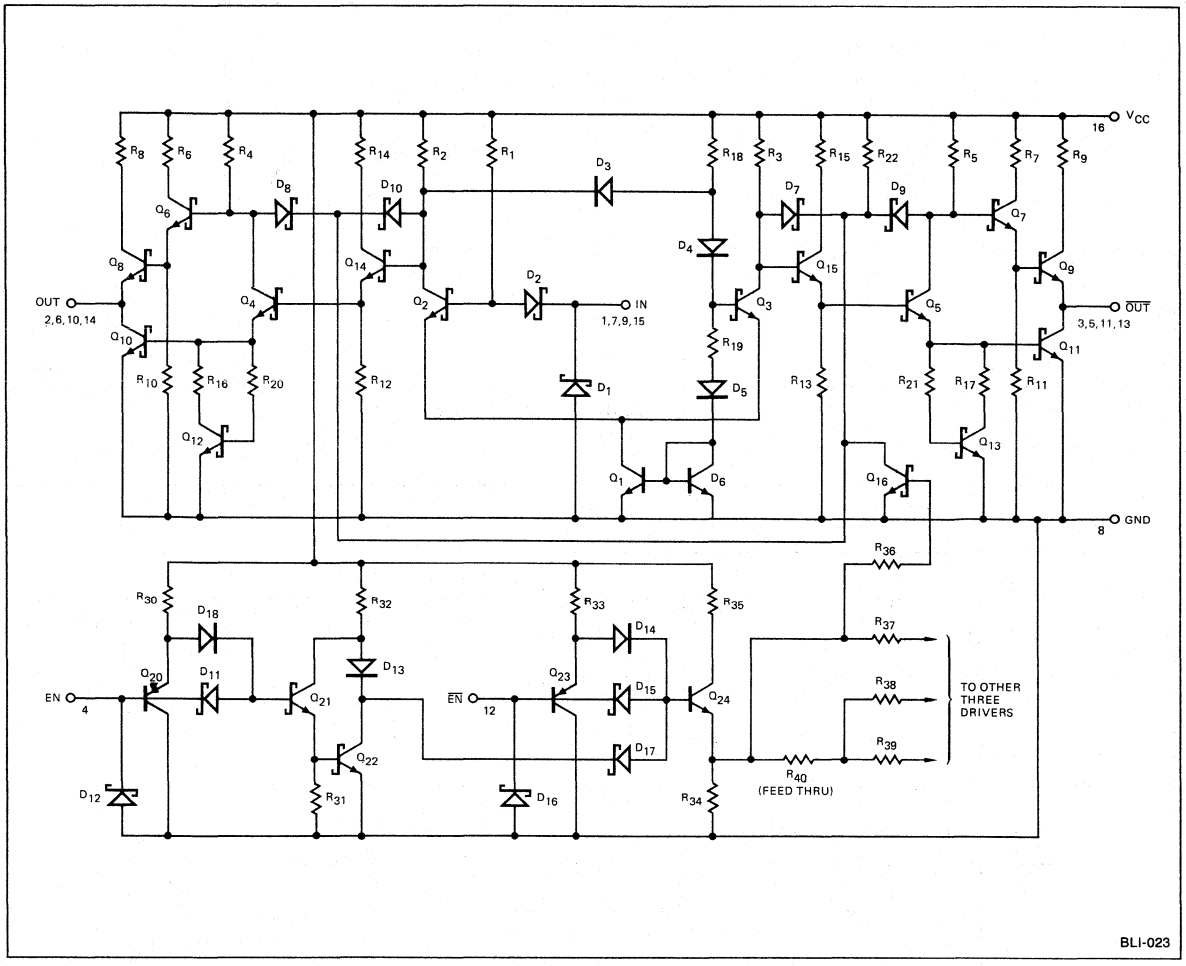


Figure 6. Am26LS31 Circuit Diagram (Only one driver shown).

The balanced differential line receiver is a three-stage circuit. The input stage consists of a low-impedance differential current amplifier with series resistor inputs to convert line signal voltage to current and provide a moderate input impedance. The input resistors provide an impedance greater than 6K on each input, power on or power off, which exceeds the requirements of RS-422 and RS-423. This is one advantage of the current amplifier input circuit. Another advantage is that is can operate with immunity to common mode voltages above V_{CC} and below ground. The differential threshold sensitivity of this circuit is 200mV, as required by RS-422. The second stage is a differential voltage amplifier, which interfaces to the single-ended output stage through an emitter follower. The output stage is a standard Low-power Schottky TTL totem-pole output with three-state capability.

The full circuit is shown in Figure 8. Resistors R_{20} and R_{21}, which connect the non-inverting input to V_{CC} and the inverting input to ground, provide the fail-safe feature, which guarantees a HIGH logic state for the receiver output when there is no signal on the line. The differential voltage amplifier in the second stage is formed by Q6 and Q3 which are biased by current source Q9. The hysteresis in the receiver switching characteristic is provided by Q4 and Q5, a differential pair biased by current source Q6, whose collectors are connected in positive feedback to the input pull-up circuits. A small amount of current is switched by Q4 and Q5, which must be overcome by the different voltage signal, resulting in the hysteresis. The output stage is driven from one side of the differential second stage by emitter follower Q17, which is a multiple emitter transistor. the second emitter is the control point for the three-state output.Q17 drives the phase splitter Q12, which in turn drives the three-state totempole output. The remainder of the circuit is the output enable control logic. This three-state capability on the receiver TTL side of the interface is a useful feature for modularizing two-way bus design.

A mask option of the input resistors (R_1, R_2, R_{20} and R_{21}) modifies the receiver characteristics to improve operation in high common mode noise environments. This device, known as the Am26LS33, has these resistors at twice the value of the Am26LS32. An input differential or common mode voltage range of ±15 volts is achieved at the expense of a minor decrease of input threshold sensitivity, to ±500mV from ±200mV.

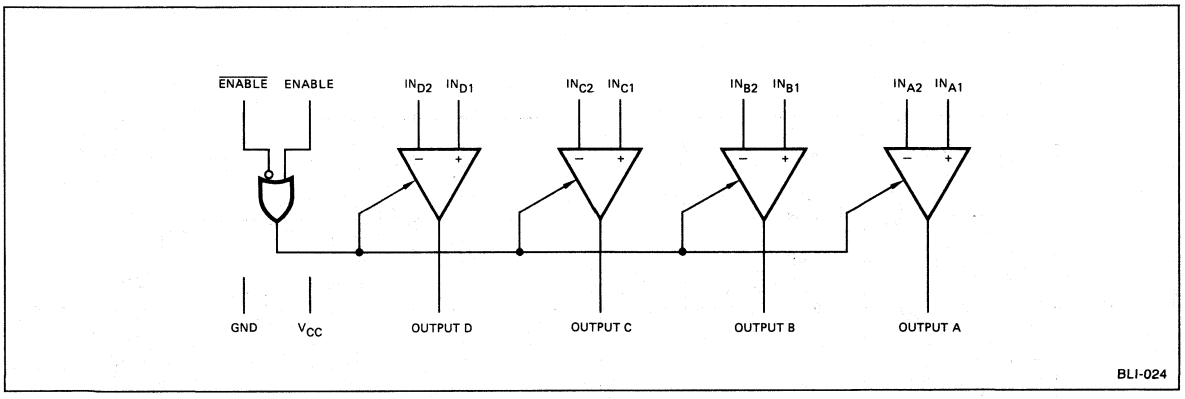
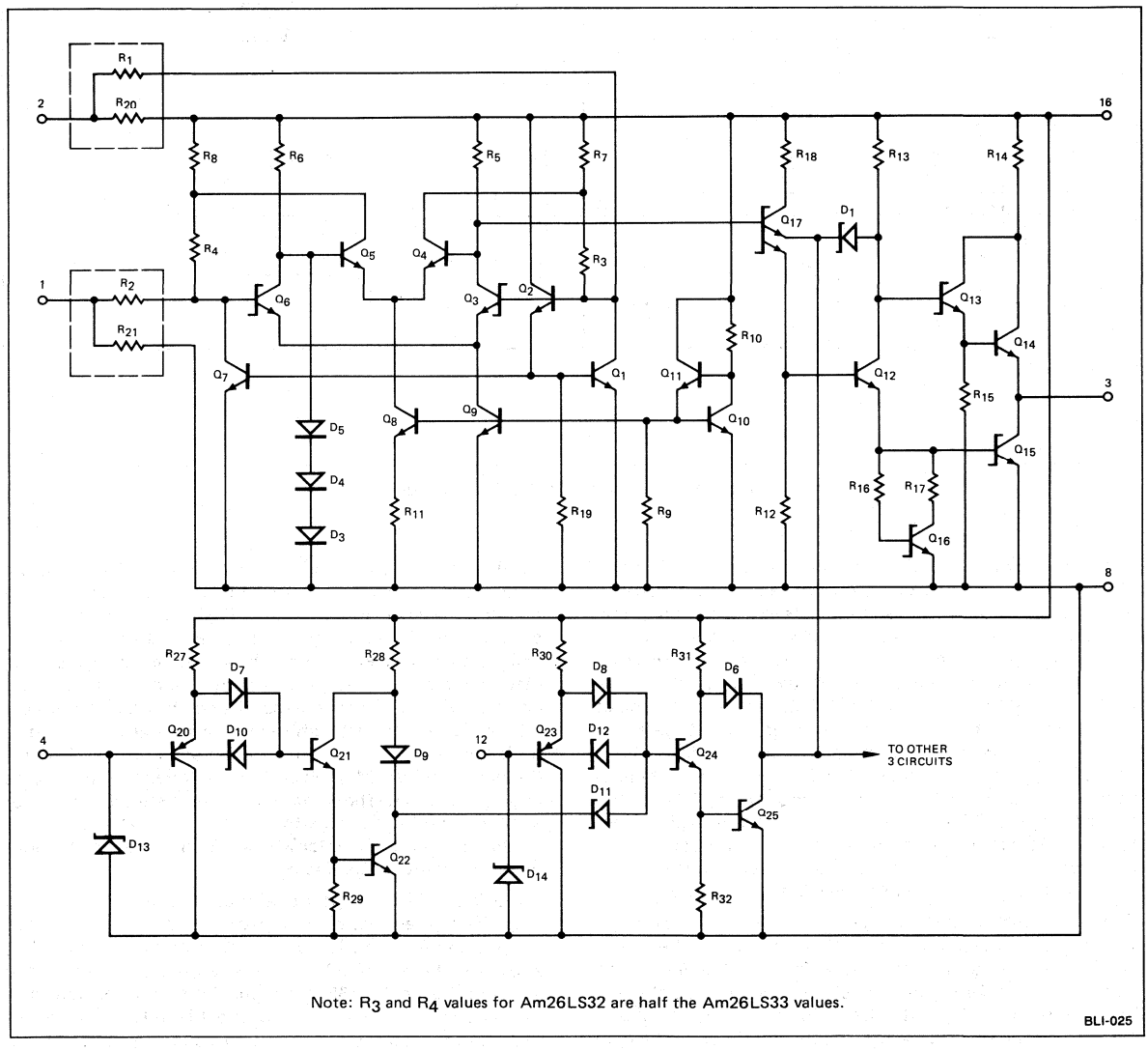


Figure 7. Am26LS32 Logic Diagram.



Note: R_3 and R_4 values for Am26LS32 are half the Am26LS33 values.

Figure 8. Am26LS32 and Am26LS33 Circuit Diagram (Only one receiver shown).

APPLICATIONS IN MIXED RS-232 AND 422/3 SYSTEMS

A system implemented with the RS-422 differential output cannot be used to drive an RS-232C system directly. An RS-423 single-ended driver, such as the Am26LS29 or Am26LS30, may be used provided certain precautions are observed.

1. Although the RS-423 driver output specification of between 4 to 5V does not meet the RS-232C specification of 6V, operation is usually satisfactory with RS-232C receivers. This is achieved because the short cable lengths permitted by RS-232C cause very little signal degredation and because of the low source impedance of the RS-423 driver.
2. RS-232C specifies that the rise time for the signal to pass through the ±3.0V transition region shall not exceed 4% of the signal element duration. RS-423 requires much slower rise times, specified from 10% to 90% of the total signal amplitude, to reduce cross talk for operation over longer distances. Therefore, the RS-423 driver in the equipment must be waveshaped. This is achieved by selection of a capacitor value for the Am26LS30 to simultaneously meet the requirements of both RS-423 and RS-232C for data rates covered by RS-232C.
3. RS-423 specifies one common return ground for each direction of transmission, RS-232C requires only one for both directions of transmission. Care must be taken to insure that a return ground path has been created when interfacing between the two systems.
4. RS-232C does not require termination, while it may be necessary for RS-422 and 423. Detailed consideration of termination is covered in the next section.

Note that RS-422 and RS-423 specifies that receivers should not be damaged by voltages up to 12V, while RS-232C allows drivers to produce output voltages up to 25V. The Am26LS32 receiver has been designed to avoid this hazard and can withstand input voltages of ±25 volts.

RS-422 TRANSMISSION LINE FEATURES

Any time a receiver and transmitter are connected with more than a few inches of a wire, problems due to reflections can arise if care is not exercised to terminate the line correctly. RS-422 describes the cable as a twisted pair of approximately 120Ω impedance terminated in a resistor R_T. R_T is not specified because there are two extreme values which may be chosen for the two following general classes of usage: (1) single direction transmission; and (2) multi-direction and multiple source transmission (party line). Considering the cable impedance only, the termination should equal the cable impedance of 120Ω. However this reduces the terminated cable resistance as seen by the driver to only 60Ω, with resulting loading of the output signal. This loading causes a reduction of S/N ratio at the received terminal due to the decrease in signal voltage swing. The solution lies in a compromise between an R_T of 120Ω which provides maximum power transfer at a reduced S/N ratio or R_T of 240Ω which causes a mis-match of 2-to-1 but no S/N reduction. The choice is left to the user as it is system dependent. Both schemes will work for an average line length and should only approach the margins at maximum line length and maximum bit rates.

Electronic Industries Association, when preparing EIA Standard RS-422 conducted their tests with 24 gauge twisted pair wire. The resulting length vs. data rate, is published as a guideline in RS-422 (Figure 9). This shows two important results: (1) Unmodulated baseband (NRZ) signalling is not recommended at distances greater than 4000 feet; (2) At data

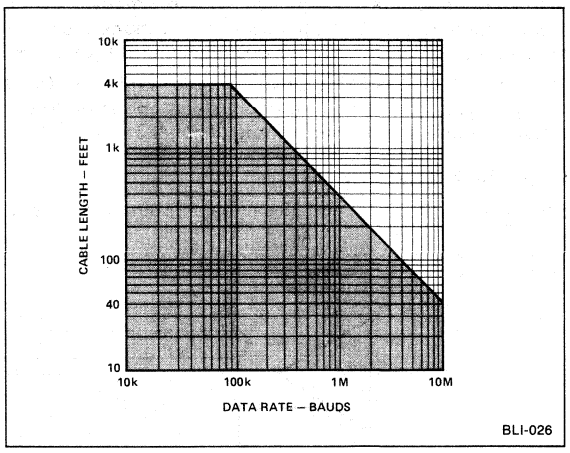


Figure 9. Data Rate Versus Cable Length for Balanced, Twisted Pair Cable (From EIA RS-422).

rates above about 100KHz, the maximum cable length for acceptable signal quality is inversely proportional to data rate.

Result (1) above is due to the DC resistance of the cable. For a 4000 foot cable with a DC resistance of 30 ohms/1000 feet, the DC series loop resistance is 240Ω. The minimum allowable terminated differential load impedance is 90Ω. The DC voltage attentuation is 90/(90 – 240) = 1/4(6db), which is arbitrarily chosen as the maximum allowable limit.

Result (2) is due to line losses. Laboratory tests using the 26LS31 Line Driver connected to the 26LS32 Line Receiver by 800 feet of ordinary 20 AWG twisted pair (Beldon #8205 plastic-jacketed wire), terminated in its characteristic impedance of 100Ω were evaluated. The input waveform was a 500KHz square wave with (10% to 90%) rise and fall times of less than 10ns. The output waveform produced rise and fall times which together accounted for approximately one-half the period ($t_r + t_f$ = 500ns). This was due to line loss and constant capacity. The energy per cycle of the output waveform is approximately 25% lower than that of the input. The input rise and fall times are not a function of line length, assuming matching termination. The output rise and fall times are dependent upon length in a complex manner. Furthermore, it can be shown by observation that they build up along the line.

Many good reference sources are available on the subject of transmission lines (References 1, 2, 3 and 4). These will provide background information to the following discussion.

Seshadri in Reference (1) has analyzed a line with series resistance losses and has shown that rise time varies with the square of the length. This shows series resistance to be a function of the square root of frequency. However when one tries to use this result in combination with the previous result, it becomes apparent just how difficult the problem is. In Reference (2), the authors point out that skin depth implies a frequency dependent series inductance as well as resistance, and that one cannot be considered without the other.

They go on to show how this leads to the same result; namely that rise and fall times vary with the square of distance.

No attempt will be made to explain here why Figure 5 shows maximum length varying inversely with frequency rather than with the square of frequency. Certainly many complex factors are involved. Our laboratory observations showed a dependence somewhere in between linear and square law.

The Am26LS31 Quad Line Driver and the Am26LS32 Quad Line Receiver are capable of good, clean operation to the distance limits and data rate limits of RS-422.

SYSTEM APPLICATIONS

The Am26LS30, 31, 32 and 33 can be combined in various signaling networks. Using Am26LS29, Am26LS30 and Am26LS32, Figure 10, a unidirectional RS-423 communication can be constructed. Allowing for the voltage variation described earlier, RS-232C requirements can be satisfied. It should be noted that the Am26LS29 or Am26LS30 is used above to meet the bipolar requirements. If a single-ended line, Figure 11, is required without a bipolar requirement, the Am26LS31 can be used by biasing the reference terminal of the receiver to approximately 1.5 volts. Note that additional resistors will enhance fail safe operation.

Figure 12 shows the use of the Am26LS31 and Am26LS32 to meet a balanced line, single direction RS-422 application. If bidirectionality is required, an additional termination should be added as shown in Figure 13.

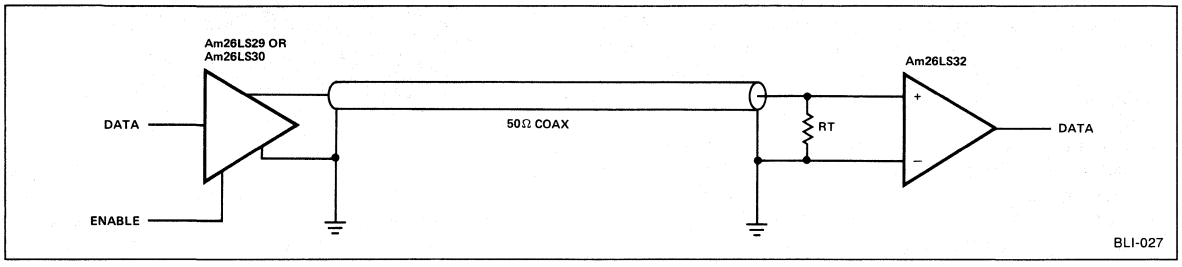


Figure 10. Unidirectional RS-423 (partial RS-232C).

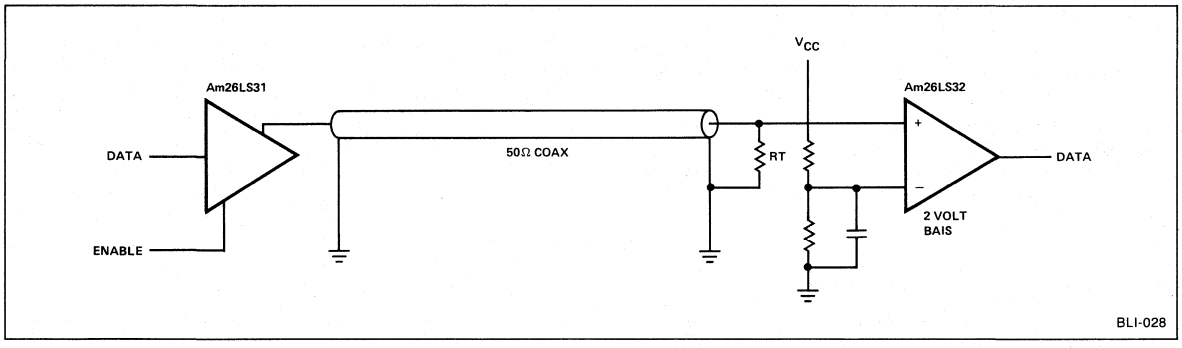


Figure 11. Single-Ended Line Without Bipolar Requirement.

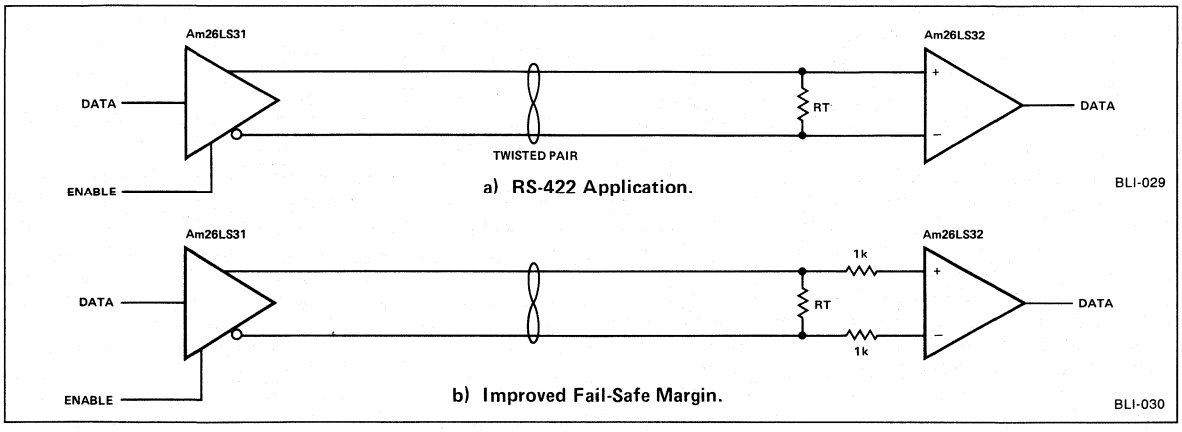


Figure 12.

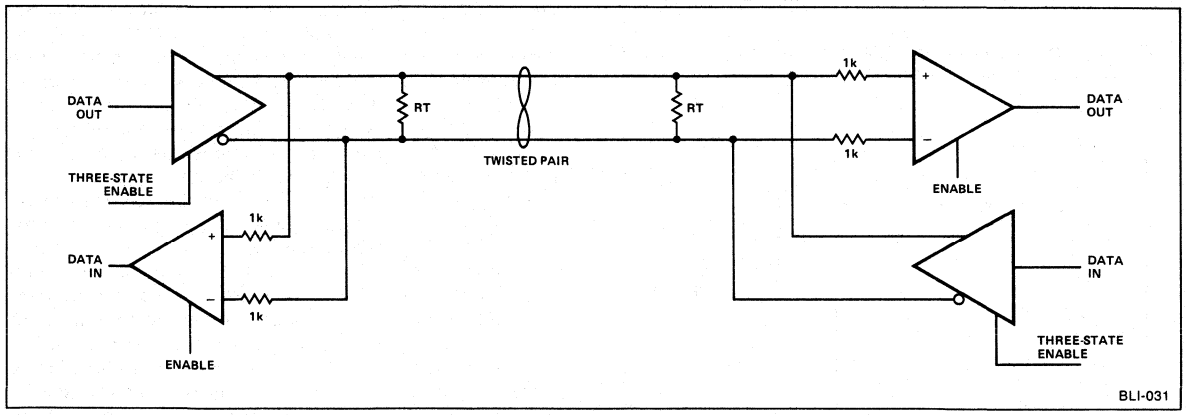


Figure 13. Bidirectional RS-422.

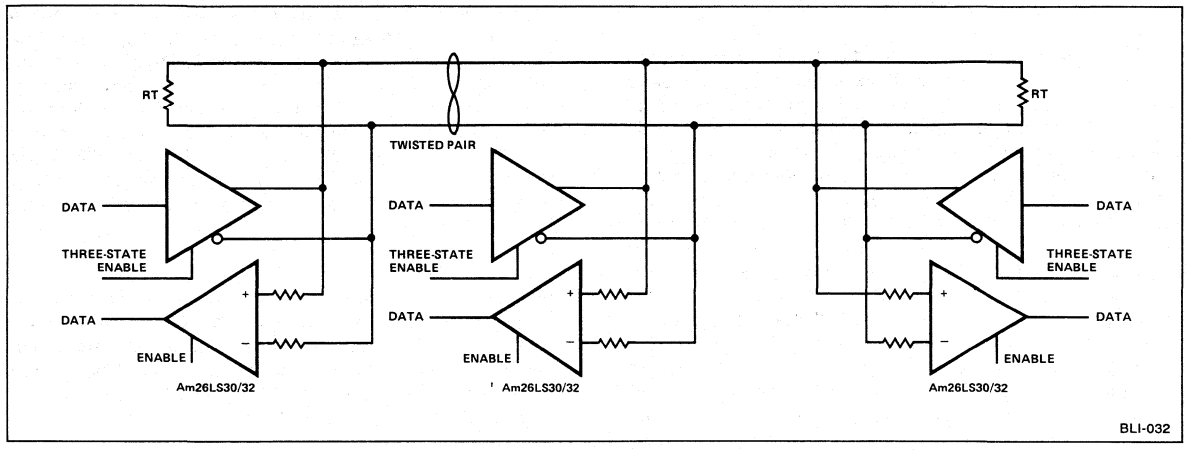


Figure 14. Party Line Configuration.

a) Full Duplex Four-Wire Data Communication RS-422 Interface (with Data Modem).

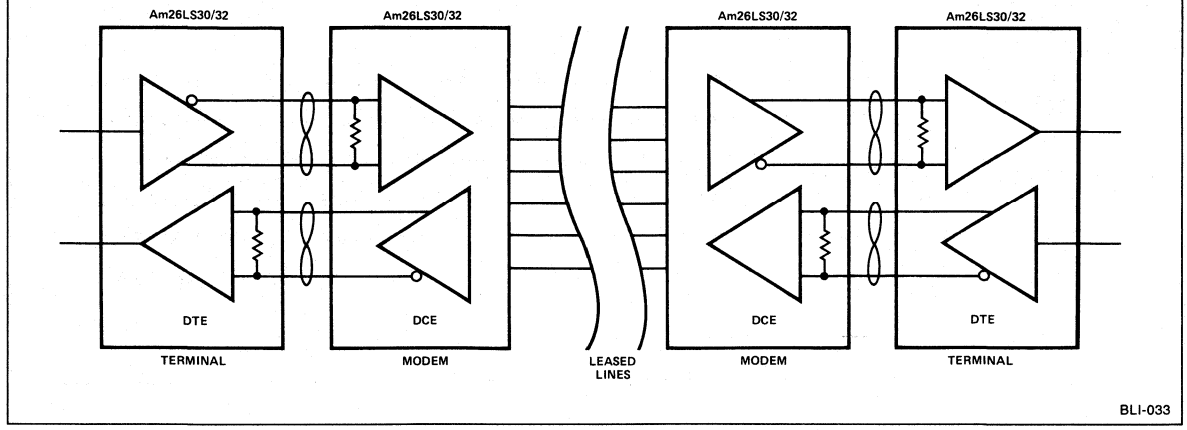


Figure 15.

b) Full Duplex Four-Wire Data Communication RS-422 Interface (without Data Modem).

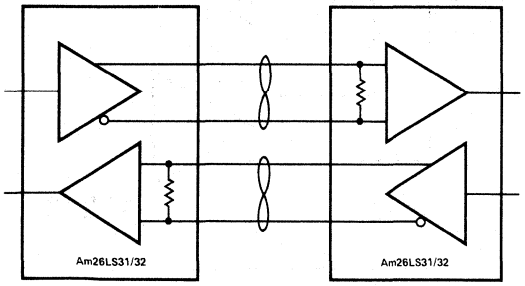


Figure 15. (Cont.)

The high speed capability of RS-422 has attracted the interest of many computer designers for use in the party line mode (Figure 14). The most common usage is that of a four wire full duplex exchange system (Figure 15). This mode of operation involves two pairs of wires each handling a single direction of traffic. The outgoing direction consists of one driver (Am26LS30 or Am26LS31) and n receivers (Am26LS32 or Am26LS33). The incoming direction consists of one receiver (Am26LS32 or Am26LS33) and n drivers (Am26LS30 or Am26LS31). This seems extremely simple to organize. However, problems arise when system ground is considered. If the network of receiver and driver span a moderate to long physical distance, ground loop noise or differences are developed changing the voltage that appears at the terminals of all receivers and drivers except for the one driver that is active. It remains the system reference as long as it is active. This induced or system developed voltage is referred to as Common Mode voltage (CMV) and as such must be considered as a device parameter. All manufacturers specify CMV capability of their receiver in compliance with RS-422 (approx. 7 volts plus signal) but there is no specification for drivers. If the dimensions of the system are short compared to 1/4 wave length of the maximum date rise and fall times, the CMV can be assumed to be minimal and drivers with single voltage supply and limited negative CMV can be used, i.e., Am26LS31. If the system dimensions are large, the CMV will cause problems in that the driver will clamp to the ground the moment the collective or apparent voltage swings below minus 0.5 volts relative to the driver ground, causing a short in the line and increasing level shift and noise. The clamping is caused in part by conduction of the I/C substrate diode. The problem can be avoided by using a driver with an output common mode range (Am26LS30). The Am26LS30 guarantees an output CMV range of ±10 volts about the driver ground reference. New international standards are under consideration to specify this mode of operation. In conclusion, a good system of 4 wire full duplex for data communication would use as an outgoing pair an Am26LS30 line driver and up to 12 – Am26LS32 line receivers, with a termination at the near and far ends of the cable. The same system would use as an incoming pair an Am26LS32 line receiver and up to 32 – Am26LS30 line drivers with only one enabled at a time and all others in three-state mode with cable termination at both near and far ends of the cable.

Many other applications are possible using this family of devices. Although the designs are based on the requirements of the EIA data communications specifications, they are not limited to these situations. Aircraft buses and internal equipment interconnections will benefit from the features offered by these products.

REFERENCES

1. Seshadri, S. R., Fundamental of Transmission Lines and Electromagnetic Fields, (U. of Wisconsin), Addison-Wesley, Reading, Mass., 1971.
2. Adler, R. B., L. J. Chu, and R. M. Fano, Electromagnetic Energy Transmission and Radiation, (MIT), John Wiley & Sons, New York, 1963.
3. Matick, R. E., Transmission Lines for Digital and Communication Networks, (IBM), McGraw-Hill, New York, 1969.
4. Reference Data for Radio Engineers, (ITT), Fifth Edition, Howard W. Sams & Company, Indianapolis, 1974.
5. Electronic Industries Association, 2001 Eye Street, N.W. Washington, D.C., RS Standard Proposal, RS-232C, August, 1969.
6. Electronic Industries Association, 2001 Eye Street, N.W. Washington, D.C., RS Standard Proposal 1220, Rev. RS-422, September 21, 1976.
7. Electronic Industries Association, 2001 Eye Street, N.W. Washington, D.C., RS Standard Proposal 1221, Rev. RS-423, September 21, 1976.

Am26LS34
Quad Differential Line Receiver

DISTINCTIVE CHARACTERISTICS

- Meets all requirements of EIA Standards RS-422, RS-423, CCITT V.10 and V.11, and the new party line standard in development under EIA Project Number 1360.
- ± 200mV sensitivity over input voltage range
- ± 150mV sensitivity for V_{CM} = 0
- −7V to +12V common mode input voltage range
- 12kΩ minimum input impedance
- Maximum guarantees for t_{PD} skew
- All AC and DC parameters guaranteed over MIL and COM'L temperature ranges
- Guaranteed input voltages hysteresis limits
  - 120mV minimum
  - 300mV maximum
- No internal failsafe
- Pin compatible with Am26LS32/32B/33

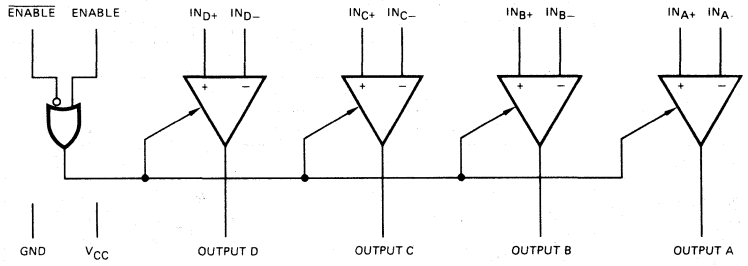
FUNCTIONAL DESCRIPTION

The Am26LS34 is a high performance, quad, differential line receiver. It has higher impedance and higher input voltage hysteresis than the similar Am26LS32B. The Am26LS34 also does not have internal fail-safe to allow greater user flexibility.

Input threshold sensitivity is specified for three different V_{CM} ranges. The improved sensitivity, guaranteed hysteresis and skew limits allow a more critical analysis of system performance in high noise environments and better system performance capability.

All performance parameters are guaranteed over ±10% supplies and over the operating temperature range. In addition, I_{OL} is specified to 24mA for easy system bus interfacing.

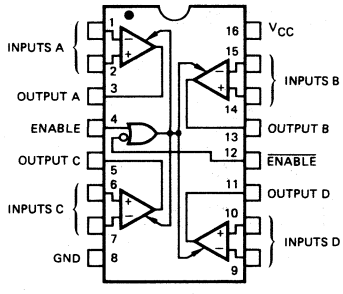
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am26LS34 Order Number
Hermetic DIP	−55 to +125°C	AM26LS34DM
Flat Pak	−55 to +125°C	AM26LS34FM
Dice	−55 to +125°C	AM26LS34XM
Hermetic DIP	0 to +70°C	AM26LS34DC
Molded DIP	0 to +70°C	AM26LS34PC
Dice	0 to +70°C	AM26LS34XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Voltage	±25V
Differential Input Voltage	30V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	−65 to +165°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

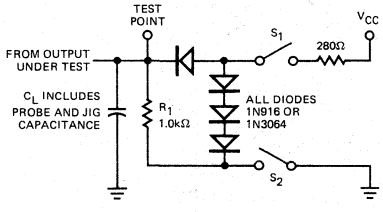
The following conditions apply unless otherwise specified:

(MIL) T_A = −55 to +125°C V_{CC} = 5.0V ± 10%
(COM'L) T_A = 0 to +70°C V_{CC} = 5.0V ± 5%

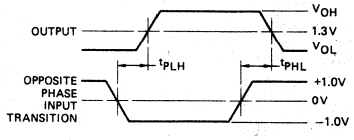
Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{TH}	Differential Input Voltage	V_{OUT} = V_{OL} or V_{OH}	V_{CM} = 0V	−150	±90	+150	mV
			−7V ≤ V_{CM} ≤ +12V	−200		+200	
			−15V ≤ V_{CM} ≤ +15V	−400		+400	
V_{HYST}	Input Hysteresis			120	180	300	mV
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ +15V (One input AC ground)		12k	20k	40k	Ω
I_{IN}	Input Current (Under Test)	V_{IN} = +12V			0.7	1.0	mA
I_{IN}	Input Current (Under Test)	V_{IN} = −7V			−0.5	−0.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min, Δ V_{IN} = +1.0V, $V_{\overline{ENABLE}}$ = 0.8V	−12mA	2.0			Volts
			−1mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min, Δ V_{IN} = −1.0V, $V_{\overline{ENABLE}}$ = 0.8V	I_{OH} = 16mA			0.4	Volts
			I_{OL} = 24mA			0.5	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA				−1.5	Volts
V_{IOC}	Open Circuit Input Voltage			2.0		3.0	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			50	μA
			V_O = 0.4V			−50	
I_{IL}	Enable LOW Current	V_{IN} = 0.4V			−0.03	−0.2	mA
I_{IH}	Enable HIGH Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Enable Input High Current	V_{IN} = 5.5V			1	100	μA
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, Δ V_{IN} = +1.0V		−30	−65	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled			52	70	mA

Note: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.

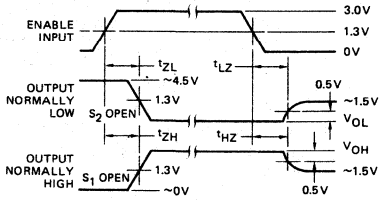
LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



PROPAGATION DELAY (Notes 1 and 3)



ENABLE AND DISABLE TIMES (Notes 2 and 3)



Notes: 1. Diagram shown for Enable LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator Rate ≤ 1.0MHz; Z_o = 50Ω; t_r, t_f ≤ 2.5ns.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

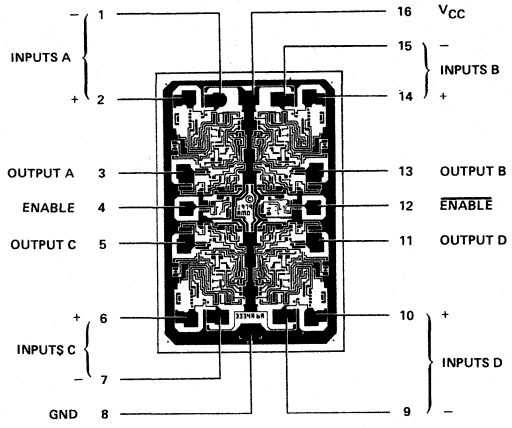
Parameters	Description	Min	Typ	Max	Units	Test Conditions
t_{PLH}	Propagation Delay, Input to Output		18	24	ns	C_L = 50pF See test circuit
t_{PHL}			20	24	ns	
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$		2	4	ns	
t_{ZL}	Output Enable Time, ENABLE to Output		16	22	ns	
t_{ZH}			10	16	ns	
t_{LZ}	Output Disable Time, ENABLE to Output		11	18	ns	C_L = 5pF See test circuit
t_{HZ}			13	18	ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Am26LS34 COM'L T_A = 0 to +70°C V_{CC} = 5.0V ± 10% Min	Am26LS34 COM'L Max	Am26LS34 MIL T_A = −55 to +125°C V_{CC} = 5.0V ± 10% Min	Am26LS34 MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay, Input to Output		30		30	ns	C_L = 50pF See test circuit
t_{PHL}			30		30	ns	
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$		±5		±5	ns	
t_{ZL}	Output Enable Time, ENABLE to Output		33		33	ns	
t_{ZH}			22		22	ns	
t_{LZ}	Output Disable Time, ENABLE to Output		27		27	ns	C_L = 5pF See test circuit
t_{HZ}			27		27	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" X 0.084"

High Performance Bus Interface Index

Am26S02

Schottky Dual Retriggerable, Resettable Monostable Multivibrator

Distinctive Characteristics

- Advanced Schottky technology with PNP inputs
- Retriggerable 0% to 100% duty cycle
- 28 ns to ∞ output pulse width range
- 100kΩ maximum timing resistor value
- Am26S02XM typical pulse width change of only 1.0% over −55°C to +125°C with R_X = 100kΩ.
- Am26S02XC typical pulse width change of only 0.4% over 0°C to +70°C with R_X = 100kΩ

FUNCTIONAL DESCRIPTION

The Am26S02 is a dual DC level sensitive, retriggerable, resettable monostable multivibrator built using advanced Schottky technology. The output pulse duration and accuracy depend on the external timing components of each multivibrator. The Am26S02 features PNP inputs to reduce the input loading.

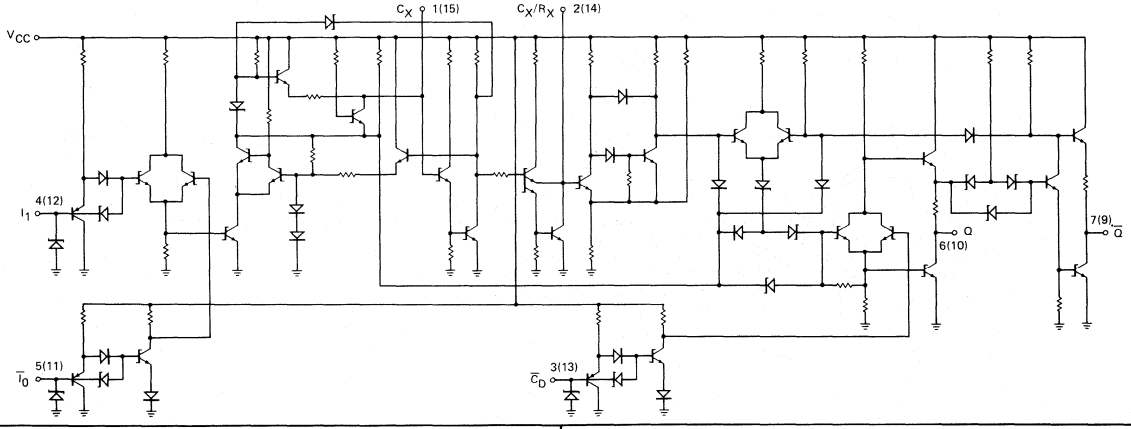
Provision is made on each multivibrator circuit for triggering the PNP inputs on either the rising or falling edge of an input signal by including an inverting and non-inverting trigger input. These PNP inputs are DC coupled making triggering independent of the input rise or fall time. Each time the monostable trigger input is activated from the OR trigger gate, full pulse length triggering occurs independent of the present state of the monostable.

The direct clear PNP input allows a timing cycle to be terminated at any time during the cycle. A LOW on the clear input forces the Q output LOW regardless of the $\overline{I_0}$ or I_1 inputs.

The Am26S02XM has a typical pulse width change of only 1.0% over the full military −55°C to +125°C temperature range and the Am26S02XC has a typical pulse width change of only 0.4% over the commercial 0°C to +70°C temperature range with a R_X = 100kΩ.

5

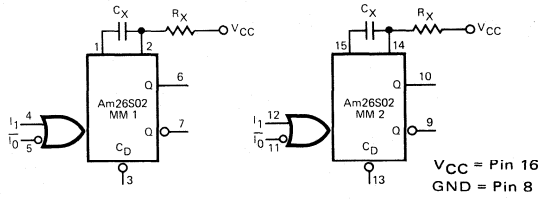
SCHEMATIC DIAGRAM
(One Monostable Multivibrator Shown)



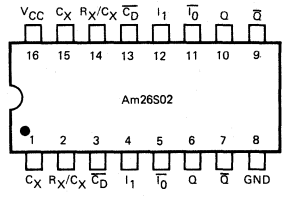
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to + 70°C	AM26S02PC
Hermetic DIP	0°C to + 70°C	AM26S02DC
Dice	0°C to + 70°C	AM26S02XC
Hermetic DIP	−55°C to +125°C	AM26S02DM
Hermetic Flat Pak	−55°C to +125°C	AM26S02FM
Dice	−55°C to +125°C	AM26S02XM

LOGIC SYMBOLS



CONNECTION DIAGRAM



Note:
Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7.
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +5.5
DC Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5.0 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am26S02XC	T_A = 0°C to +70°C	V_{CC} = 5.0 V ±5% (COM'L)	MIN. = 4.75 V	MAX. = 5.25 V
Am26S02XM	T_A = −55°C to +125°C	V_{CC} = 5.0 V ±10% (MIL)	MIN. = 4.5 V	MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2mA V_{IN} = V_{IH} or V_{IL}	2.5	2.8		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}		0.38	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA		−0.8	−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		−0.15	−0.4	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		0.1	20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 1.0V T_A = 25°C Only	−8	−15	−35	mA
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, I_{IX} = 0.33 mA (Notes 5 & 6)		48	69	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with pin 5 and 11 grounded and I_{IX} applied to pins 2 and 14.
6. I_{IX} is the current into the $R_X C_X$ node to simulate R_X.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	$\overline{I_0}$ to Q		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF, R_X = 5kΩ, C_X = 0 pF		13	20	ns
t_{PHL}	$\overline{I_0}$ to $\overline{Q}$				15	23	ns
t_{PLH}	I_1 to Q				12	20	ns
t_{PHL}	I_1 to $\overline{Q}$				12	20	ns
t_{PLH}	Clear to $\overline{Q}$				21		ns
t_{PHL}	Clear to Q				9	13	ns
t_{pw}	Pulse Width	$\overline{I_0}$ HIGH or I_1 LOW		20	10		ns
		$\overline{I_0}$ LOW or I_1 HIGH		16	7		ns
		Clear LOW		24	16		ns
t_s	Clear Recovery (inactive) to Trigger			−10	−22		ns
t_{pwQ} (Min.)	Minimum Pulse Width Q Output		V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0 pF R_L = 1.0 kΩ	27	33	39	ns
t_{pwQ}	Pulse Width Q Output		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF (CK05 Type)	3.23	3.42	3.61	μs
R_X	Timing Resistor		0°C to 70°C	5		100	kΩ
			−55°C to +125°C	5		50	

DEFINITION OF FUNCTIONAL TERMS:

$\overline{C_D}$ Asynchronous direct CLEAR. A LOW on the clear input resets the monostable regardless of the other inputs.

$\overline{I_0}$ Active-LOW input. With I_1 LOW, a HIGH-to-LOW transition will trigger the monostable.

I_1 Active-HIGH input. With $\overline{I_0}$ HIGH, a LOW-to-HIGH transition will trigger the monostable.

Q The TRUE monostable output.

$\overline{Q}$ The Complement monostable output.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{C_D}$	I_1	$\overline{I_0}$	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	L	↓	⎍	⎍
H	X	L	L	H
H	↑	H	⎍	⎍

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
↓ = HIGH-to-LOW Transition
⎍ = LOW-HIGH-LOW Pulse
⎍ = HIGH-LOW-HIGH Pulse
X = Don't Care

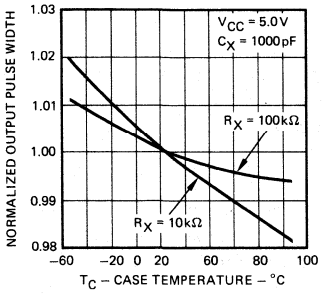
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
C_X	Mono 1 1	–	–	–
R_X/C_X	2	–	–	–
$\overline{C_D}$	3	0.4	–	–
I_1	4	0.4	–	–
$\overline{I_0}$	5	0.4	–	–
Q	6	–	40	10
$\overline{Q}$	7	–	40	10
GND	8	–	–	–
$\overline{Q}$	Mono 2 9	–	40	10
Q	10	–	40	10
$\overline{I_0}$	11	0.4	–	–
I_1	12	0.4	–	–
$\overline{C_D}$	13	0.4	–	–
R_X/C_X	14	–	–	–
C_X	15	–	–	–
V_{CC}	16	–	–	–

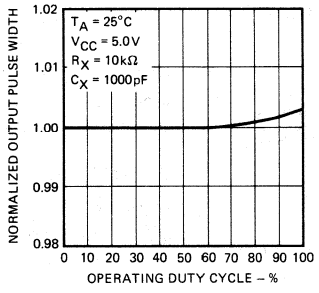
A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

5

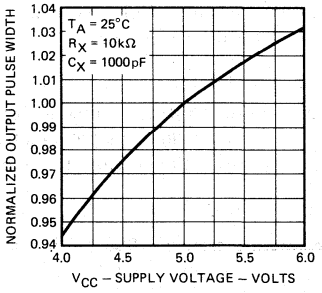
Typical Normalized Output Pulse Width Versus Case Temperature



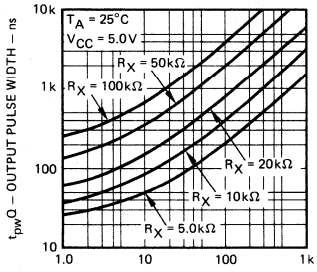
Normalized Output Pulse Width Versus Operating Duty Cycle



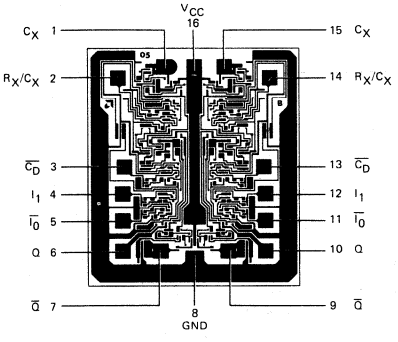
Typical Normalized Output Pulse Width Versus Supply Voltage



Output Pulse Width Versus External Timing Capacitance



Metallization and Pad Layout



DIE SIZE 0.062" X 0.071"

OPERATION RULES

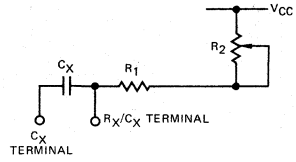
TIMING

1. Timing components C_x and R_x values.

Operating Temperature Range

	0°C to 70°C	-55°C to +125°C
R_x MIN.	5kΩ	5kΩ
R_x MAX.	100kΩ	50kΩ
C_x	any value	any value

2. Remote adjustment of timing.



$R_1 + R_2 = R_x$

$R_1 \geq R_x$ MIN.

$R_2 < R_x$ MAX. $- R_1$

In the above arrangement, R_1 and C_x should be as close as possible to the device pins to minimize stray capacitance and external noise pickup. The variable resistor R_2 can be located remotely from the device if reasonable care is used.

3. Pulse width change measurements.

The pulse width $t_{pw}Q$ is specified and measured with components of better than 0.1% accuracy. If measurements are made with reduced component tolerances, the expected accuracy should be adjusted accordingly. Note that pulse width temperature stability improves as R_x increases.

4. Timing for $C_x \leq 1000$ pF.

When using capacitor of less than or equal to 1000 pF in value, the output pulse width should be determined from the output pulse width versus external timing capacitance graph.

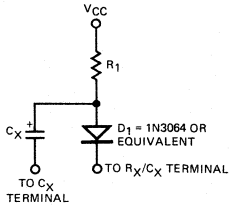
5. Timing for $C_x > 1000$ pF.

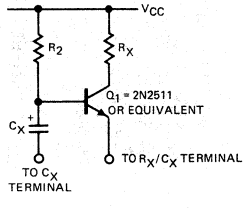
For capacitors of greater than 1000 pF in value, the output pulse width, $t_{pw}Q$, is determined by

$$t_{pw}Q = 0.30\, C_x R_x \left(1 + \frac{0.11}{R_x}\right)$$

where

R_x is in kilohms
C_x is in picofarads
$t_{pw}Q$ is in nanoseconds





$R_1 \leq 0.6 \times R_x$ MAX.

$R_2 < 0.7 \times h_{FEQ1} \times R_x$

6. Protection of electrolytic timing capacitors.

If the electrolytic capacitor to be used as C_x cannot withstand 1.0 volt reverse bias, one of the two circuit techniques shown below should be used to protect the electrolytic capacitor from the reverse voltage. The accuracy of the pulse width may be dependent on the diode (transistor) characteristics.

The output pulse width, $t_{pw}Q$ for the diode circuit modifies the previous timing equation as follows:

$$t_{pw}Q = 0.26\, C_x R_x \left(1 + \frac{0.13}{R_x}\right)$$

The output pulse width for the transistor circuit is

$$t_{pw}Q = 0.21\, C_x R_x \left(1 + \frac{0.16}{R_x}\right)$$

Notice that the transistor circuit allows values of timing resistor R_2 larger than the R_x MIN. $< R_x <$ R_x MAX. to obtain longer output pulse widths for a given C_x.

TRIGGER AND RETRIGGER

1. Triggering.

The minimum pulse width signal into input $\overline{I}_0$ or input I_1 to cause the device to trigger is 20ns. Refer to the truth table for the appropriate input conditions.

2. Retriggering.

The retriggered pulse width, $t_{pwr}Q$, is the time during which the output is active after the device is retriggered during a timing cycle. It differs from the initial pulse width $t_{pw}Q$ timing equation as follows.

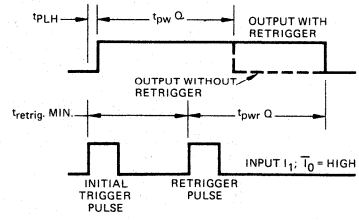
$$t_{pwr}Q = t_{pw}Q + t_{PLH}$$

where t_{PLH} is the propagation delay time from the $\overline{I}_0$ or I_1 input to the output. Note that t_{PLH} is typically 14ns and therefore becomes relatively unimportant as $t_{pw}Q$ increases.

3. Rapid retriggering.

A minimum retriggering time does exist. That is, the device cannot be retriggered until a minimum recovery time has elapsed. The minimum retrigger time is approximately.

t_{retrig} MIN. $= 0.2\, C_x$
C is in picofarads
t is in nanoseconds



CLEAR

A LOW on the clear inputs terminates the timing cycle. A new trigger cycle cannot be initiated while the clear is LOW. With the clear HIGH, the device is under the command of the I_1 and $\overline{I}_0$ inputs.

Am26S10 • Am26S11

Quad Bus Transceivers

Distinctive Characteristics

Input to bus is inverting on Am26S10
Input to bus is non-inverting on Am26S11
Quad high-speed open collector bus transceivers
Driver outputs can sink 100mA at 0.8V maximum

- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am26S10 and Am26S11 are quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

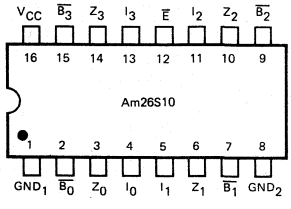
The Am26S10 and Am26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

ORDERING INFORMATION

Package Type	Temperature Range	Am26S10 Order Number	Am26S11 Order Number
Molded DIP	0°C to +70°C	AM26S10PC	AM26S11PC
Hermetic DIP	0°C to +70°C	AM26S10DC	AM26S11DC
Dice	0°C to +70°C	AM26S10XC	AM26S11XC
Hermetic DIP	–55°C to +125°C	AM26S10DM	AM26S11DM
Hermetic Flat Pack	–55°C to +125°C	AM26S10FM	AM26S11FM
Dice	–55°C to +125°C	AM26S10XM	AM26S11XM

CONNECTION DIAGRAMS

Top Views



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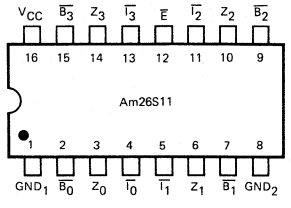
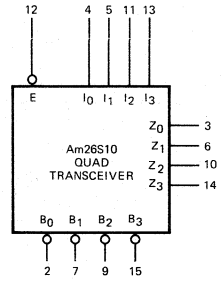


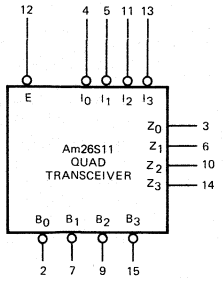
LIC-369

Note: Pin 1 is marked for orientation.

LOGIC SYMBOLS



LIC-370

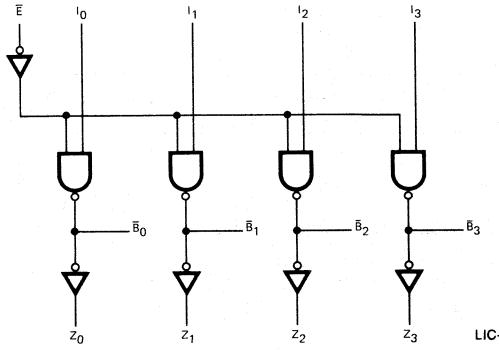


LIC-371

V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

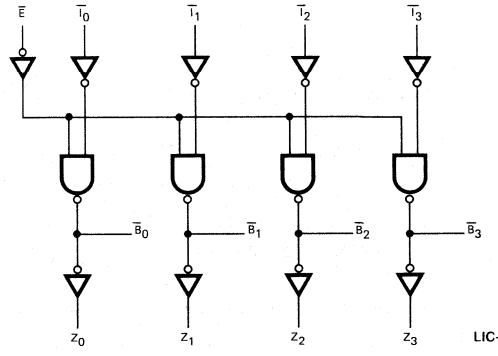
LOGIC DIAGRAMS

Am26S10



LIC-372

Am26S11



LIC-373

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Am26S10XC, Am26S11XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am26S10XM, Am26S11XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OH} = −1.0mA, V_{IN} = V_{IL} or V_{IH}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IL} or V_{IH}				0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V	Enable			20	μA
			Data			30	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX. (Note 3)	MIL	−20		−55	mA
			COM'L	−18		−60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX., Enable = GND	Am26S10		45	70	mA
			Am26S11			80	

Bus Input/Output Characteristics

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA		0.33	0.5	Volts
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
			COM'L	I_{OL} = 40mA		0.33	0.5	
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.		V_O = 0.8V			−50	μA
			MIL	V_O = 4.5V			200	
			COM'L	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V, V_{CC} = MAX		MIL	2.4	2.0		Volts
				COM'L	2.25	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V, V_{CC} = MIN		MIL		2.0	1.6	Volts
				COM'L		2.0	1.75	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data Input to Bus	Am26S10	R_B = 50Ω C_B = 50pF (Note 1)		10	15	ns
t_{PHL}					10	15	
t_{PLH}		Am26S11			12	19	
t_{PHL}					12	19	
t_{PLH}	Enable Input to Bus	Am26S10			14	18	ns
t_{PHL}					13	18	
t_{PLH}		Am26S11			15	20	
t_{PHL}					14	20	
t_{PLH}	Bus to Receiver Out		R_B = 50Ω, R_L = 280Ω C_B = 50pF (Note 1), C_L = 15pF		10	15	ns
t_{PHL}					10	15	
t_r	Bus		R_B = 50Ω C_B = 50pF (Note 1)	4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1. Includes probe and jig capacitance.

TRUTH TABLES

Am26S10

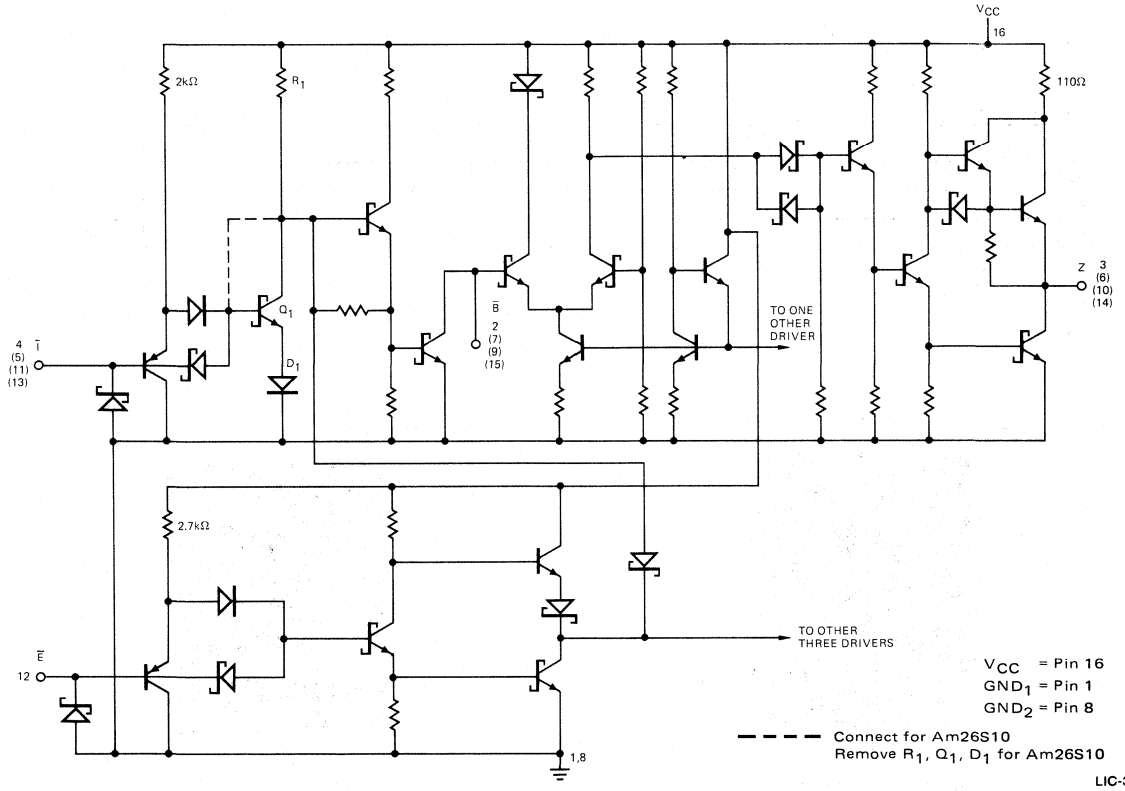
Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

Am26S11

Inputs		Outputs	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

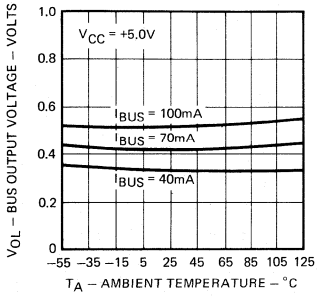
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

Am26S10/Am26S11 SCHEMATIC DIAGRAM



TYPICAL PERFORMANCE CURVES

Typical Bus Output Low Voltage Versus Ambient Temperature



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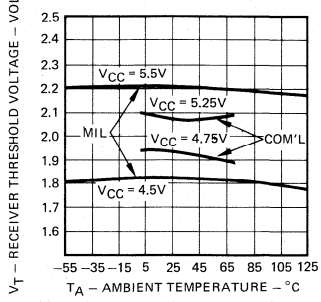
Receiver Threshold Variation Versus Ambient Temperature



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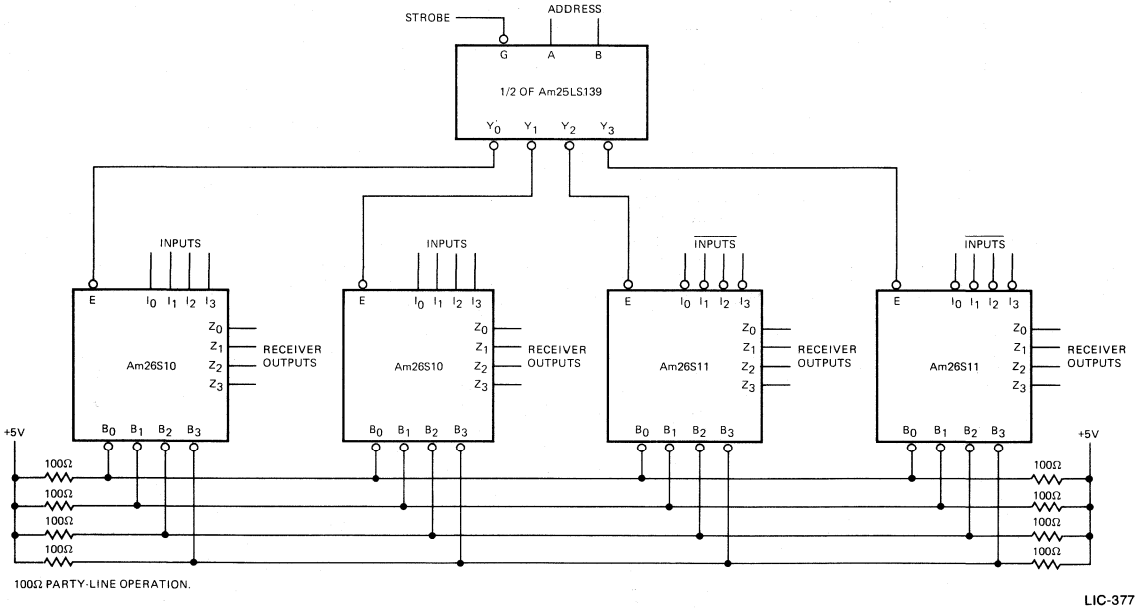
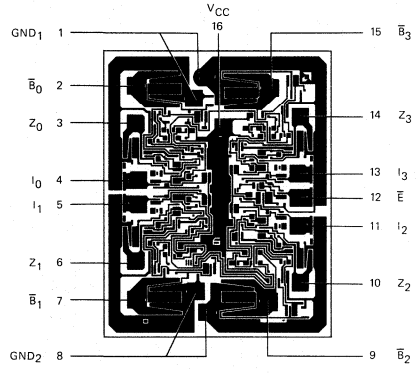
TYPICAL APPLICATION



LIC-377

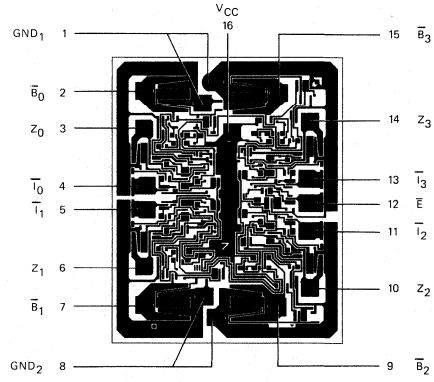
Metallization and Pad Layout

Am26S10



DIE SIZE 0.059" X 0.075"

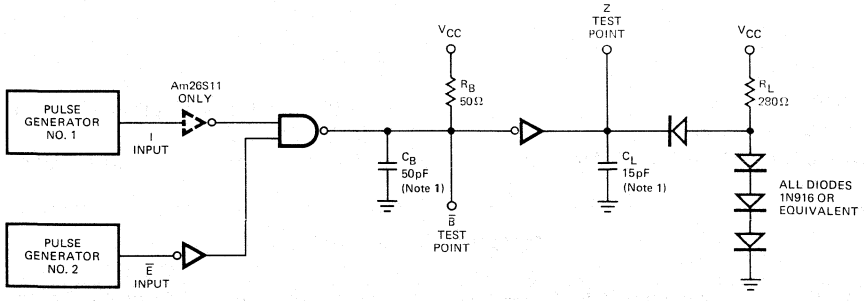
Am26S11



DIE SIZE 0.059" X 0.075"

SWITCHING CHARACTERISTICS

TEST CIRCUIT



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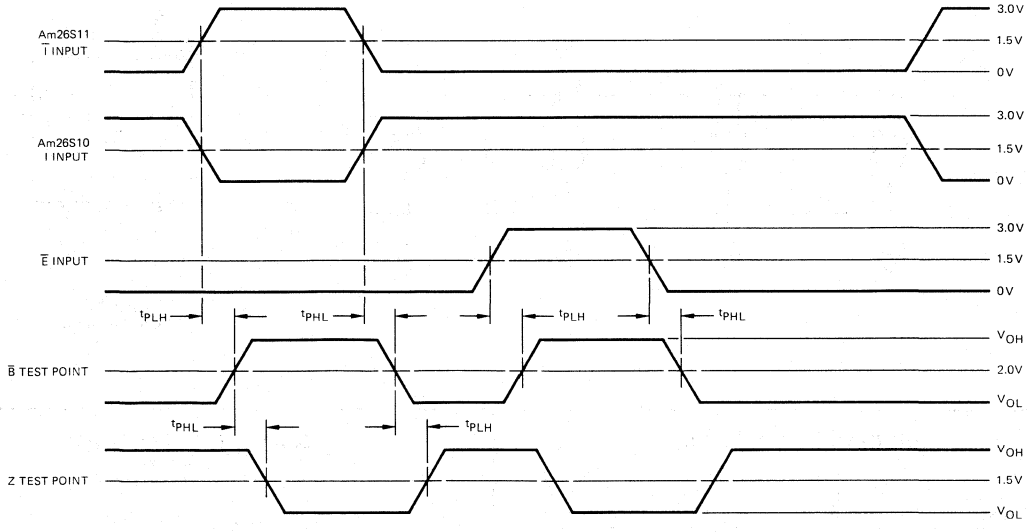
Note 1. Includes Probe and Jig Capacitance.

5

WAVEFORMS



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Am26S12•Am26S12A

Quad Bus Transceiver

Distinctive Characteristics

- Quad high-speed bus transceivers
- Driver outputs can sink 100mA at 0.7V typically
- 100% reliability assurance testing in compliance with MIL-STD-883
- Choice of receiver hysteresis characteristics

FUNCTIONAL DESCRIPTION

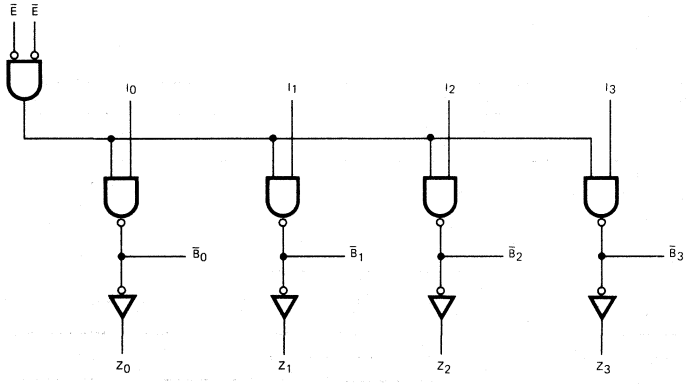
The Am26S12 • Am26S12A are high-speed quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.7 volts and four high-speed bus receivers. Each driver output is brought out and also connected internally to the high-speed bus receiver. The receiver has an input hysteresis characteristic and a TTL output capable of driving ten TTL Loads.

An active LOW, two-input AND gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable inputs can be conveniently driven by active LOW decoders such as the Am54S/74S139.

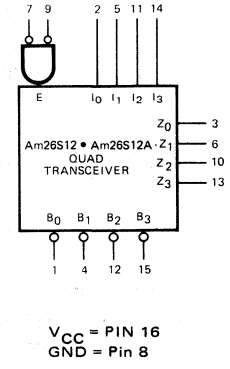
The high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The hysteresis characteristic of the Am26S12 receiver is chosen so that the receiver output switches to a HIGH logic level when the receiver input is at a HIGH logic level and moves to 1.4 volts typically, and switches to a LOW logic level when the receiver input is at a LOW logic level and moves to 2.0 volts typically. This hysteresis characteristic makes the receiver very insensitive to noise on the bus.

The Am26S12A is functionally identical to the Am26S12 but has a different hysteresis characteristic so that the output switches with the input being typically at 1.2 volts or 2.25 volts. In both devices the threshold margin, the difference between the switching points, is greater than 0.4 volts.

LOGIC DIAGRAM/SYMBOL



LIC-380



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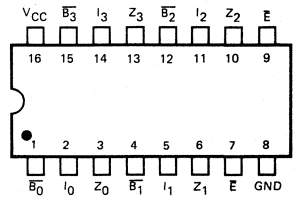
ORDERING INFORMATION

Package Type	Temperature Range	Am26S12 Order Number	Am26S12A Order Number
Molded DIP	0°C to +75°C	AM26S12PC	AM26S12APC
Hermetic DIP	0°C to +75°C	AM26S12DC	AM26S12ADC
Dice	0°C to +75°C	AM26S12XC	AM26S12AXC
Hermetic DIP	−55°C to +125°C	AM26S12DM	AM26S12ADM
Flat Pak	−55°C to +125°C	AM26S12FM	AM26S12AFM
Dice	−55°C to +125°C	AM26S12XM	AM26S12AXM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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AXIMUM RATINGS (Above which the useful life may be impaired)

rage Temperature	−65°C to +150°C
mperature (Ambient) Under Bias	−55°C to +125°C
ply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
Input Voltage	−0.5V to +5.5V
tput Current, Into Outputs (BUS)	200mA
tput Current, Into Outputs (Receiver)	30mA
Input Current	−30mA to +5.0mA

ECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

26S12XC-Am26S12AXC T_A = 0°C to +75°C V_{CC} = 5.0V ±5% (COM Range)
26S12XM-Am26S12AXM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL Range) Note 1

ameters	Description	Test Conditions	Min.	Typ. (Note 2)	Max.	Units
I_{CC}	Power Supply Current	V_{CC} = MAX.		46	70	mA
I_{BUS}	Bus Leakage Current	V_{CC} = MAX. or 0V; V_{BUS} = 4.0V; Driver in OFF State			100	μA

iver Characteristics

V_{OL} (Note 1)	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	COM'L	I_{OL} = 100mA		0.7	0.8	Volts
			MIL	I_{OL} = 60mA		0.55	0.7	Volts
				I_{OL} = 100mA		0.7	0.85	
V_{IH}	Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 5.5V					1.0	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_I = 2.4V				1.0	40	μA
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_I = 0.4V				−0.4	−1.6	mA

ceiver Characteristics

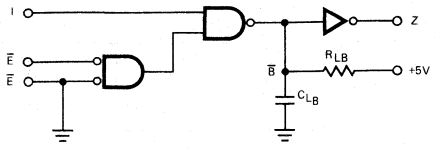
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800μA V_{IN} = V_{IL} (Receiver)		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IL} (Receiver)			0.4	0.5	Volts
V_{IH}	Input HIGH Level Threshold	$\overline{E}$ = H	Am26S12	1.8	2.0	2.2	Volts
			Am26S12A	2.05	2.25	2.45	
V_{IL}	Input LOW Level Threshold	$\overline{E}$ = H	Am26S12	1.2	1.4	1.6	Volts
			Am26S12A	1.0	1.2	1.4	
V_{TM}	Input Threshold Margin	$\overline{E}$ = H		0.4			Volts
OS	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−20		−55	mA

es: 1. For the Am26S12FM, Am26S12AFM the output current must be limited at 60mA or the maximum case temperature limited to 125°C for correct operation.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

itching Characteristics (T_A = 25°C, V_{CC} = 5.0V)

ameters	Description	Conditions	Min.	Typ.	Max.	Units
PLH	Turn Off Delay Input to Bus	C_{LB} = 15pF, R_{LB} = 100Ω		7	11	ns
PHL	Turn On Delay Input to Bus	C_{LB} = 300pF, R_{LB} = 50Ω		14	21	ns
PLH	Turn Off Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
PHL	Turn On Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
PLH	Turn Off Delay Bus to Output	C_L = 15pF		18	26	ns
PHL	Turn On Delay Bus to Output	C_L = 15pF		18	26	ns

SWITCHING CIRCUITS AND WAVEFORMS



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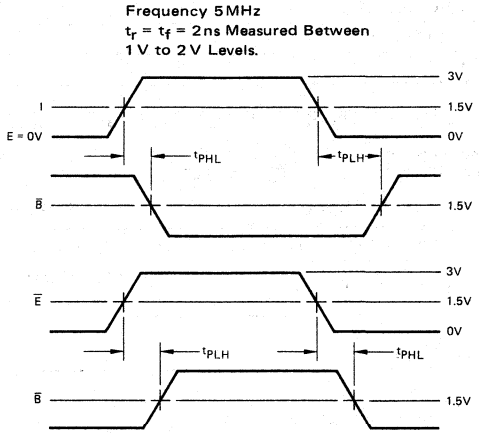
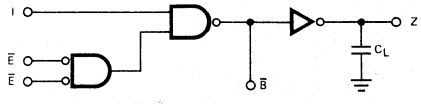


LIC-384

Figure 1. Bus Propagation Delays



LIC-385

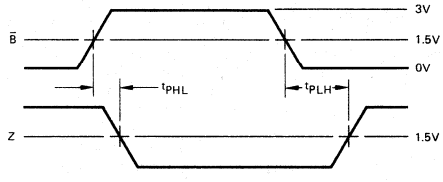


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Figure 2. Receiver Propagation Delays

TRUTH TABLE
Am26S12/26S12A

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table II

PERFORMANCE CURVES

Am26S12 Typical Receiver Input Characteristic

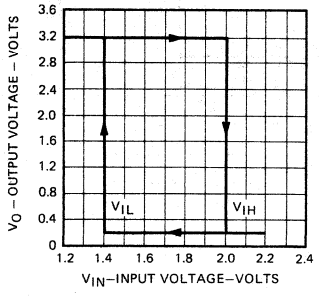

Figure 3

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Am26S12A Typical Receiver Input Characteristic

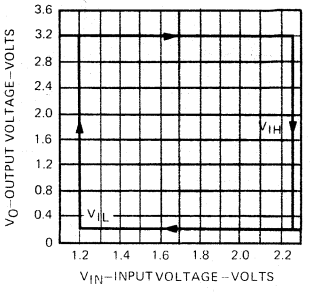

Figure 4

LIC-388

INPUT/OUTPUT CIRCUITRY

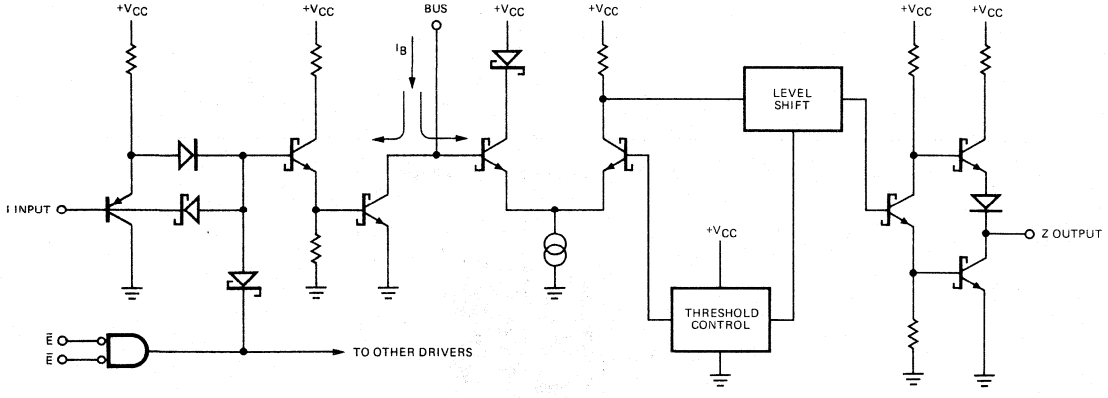

Figure 5

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Am26S12/26S12A APPLICATION

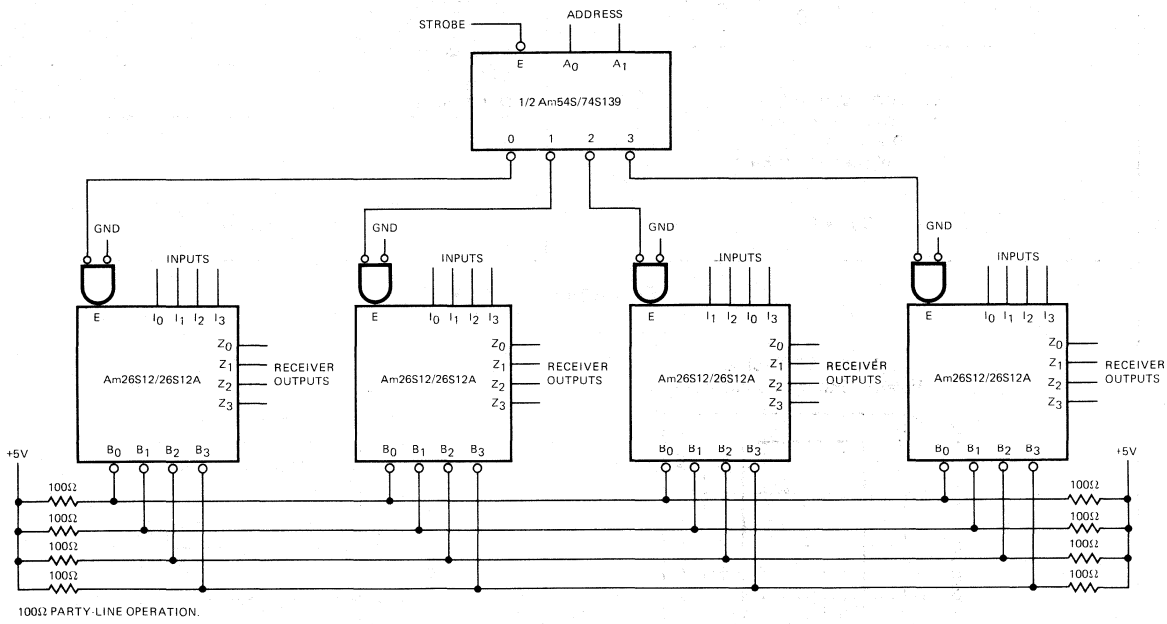

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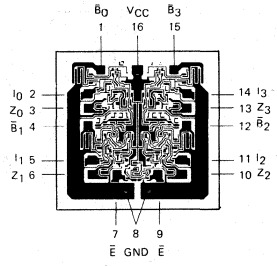
Figure 6

Metallization and Pad Layout



DIE SIZE: 0.071" x 0.072"

Am2900 Processor Family Index

Am2900 Components Continuously Become Faster and Faster Guidelines on Testing Am2900 Family Device

Design Aids

Am2900 COMPONENTS CONTINUOUSLY BECOME FASTER AND FASTER

MORE SPEED: NO MORE POWER

There's a good old tried and proven way to make faster IC's – burn more power. (That's the only real difference between "LS" and "S" devices). But that solution isn't satisfactory for LSI devices like the Am2900 family. Power is constrained to existing levels for reliability reasons.

Am2900 parts are always designed to obtain the maximum speed at a power level which is safe for the package types and operating environment of the part. To increase speeds, new technologies must be used to build faster components at no increase in power.

NEW CIRCUIT DESIGN TECHNIQUES MAKE FASTER GATES

One way to make faster components is to use new circuit design techniques. The most obvious is internal ECL, which provides very fast gates at similar power levels to LS TTL. Other design techniques, such as low-level logic (with very small logic swings on-chip), can also provide higher speeds without introducing the time penalty of ECL to TTL conversion.

Finally, very low power gates used in non-critical speed paths make more power available for use in critical speed paths. As the 2900 family develops, all these technologies will be used within a single component to achieve the highest speeds without increasing power. Among the first products to take advantage of mixed-circuit technology will be the Am2903A.

IMPROVED PROCESS CONTROL ALLOWS TIGHTER SPECS

Today's 2900 parts are carefully characterized over a wide range of voltages, temperatures, and process parameters before an AC specification is published. As manufacturing technology improves, the process is subject to smaller run-to-run variations, so that all of the product is closer to design nominal. This makes it possible to specify parameters more closely to typical without incurring large yield losses. The first product reflecting this is the Am2903.

WHAT'S GOOD FOR THE GOOSE IS GOOD FOR THE GANDER

Many new tools in production technology are emerging, primarily spurred by the emphasis on high-speed MOS memories. The same tools, such as projection masking, also provide for smaller geometries in bipolar circuits. As MOS gets faster, so does bipolar. The Am2901B obtains its speed improvement over the Am2901A through these tools.

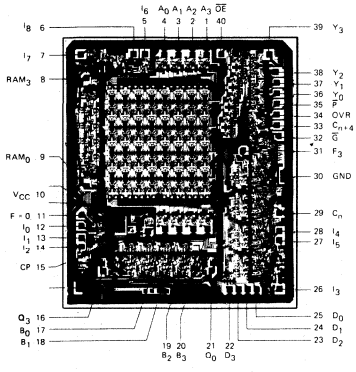
DESIGN FOR THE FUTURE

Every Am2900 part will undergo an evolution as new technologies become practical for production. Every part type will continuously become faster. Within a few short years, 2900-based designs will compete favorably with Schottky MSI on a speed basis at a fraction of the component count.

Most existing 2900 designs can be offered in higher performance versions simply by substitution of the 2901B for the 2901A, the 2909A for the 2909, the 2903A for the 2903, and so forth. Your 2900 design won't run out of speed in a few years. Advanced Micro Devices' 2900 Family will serve tomorrow's needs as well as today's.

SMALLER DIE SIZES MAKE FASTER PARTS

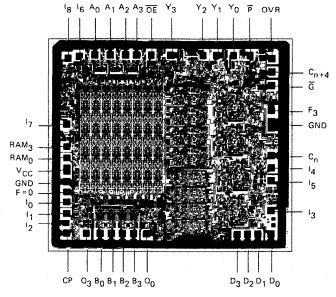
Am2901



DIE SIZE 0.167" X 0.198"

Speed A,B → $\overline{G}$,$\overline{P}$ 80ns

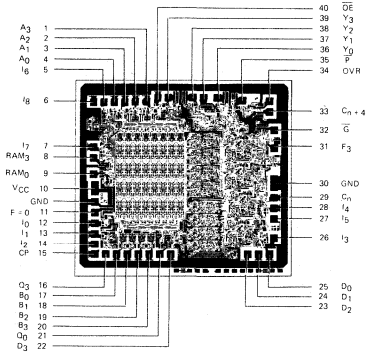
Am2901A



DIE SIZE 0.132" X 0.149"

Speed A,B → $\overline{G}$,$\overline{P}$ 65ns

Am2901B



DIE SIZE 0.117" X 0.128"

Speed A,B → $\overline{G}$,$\overline{P}$ 50ns

INTRODUCTION

THREE GENERATIONS OF TTL

Transistor-transistor logic has been the dominant technology for digital circuits since it was developed in the mid-1960's. It has proven itself to be manufacturable in high volume using an extremely reliable process technology. The processes used for TTL have evolved over the years, making components smaller, faster and less expensive. Relative to a TTL gate manufactured in 1966, a gate on a circuit manufactured today occupies 1/5 the area, consumes 1/10 the power, is twice as fast and costs less than 1/100 the price.

The circuits built using TTL technology have gone through two generations; the Am2900 Family represents the beginning of the third. Each generation consists of circuits which are fundamental building blocks of systems – circuits which can be interconnected in many different ways to build many different systems. Only by producing such universal circuits can manufacturing volumes be high enough to generate the rapid cost reductions characteristic of the integrated circuit industry.

The quality which distinguishes one generation from another is the level of integration used, and, because of the level of integration, the philosophy behind the circuit.

If one draws a curve plotting the cost of an individual gate against the number of gates on a chip, Figure 1 results.

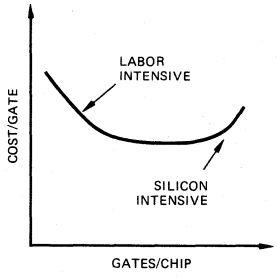


Figure 1. MPR-001

At the left, cost per gate is inversely proportional to the number of gates on the chip. The chip is small enough that it does not represent a significant portion of the cost of the product – it is virtually free. The cost of the product is composed of labor in assembly and test, the cost of processing an order, shipping and fixed overhead. Doubling the number of gates on the chip doesn't materially affect the cost so the cost per gate halves. As the number of gates per chip increases, the die begins to cost more, reversing the downward trend. As die cost dominates, the cost per gate remains relatively flat until the yield of the die begins to decline markedly. The cost per gate then begins to rise again. The lowest cost per gate is achieved at a level of integration corresponding to the flat region. This is the optimum level of integration.

As technology improves, costs are constantly reduced and the optimum level of integration occurs at more and more gates per chip.

The three curves of Figure 2 are the reason for the three generations of TTL. Each generation has consisted of fundamental system building blocks designed to take advantage of the optimum level of integration at the time.

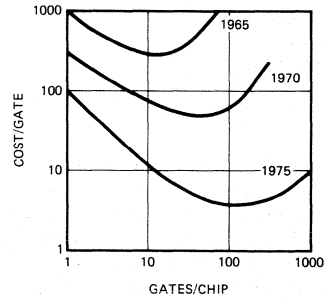


Figure 2. MPR-002

GENERATION I – SSI, 1965

In 1965, the optimum level of integration was three-to-six gates per chip. Users were delighted to buy such chips at $10-20 each. The circuits were useful in many systems. They consisted of gates – the 7400, 7410, 7420 – and, pressing the state of the art, some flip-flops. They were fundamental building blocks.

GENERATION II – MSI, 1970

Beginning around 1968, it became economical to put more gates on a chip and the industry was faced with a problem: How does one put 20 gates on a chip and build a universal building block? Clearly, one answer was to bring the inputs and outputs off chip as had been done before. But that was the wrong answer. The right answer was to redefine fundamental building blocks. The new building blocks fell into seven categories:

- Counters
- Decoders
- Multiplexers
- Operators (adders, comparators)
- Encoders
- Registers
- Latches

All systems could be defined in terms of these seven functions, and integrated circuits could be defined at the 20-50 gate/chip level which performed these functions efficiently. This, of course, is MSI. Over the last six or seven years, more and more circuits of this type have been introduced, utilizing standard gold-doped technology, low-power TTL, high-speed TTL, Schottky TTL, and now low-power Schottky TTL technology. Today, there are over 250 different MSI circuits and new ones appear every month. But in today's technology, many of these circuits are not particularly cost effective. They are too small for today's technology and their costs are labor intensive. (Labor costs do not follow traditional semiconductor pricing patterns.) In 1977, the optimum level of integration for bipolar logic is around 500 gates/chip.

GENERATION III – The Am2900 Family, 1976

At a 500-gate-per-chip level of integration, one does not build counters, decoders, and multiplexers. A new definition of fundamental system functions is needed. Advanced Micro Devices has defined these eight categories:

- Data Manipulation
- Microprogram Control
- Macroprogram Control
- Priority Interrupt
- Direct Memory Access
- I/O Control
- Memory Control
- Front Panel Control

The Am2900 Family consists of circuits designed to perform those functions efficiently. They are fundamental system building blocks; they contain hundreds of gates per chip; they are fast – utilizing Low-Power Schottky TTL technology; they are expandable; they are flexible – useful in emulation; and they are driven under microprogram control.

THE Am2900 FAMILY

The Am2900 Family consists of a series of LSI building blocks designed for use in microprogrammed computers and controllers. Each device is designed to be expandable and sufficiently flexible to be suitable for emulation of many existing machines. It is the wide variety of machine architectures possible with the Am2900 Family which sets it apart from the fixed-instruction microprocessors such as the Am9080A.

While an Am9080A can be used to build a microcomputer with only four or five packages, an Am2900 design will require 30 or 40 or more. The Am9080A design will, therefore, almost always be cheaper. But the Am9080A, or any other fixed-instruction processor, can execute only one instruction set, so it is not really suitable for emulation of another machine.

Moreover, a fixed-instruction processor operates only on words of a single length, usually eight bits. An Am2900 design, on the other hand, can be constructed for any word length which is a multiple of four bits.

Many applications require specialized operations to be performed at relatively high speed. Such functions as multiply and divide and special graphic control operations, can be done in microcode 10–100 times faster than in fixed-instruction MOS processors.

MICROPROGRAMMED ARCHITECTURE

Most small processors today are being designed using a technique called microprogramming. In microprogrammed systems, a large portion of the system's control is performed by a read only memory (usually PROM) rather than large arrays of gates and flip-flops. This technique frequently reduces the package count in the controller and provides a highly ordered structure in the controller, not present when random logic is used. Moreover, microprogramming makes changes in the machines' instruction set very simple to perform – reducing the post-production engineering costs for the system substantially.

The Am2900 Family of Bipolar LSI devices has been designed for use in microprogrammed systems. Each device performs a basic system function and is driven by a set of control lines from a microinstruction.

Figure 3 illustrates a typical system architecture. There are two "sides" to the system. At the left is the control circuitry and on the right is the data manipulation circuitry. The block labeled "2901 array" consists of the ALU, scratchpad registers, data steering logic (all internal to the Am2901's), plus left/right shift control and carry lookahead circuit. Data is processed by moving it from main memory (not shown) into the 2901 registers, performing the required operations on it and returning the result to main memory. Memory addresses may also be generated in the 2901's and sent out to the memory address register (MAR). The four status bits from the 2901's ALU are captured in the status register after each operation.

The logic on the left side is the control section of the computer. This is where the Am2909, 2910, or 2911 is used. The entire system is controlled by a memory, usually PROM, which contains long words called microinstructions. Each microinstruction contains bits to control each of the data manipulation elements in the system. There are, for example, nine bits for the 2901 instruction lines, eight bits for the A and B register addresses, two or three bits to control the shifting multiplexers at the ends of the 2901 array (Figure 19 or 2901 data sheet), and bits to control the register enables on the MAR, instruction register, and various bus transceivers. When the bits in a microinstruction are applied to all the data elements and everything is clocked, then one small operation (such as a data transfer or a register-to-register add) will occur.

A "machine instruction" (such as a minicomputer instruction or a 9080A instruction) is performed by executing several microinstructions in sequence. Each microinstruction therefore contains not only bits to control the data hardware, but also bits to define the location in PROM of the next microinstruction to be executed. The fields are labeled in Figure 3 as I, CC, and BA. The I field controls the sequencer. It indicates where the next address is located – the μPC, the stack, or the direct inputs – and whether the stack is to be pushed or popped.

The CC field contains bits indicating the conditions under which the I field applies. These are compared with the condition codes in the status register and may cause modification to the I field. The comparing and modification occurs in the block labeled "control logic". Frequently this is a PROM or PLA. In the case of the Am2910, it is built into the chip. The BA field is a branch address or the address of a subroutine.

PIPELINING

The address for the microinstructions is generated by the sequencer, starting from a clock edge. The address goes from the sequencer to the ROM and, an access time later, the microinstruction is at the ROM outputs.

A pipeline register is a register placed on the output of the microprogram memory to essentially split the system in two. The pipeline register contains the microinstruction currently being executed ①. (Refer to the circled numbers in Figure 3.) The data manipulation control bits go out to the system elements and a portion of the microinstruction is returned to the sequencer ② to determine the address of the next microinstruction to be executed. That address ③ is sent to the ROM and the next microinstruction ④ sits at the input of the pipeline register. So while the 2901's are executing one instruction, the next instruction is being fetched from ROM. Note that there is no sequential logic in the sequencer between the select lines and the output. This is important because the loop ① to ② to ③ to ④ must occur during a single clock cycle. During the same time, the loop from ① to ⑤ must occur in the 2901's. These two paths are roughly the same (around 200ns worst case for a 16-bit system). The presence of the pipeline register allows the microinstruction fetch to occur in parallel with the data operation rather than serially, allowing the clock frequency to be doubled.

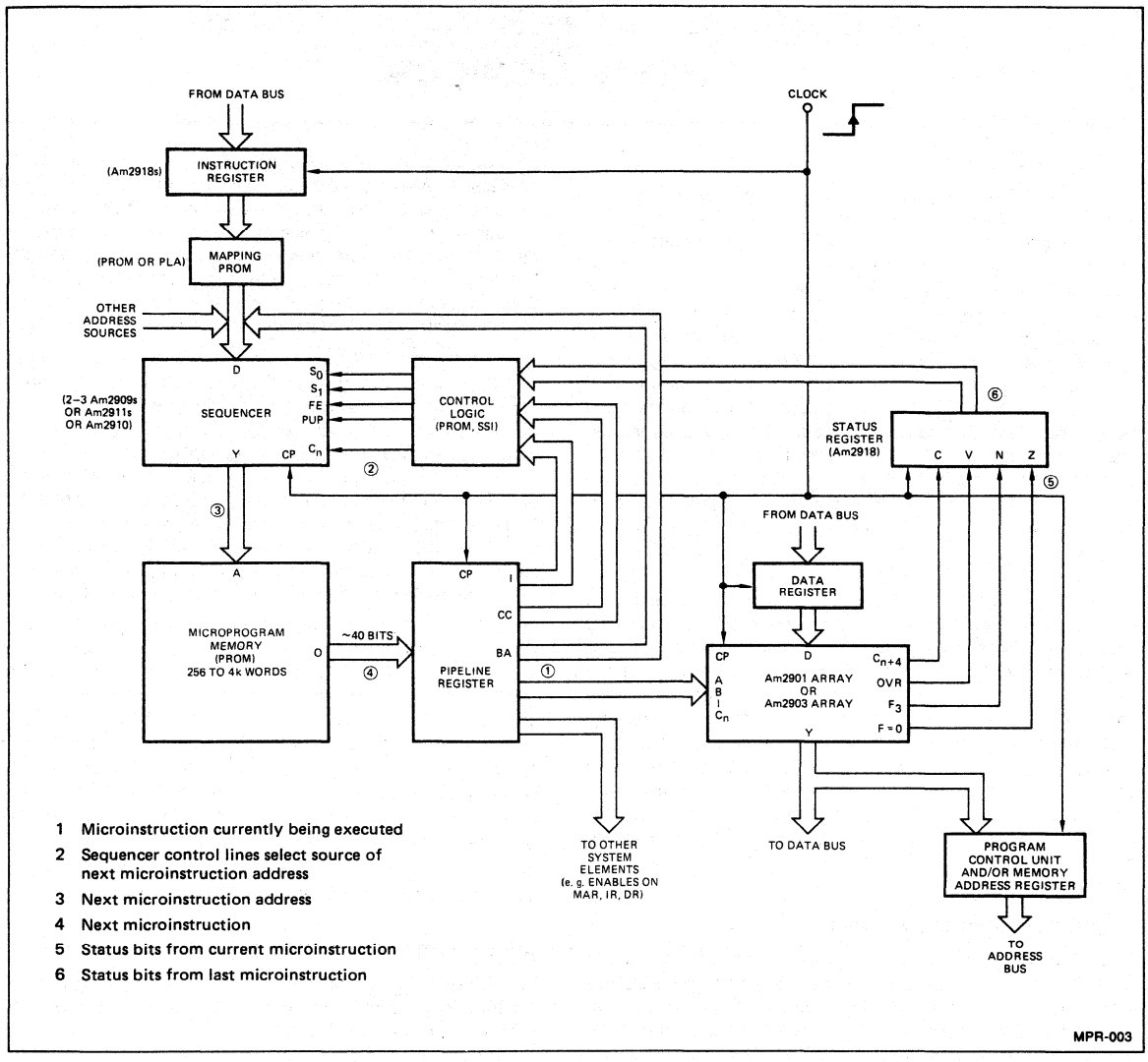


Figure 3.

The system shown in Figure 3 works as follows. A sequence of microinstructions in the PROM is executed to fetch an instruction from main memory. This requires that the program counter, often in a 2901 working register, be sent to the memory address register and incremented. The data returned from memory is loaded into the instruction register. The contents of the instruction register is passed through a PROM or PLA to generate the address of the first microinstruction which must be executed to perform the required function. A branch to this address occurs through the sequencer. Several microinstructions may be executed to fetch data from memory, perform ALU operations, test for overflow, and so forth. Then a branch will be made back to the instruction fetch cycle. At this point, there may be branches to other sections of microcode. For example, the machine might test for an interrupt here and obtain an interrupt service routine address from another mapping ROM rather than start on the next machine instruction. There are obviously many possibilities. Throughout this data book, in application notes, and within data sheets, some suggested techniques will be found.

Additional application notes are in preparation and are planned for publication. Advanced Micro Devices' Applications' staff is available to answer questions and provide technical assistance as well. They may be reached by calling (408) 732-2400, or, outside California (800) 538-8450. Ask for Am2900 Family Applications.

Guidelines on Testing Am2900 Family Devices

I. INTRODUCTION

The Am2900 Family represents a major step forward in bipolar technology, in that each device contains a number of MSI-type functions interconnected on one chip. The gate counts in the parts comprising the Am2900 Family are around 10 times the gate count of MSI functions. While this produces a number of advantages for manufacturing, such as reduced component count and lower costs, it complicates the incoming-inspection problem because test programs tend to be long and complex and must be carefully designed to insure that *all bad parts are rejected* and *most good parts are accepted.* While stating these two criteria is simple, reducing them to practice is not. LSI devices are not as "forgiving" of simplifications in test patterns and assumptions about forcing functions and noise levels, as their simpler counterparts. These notes are intended to point out some common areas of difficulty and their solutions.

II. THE PURPOSE OF TESTING

Testing is performed at most facilities during an inspection of purchased material. The reason, of course, is that it is much less expensive to screen parts then, than it is to troubleshoot and repair completed boards. Ideally, all the parts passed by incoming inspection will work in the system. This is insured through a specification which defines the way the part must behave in the system, and the incoming test should confirm that devices received meet the specification. The incoming test should not reject devices which meet the specification. When test programs are too tight or test for conditions not contained in the specification, delays in shipments occur and significant costs are incurred by both the vendor and the buyer trying to resolve "correlation problems."

III. GUARANTEEING THAT THE PARTS WORK

One step in testing devices is to perform DC parametric tests: I_{CC}, V_{OH}, V_{OL} and the like. These tests on bipolar LSI are not really different from those performed on simpler TTL devices, except that the number of pins involved is greater, and more complex set-ups may be required to put outputs in the proper state for testing. Another step is functional testing, and for bipolar LSI, function tests are significantly different than for MSI. The function tests must first insure that the device is capable of working, i.e., it's hooked up correctly inside. These kinds of tests can be described as "stuck-at-one, stuck-at-zero" tests, because they are designed to exercise each gate in the part. Even for a part as complex as the Am2901, the "stuck-at" tests can be performed quickly. Less than 400 test patterns must be applied to the part to exercise every gate.

But, "stuck-at" tests make an assumption: if a gate works, then it works regardless of the state of other gates in the circuit. Each gate is treated independently, but, in the integrated circuit, no gate is an island. The performance of one gate can, in fact, depend on the states of surrounding gates, because they share common inputs or common ground lines.

These possible faults are often not tested by "stuck-at" tests, because they are not independent of the state of surrounding logic. These potential faults depend on the physical and logical construction of the circuit. They are usually called "pattern sensitivities." Pattern-sensitive faults, like the two described above, are not something new. All digital products exhibit pattern sensitivities – even SSI. But, on simpler parts, either traditional "stuck-at" tests happen to find most of them, or the parts are easy enough to test that all possible data patterns are generated during testing. Neither of these circumstances is true for bipolar LSI. A special effort must be made to apply many data patterns to the devices to check for pattern-sensitive faults. This has been done for years with RAM patterns such as GALPAT. It must now be done with logic functions as well.

In the devices in the Am2900 Family, as with RAMs, testing all possible data patterns is not practical, but, the various MSI kinds of functions in the devices (register, ALU, multiplexer, etc.) can generally be logically isolated, and each of those functions should be checked independently for all possible data patterns. This principle works because (1) as a rule, it is possible to control the MSI functions in a 2900 part with some degree of independence, and (2) the MSI functions are usually physically separated on the die, so that a data pattern within one MSI block will not exhibit pattern sensitivity dependent on the data in another MSI block.

In the Am2901, for example, ALU tests using the two RAM ports as data sources are unlikely to be affected by the state of the data inputs or the Q register. The shift multiplexer at the input of the RAM is unlikely to be affected by the Q register or the ALU source-select multiplexers. The control logic for the ALU source multiplexers should not be affected by anything in the ALU. By applying these kinds of principles intelligently, function tests can be constrained to a few thousand tests which provide a very high confidence level that the part is not subject to pattern-sensitive faults within its operating range.

As an example of the test philosophy used on these parts, the function tests for the Am2901 are described below.

Am2901 FUNCTION TEST DESCRIPTION

The following describes the function tests performed on the Am2901. The $\overline{OE}$ pin is low during the entire function tests and each test gets one clock pulse.

A-Port Galpat via ALU

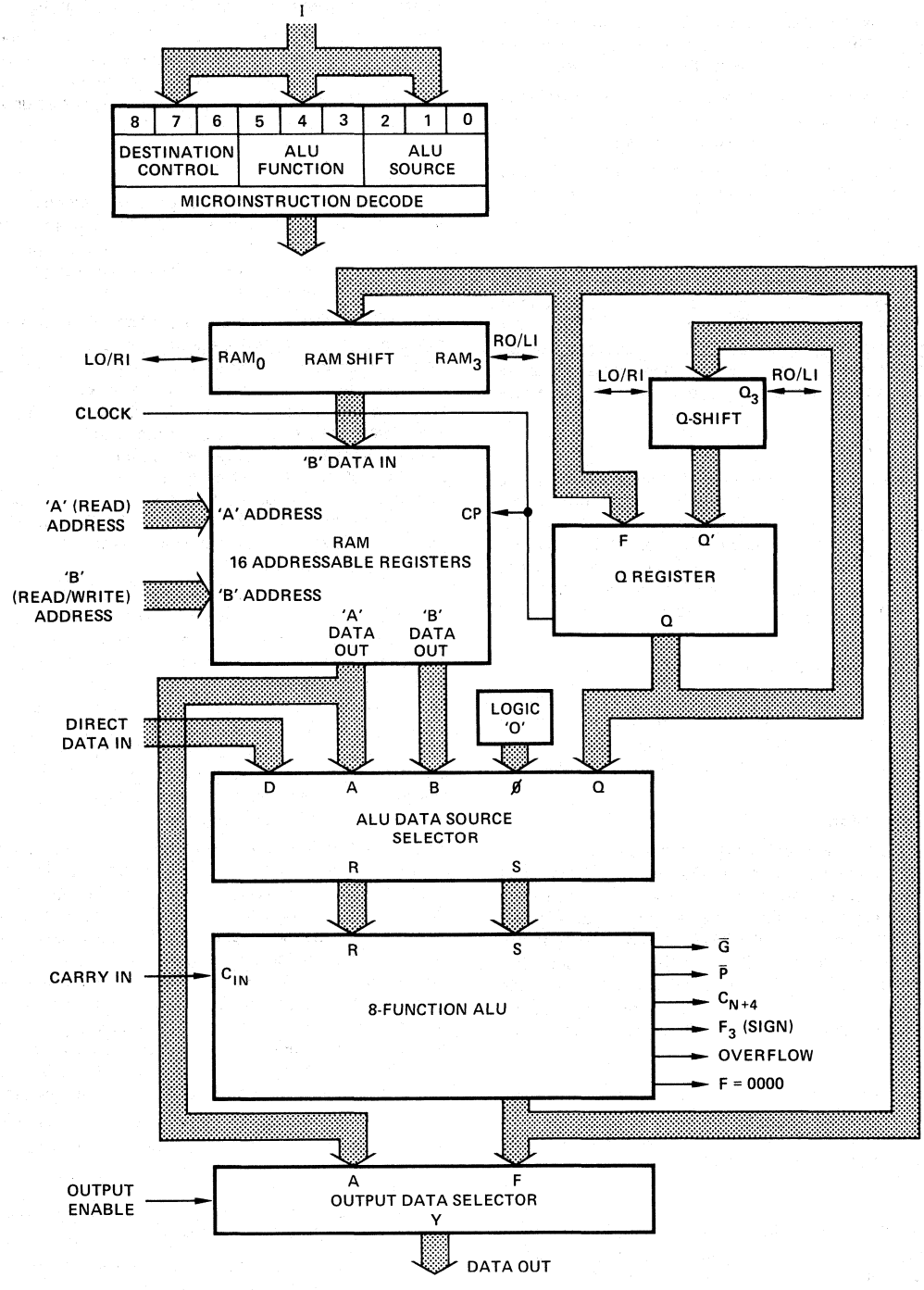
These are tests in which the A-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the B-address is the same as the A-address and OP code 337 is used for a write operation, while OP code 134 is used for a write operation, while OP code 134 is used for a read operation. The four shift-operation pins, Q_0, Q_3, RAM_0 and RAM_3, are ignored.

B-Port Galpat via ALU

These are tests in which the B-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the A-address is the inverse of the B-address and OP code 337 is used for a write operation while OP code 133 is used for a read operation. The four shift-operation pins, Q_0, Q_3, RAM_0 and RAM_3, are ignored.

A-Port Galpat Bypass ALU

These are tests in which the A-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the B-address is the inverse of the A-address and OP code



THE Am2901 4-BIT MICROPROCESSOR SLICE

337 is used for a write operation while OP code 233 is used for a read operation. The four shift-operation pins, Q_0, Q_3, RAM_0 and RAM_3, are ignored.

Repeat 1 above by inverting the Data and Y output information on D_{3-0} and Y_{3-0}. All other outputs are ignored. This performs Galloping "zeros" in a field of "ones" for the A-Port via ALU.

Repeat Item 2 above by inverting the Data and Y output information on D_{3-0} and Y_{3-0}. All other outputs are ignored. This performs Galloping "zeros" in a field of "ones" for the A-Port via ALU.

Repeat Item 3 above by inverting Data and Y output information on D_{3-0} and Y_{3-0}. All the other outputs are ignored. This is Galloping "zeros" in a field of "ones" for A-Port bypass ALU.

ALU Source Code

During these tests, the A and B-addresses are at word locations preloaded with known values. The Q register is also preloaded. Then, with the ALU destination OP code = 1 (No-OP) and the ALU function code = 6 (exclusive OR), the source code is cycled through from 0-7. The function code is then modified to 7 (exclusive NOR) and the source code sequence is cycled through once more.

ALU Function Code

During these tests, the memory is preloaded with content equal to the address. In other words, word 0 is loaded with 0, word 1 with 1, and so on. Then, with A-address = B-address, a destination OP code of 1 (No OP), and a source OP code of 1 (A&B Port selected), the ALU function code is cycled through the sequence of 7, 5, 4, 0, 1, 3, 2, 6 for every set of A&B address. This whole sequence is then repeated with A-address equal to the inverse of the B-address.

Arithmetic Operation & Carry Generation

During these tests, the memory is preloaded with content address. With OP code 105, whereby D input is added to the A-Port of the memory, the tester cycles through every possible D input added to every word in memory with carry in being both one and zero.

Q Register Operation

During these tests, the Q register is first loaded with all zeros. Then, with Cn = 0 and with OP code 006, whereby Q register is loaded with the sum of data input and Q-register content on every clock cycle, the device is clocked through all possible data inputs. The Cn input is then changed to a ONE, and with OP code 016 whereby Q register is loaded with the difference of Q-D. The device is clocked through all possible data input again. This checks both the add and subtract modes of the ALU, the internal-carry-lookahead circuitry and the Q-register operation.

Q Register Shifting

During these tests, a unique string of data (11100001 010011011110) is shifted into the appropriate shift inputs. OP codes used in this group of tests are 432 for shift left, 532 for no shift, 632 for shift right and 732 for no shift.

RAM Shifting

During these tests, A and B-address are at word 0. A string of data (11100001010011011110) is shifted into the appropriate shift inputs. OP codes used are 434 and 533 for left shift, 634 and 733 for right shift.

IV. AVOIDING THE REJECTION OF GOOD DEVICES

Discrepancies in testing results between the vendor and the buyer result in much irritation and substantial costs for both. Some of the common sources of these discrepancies are discussed below.

Testing for Unspecified or "don't care" Conditions

The data sheet (or purchase specification) defines the characteristics of the part. It is hard enough to test for everything specified without adding additional tests for unspecified parameters. If the state of an output is not specified under certain conditions, then it should not be tested.

Noise

Many testing problems result from noise produced by the interactions of the device being tested and the test system. Typical test fixtures have lead interactives several times that of a PC board socket. This inductance, especially in the device ground path, is the source of these problems.

When the inputs to the device are changed there is a sequence of rapid changes in the devices ground currently as signals propagate through internal gates to the outputs. These appear as changes in the voltage drop across the device ground lead. This voltage drop can be as much as 2 volts across a few inches of wire. Rise times are on the order of 1nsec and pulse widths range from 2 to 10nsec. Output tranisient current during switching may be 50 to 100mA. The test systems input and output reference voltages are set with respect to tester ground and are not effected by these transients. Consequently the effective input voltages to the device will vary. If the ground pin goes up 1 volt, all the inputs effectively go down 1 volt.

This must be considered in selecting levels for V_{IL} and V_{IH}. The device data sheet says V_{IL} must be less than 0.8V and V_{IH} more than 2.0V. But this is as measured at the device package pins, between input and ground. This means that if the ground varies $\pm$0.5 volt the input levels must be $V_{IL} \leq 0.3V$ and $V_{IH} \leq 2.5V$. If this is not done, a noise pulse could, for example, make the clock input effectively go high in the middle of the clock low time, causing an extra clock pulse. A similar situation exists at the device outputs, requiring V_{OL} to be set higher, and V_{OH} lower, than the data sheet numbers. AMD uses $V_{IL} = OV$, $V_{IH} = 3V$, $V_{OL} = 1V$, $V_{OH} = 2V$ for functional tests.

Proper observations are important to the understanding and control of these problems. Small changes in timing, bypass capacitors, etc will have large effects on the noise. An oscilloscope of 200 MHz or greater bandwidth is essential. Noise voltage should be measured at the device ground pin (at the device package edge, not the bottom of the test socket). Connect the probe ground to the tester chassis. In order to see the peak noise voltage, cycle the tester through a long pattern. Trigger the scope internally from the noise waveform. Turn the trigger level slowly up until the trace is almost lost. The peak noise voltage will appear at the left side of the screen. Sweep speed should be about 10nsec/div. Repeat for the peak of the opposite polarity.

Another useful technique is to identify a particular test pattern location which causes significant noise. Sync the oscilloscope to this test cycle. Using a two channel scope, connect one channel to an input pin and the other channel to the device ground pin. Invert the channel on the ground pin and add the two channels. The waveform will show the effective input levels.

An additional problem is introduced by I/O pins. When output load circuits are connected to these pins the tester must drive the load and the device when the pins are inputs. If the tester has a driver impedance of 50ohms and the load supplies 16mA into V_{OL}, the input level produced will be 0.8V too high. This must be compensated by further reducing the programmed V_{IL} for only the I/O pins. Some devices are sensitive to input voltages below ground.

If the tester does not provide suitable alternate driver supplies, it may be necessary to provide resistor pullups for input-only pins.

The same ground lead inductance problems causes difficulties in DC testing. Many DC tests require some functional sequence to produce the correct device state. The input levels must be such to avoid false clocks, etc. DC tests may be used to verify input threshold levels. To do this, an output test such as V_{OL} or V_{OH} is selected where the outputs combinatorally depend on the inputs. Using non-threshold levels the appropriate input conditions are applied. The input levels are then reprogrammed to threshold levels. The outputs are then measured for V_{OL} or V_{OH}. It is not possible to do the functional set-up with threshold levels, even if it is only a single line, as oscillations may occur. Switching between alternate driven supplies also may generate sufficient noise to cause problems.

AC Testing

Many modern testers allow switching tests to be performed during the application of complex test sequences. The switching and function tests can then occur together. Unfortunately, this blurs the distinction between functional failure and switching-speed failure when a device is rejected, so, it is a good idea to do some preliminary function testing with "loose" AC limits before trying to do everything at once. When function and AC testing are combined, it is important to consider the *driving conditions* under which the AC parameters are tested. Switching measurements on Bipolar ICs are usually made with input levels switching between 0V and 3.0V (sometimes 0.4V and 2.4V are used). The output transition is measured at 1.5V (sometimes at 1.3V).

They are never specified at threshold levels (0.8V and 2.0V) because of noise problems.

Realistic AC tests require sequencing through many lines of test pattern to include a variety of data paterns. Unfortunately the AC accuracy of most modern logic testers is not as good as memory testers. There are often significant differences between different waveform formats. The position of an edge may depend on whether adjacent pins are switching and whether they are going up or down. This limits the accuracy of testing, especially for such parameters as hold times, where tester error usually exceeds the difference between device typical and data sheet maximum. This may be observed on an oscilloscope by cycling the tester and synchronizing the scope to a repetitive pulse, such as the device clock pin.* Do not trigger the scope on any particular tester cycle. Observing a device input on the second scope channel will show many overlapping transitions, positive and negative. The width of this band must be added to other error sources to determine tester accuracy.

*Use a sweep speed of 1nsec/div.

Temperature Testing

Integrated circuits are specified to operate over either the commercial range of 0° to +70°C or the military range of −55°C to +125°C. Standard screening procedures (from MIL-STD-883) call for 100% testing at 25°C followed by sample testing at the high and low temperature. Many users duplicate this test sequence in their incoming inspection, and some test 100% at temperature.

Testing problems are rarely encountered at low temperatures, if care is taken to prevent ice formation on the test socket. At high temperature, difficulties may arise because of the difficulty in creating a test environment which is representative of the thermal conditions found in the system.

High temperature testing with a controlled ambient temperature is very difficult because the thermal coefficient between the package and the surrounding environment depends on humidity, rate of air flow, package color, connections to package pins, and position of surrounding devices. For testing purposes, only the case temperature can really be controlled. (Most systems' thermal engineering is also designed to control case temperatures.)

V. INCOMING INSPECTION AND TESTING SUPPORT PRODUCTS

AMD provides several products to assist in the development of incoming inspection testing for most Am2900 LSI devices (Am2901B, Am2903, Am2904, Am2909, Am2910, Am2911, Am2914, Am2930, Am2932, Am2940, Am2942, Am2950, Am2951, Am2960, Am29705).

Sentry Test Programs

These are complete data sheet function, DC and AC parameter programs. They run on a Fairchild Sentry VII with low voltage test heads, 4K local memory and SPM. Complete load board documentation is included. Programs are supplied on magnetic tape in TDX format. Source files in ASCII code on magnetic tape can be provided for those who wish to generate test programs for other testers. Test programs require a licensing agreement.

Functional and AC Test Patterns

These are supplied on magnetic tape in ASCII code. They are the source files for the Sentry patterns. Waveform drawings for each test setup are included. Test patterns require a licensing agreement.

Basic Test Specification

This is a description of the test conditions for all DC parametric tests and also contains a list of all AC tests performed with limits. Basic Test Specifications require a licensing agreement.

Correlation Kit

This consists of two devices and datalog from AMD's characterization program.

ORDERING INFORMATION

Order Code	Description
AM29XX – SEN	Sentry Test Program
AM29XX – PAT	Functional & AC Test Patterns
AM29XX – BAS	Basic Test Specification
AM29XX – KIT	Correlation Kit

Am2901 • Am2901A • Am2901B

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- Two-address architecture –
  Independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU –
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection –
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU –
  Add and shift operations take only one cycle.
- Four status flags –
  Carry, overflow, zero, and negative.
- Expandable –
  Connect any number of Am2901's together for longer word lengths.
- Microprogrammable –
  Three groups of three bits each for source operand, ALU function, and destination control.
- Fast –
  Am2901B is up to 27% faster than Am2901A, up to 50% faster than Am2901. The Am2901B meets or exceeds all of the specifications for the Am2901 and Am2901A.

TABLE OF CONTENTS

For applications information see the last part of this data sheet and chapters III and IV of **Bit Slice Microprocessor Design,** Mick & Brick, McGraw Hill Publications.

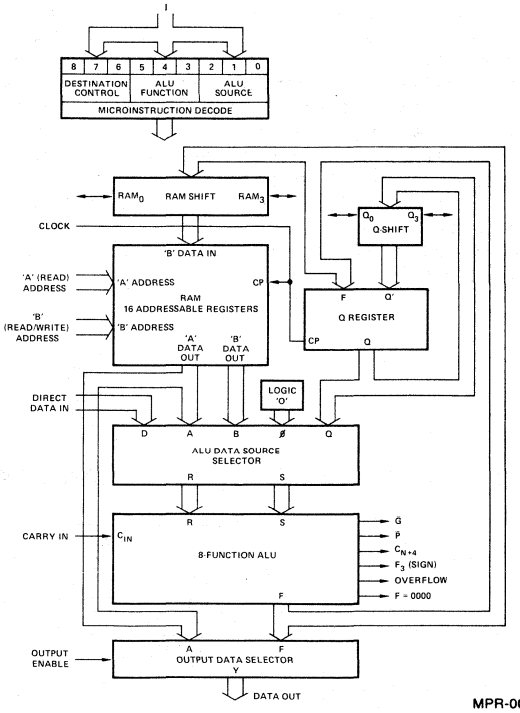
GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901 will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

The Am2901B is a plug-in replacement for the Am2901 or Am2901A, but is 25% faster than the Am2901A and 50% faster than the Am2901.

MICROPROCESSOR SLICE BLOCK DIAGRAM



MPR-004

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 4.

The clock input to the Am2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

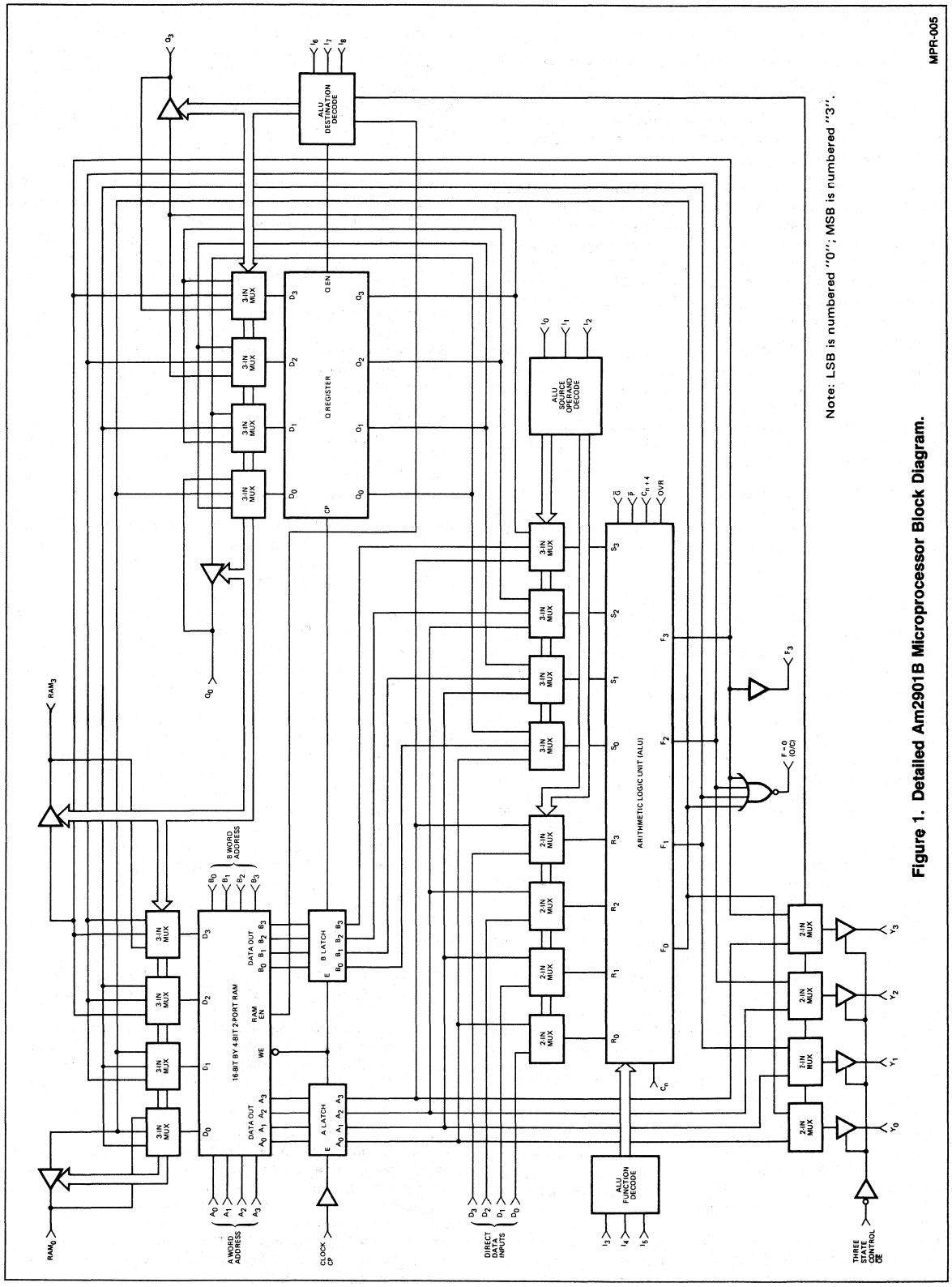


Figure 1. Detailed Am2901B Microprocessor Block Diagram.

Mnemonic	MICRO CODE I_2	I_1	I_0	Octal Code	ALU SOURCE OPERANDS R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Figure 2. ALU Source Operand Control.

Mnemonic	MICRO CODE I_5	I_4	I_3	Octal Code	ALU Function	SYMBOL
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	R ∀ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

Mnemonic	MICRO CODE I_8	I_7	I_6	Octal Code	RAM FUNCTION Shift	Load	Q-REG. FUNCTION Shift	Load	Y OUTPUT	RAM SHIFTER RAM_0	RAM_3	Q SHIFTER Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control.

OCTAL I_{210} OCTAL / I_{543} ALU Source / ALU Function	0 A, Q	1 A, B	2 O, Q	3 O, B	4 O, A	5 D, A	6 D, Q	7 D, O
0	C_n = L R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R AND S	A∧Q	A∧B	0	0	0	D∧A	D∧Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	A∀Q	A∀B	Q	B	A	D∀A	D∀Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

Figure 5. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 5 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the Am2901 can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A∧Q
4 1		A∧B
4 5		D∧A
4 6		D∧Q
3 0	OR	A∨Q
3 1		A∨B
3 5		D∨A
3 6		D∨Q
6 0	EX-OR	A∀Q
6 1		A∀B
6 5		D∀A
6 6		D∀Q
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$∧Q
5 1		$\overline{A}$∧B
5 5		$\overline{D}$∧A
5 6		$\overline{D}$∧Q

Figure 6. ALU Logic Mode Functions.

Octal	C_n = 0 (Low)		C_n = 1 (High)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q–1	PASS	Q
1 3		B–1		B
1 4		A–1		A
2 7		D–1		D
2 2	1's Comp.	–Q–1	2's Comp. (Negate)	–Q
2 3		–B–1		–B
2 4		–A–1		–A
1 7		–D–1		–D
1 0	Subtract (1's Comp)	Q–A–1	Subtract (2's Comp)	Q–A
1 1		B–A–1		B–A
1 5		A–D–1		A–D
1 6		Q–D–1		Q–D
2 0		A–Q–1		A–Q
2 1		A–B–1		A–B
2 5		D–A–1		D–A
2 6		D–Q–1		D–Q

Figure 7. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R} \wedge S$	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1} + P_3P_2P_1P_0 (G_0 + \overline{C_n})$	See note

Note: $[\overline{P}_2+\overline{G}_2\overline{P}_1+\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3+\overline{G}_3\overline{P}_2+\overline{G}_3\overline{G}_2\overline{P}_1+\overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Figure 8.

ORDERING INFORMATION

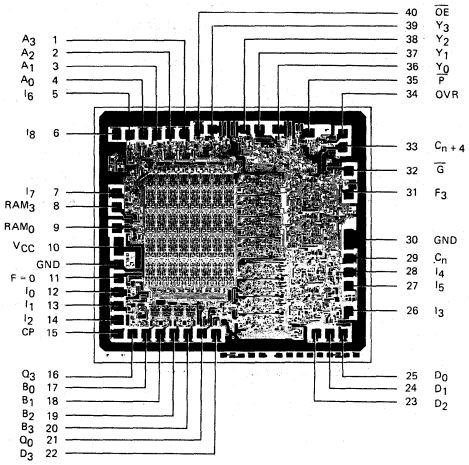
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2901 Order Number	Am2901A Order Number	Am2901B Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2901PC	AM2901APC	AM2901BPC	P-40	C	C-1
AM2901DC	AM2901ADC	AM2901BDC	D-40	C	C-1
AM2901DC-B	AM2901ADC-B	AM2901BDC-B	D-40	C	B-2 (Note 4)
	AM2901ADM	AM2901BDM	D-40	M	C-3
	AM2901ADM-B	AM2901BDM-B	D-40	M	B-3
	AM2901AFM	AM2901BFM	F-42	M	C-3
	AM2901AFM-B	AM2901BFM-B	F-42	M	B-3
	AM2901AXC	AM2901BXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
	AM2901AXM	AM2901BXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Figure 9.

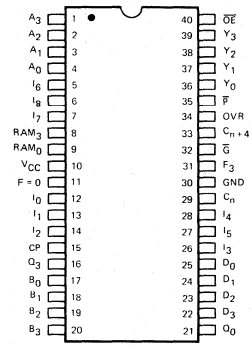
METALLIZATION AND PAD LAYOUT



Am2901B
DIE SIZE 0.117" X 0.128"

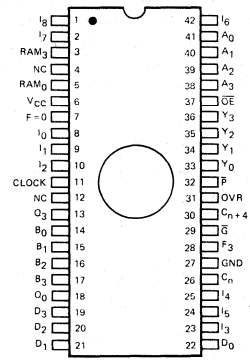
CONNECTION DIAGRAM
Top View

DIP



MPR-006

FLAT PACK CONNECTIONS
Top View



MPR-007

Note: Pin 1 is marked for orientation.

Figure 10.

PIN DEFINITIONS

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.

Y_{0-3} The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{G}$, $\overline{P}$ The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902 for carry-lookahead.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

F_3 The most significant ALU output bit.

C_n The carry-in to the internal ALU.

C_{n+4} The carry-out of the internal ALU.

CP The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

Part Number Suffix	V_{CC}	Temperature
PC, PCB, DC, DCB XC	4.75V to 5.25V	T_A = 0°C to +70°C
DM, DMB FM, FMB XM	4.50V to 5.50V	T_C = −55°C to +125°C

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq$ 0.4V and $V_{IH} \geq$ 2.4V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4			
				I_{OH} = −800μA, OVR, $\overline{P}$	2.4			
				I_{OH} = −600μA, F_3	2.4			
				I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4			
				I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
			C_{n+4}	I_{OL} = 10mA			0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		Clock, $\overline{OE}$			−0.36	mA
				A_0, A_1, A_2, A_3			−0.36	
				B_0, B_1, B_2, B_3			−0.36	
				D_0, D_1, D_2, D_3			−0.72	
				I_0, I_1, I_2, I_6, I_8			−0.36	
				I_3, I_4, I_5, I_7			−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
				C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Clock, $\overline{OE}$			20	μA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
				D_0, D_1, D_2, D_3			40	
				I_0, I_1, I_2, I_6, I_8			20	
				I_3, I_4, I_5, I_7			40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
				C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	Y_0, Y_1, Y_2, Y_3	V_O = 2.4V			50	μA
				V_O = 0.5V			−50	
			$RAM_{0,3}$ $Q_{0,3}$	V_O = 2.4V (Note 4)			100	
				V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				OVR, $\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}$, $Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX.	COM'L and MIL	T_A = 25°C		160	250	mA
			COM'L Only	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			MIL Only	T_C = −55°C to +125°C			280	
				T_C = +125°C			198	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
5. "MIL" = Am2901XM, DM, FM. "COM'L" = Am2901XC, PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

I. Am2901B Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2901B over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BDM
Am2901BFM

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.	88ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	15MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	88ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	82	84	80	70	90	86	94	–
D	44	38	40	34	50	45	48	–
Cn	34	32	24	–	38	31	39	–
I012	53	50	47	46	65	55	58	–
I345	58	58	58	48	64	56	55	–
I678	29	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	50	–	–	–	–	–	–	–
Clock ↓	53	50	49	41	63	58	61	31

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	30	0 (Note 3)	88 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	–	–	55	0
Cn	–	–	42	0
I012	–	–	58	0
I345	–	–	62	0
I678	14	Do Not Change		0
RAM0, 3, Q0, 3	–	–	18	3

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	40	25

Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

I. Am2901B Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2901B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BPC
Am2901BDC

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	69ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	16MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	69ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	60	61	59	50	70	67	71	–
D	38	36	40	33	48	44	45	–
Cn	30	29	20	–	37	29	38	–
I012	50	47	45	45	56	53	57	–
I345	51	52	52	45	60	49	53	–
I678	28	–	–	–	–	–	35	35
A Bypass ALU (I = 2XX)	37	–	–	–	–	–	–	–
Clock ↓	49	48	47	37	58	55	59	29

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	69 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	–	–	51	0
Cn	–	–	39	0
I012	–	–	56	0
I345	–	–	55	0
I678	11	Do Not Change		0
RAM0, 3, Q0, 3	–	–	16	0

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	35	25

Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

III. Am2901A Guaranteed Commercial Range Performance

The Am2901B meets or exceeds all of the specifications for the earlier Am2901A. Parts may still be ordered and marked as Am2901A.

IV. Am2901A Guaranteed Military Range Performance

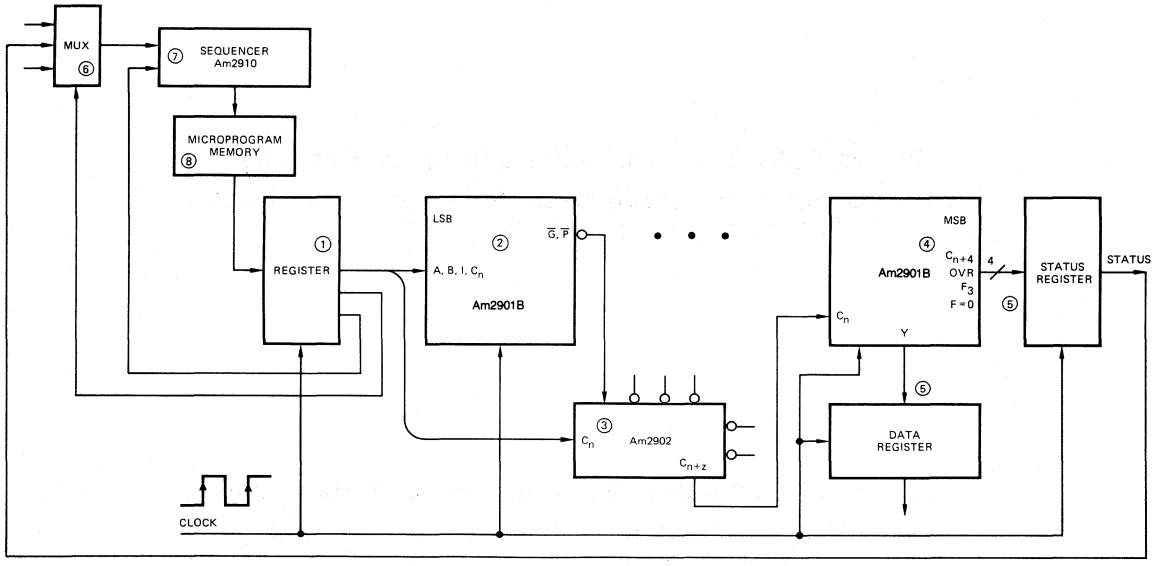
The Am2901B meets or exceeds all of the specifications for the earlier Am2901A. Parts may still be ordered and marked as Am2901A.

V. Am2901 Guaranteed Commercial Range Performance

The Am2901B meets or exceeds all of the specifications of the Am2901. Parts may still be ordered and marked as Am2901.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than Am2901B are representative for available MSI parts.



MPR-010

Pipelined System. Add without Simultaneous Shift.

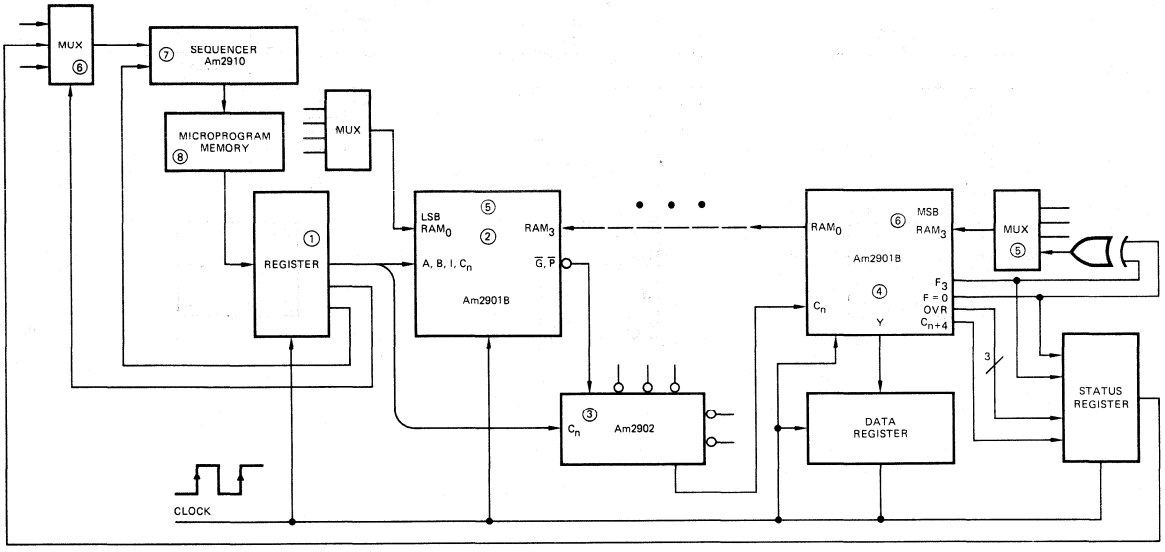
DATA LOOP			CONTROL LOOP		
① Register	Clock to Output	15	① Register	Clock to Output	15
+ ② 2901B	A, B to $\overline{G}$, $\overline{P}$	50	+ ⑥ MUX	Select to Output	20
+ ③ 2902	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	10	+ ⑦ 2910	CC to Output	45
+ ④ 2901B	C_n to C_{n+4}, OVR, F_3, F = 0, Y	37	+ ⑧ PROM	Access Time	55
+ ⑤ Register	Set-up Time	5	+ ① Register	Set-up Time	5
		117ns			140ns

Minimum clock period = 140ns

Figure 12.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS (Cont.)

Speeds used in calculations for parts other than Am2901B are representative for available MSI parts.



MPR-011

Pipelined System. Simultaneous Add and Shift Down.

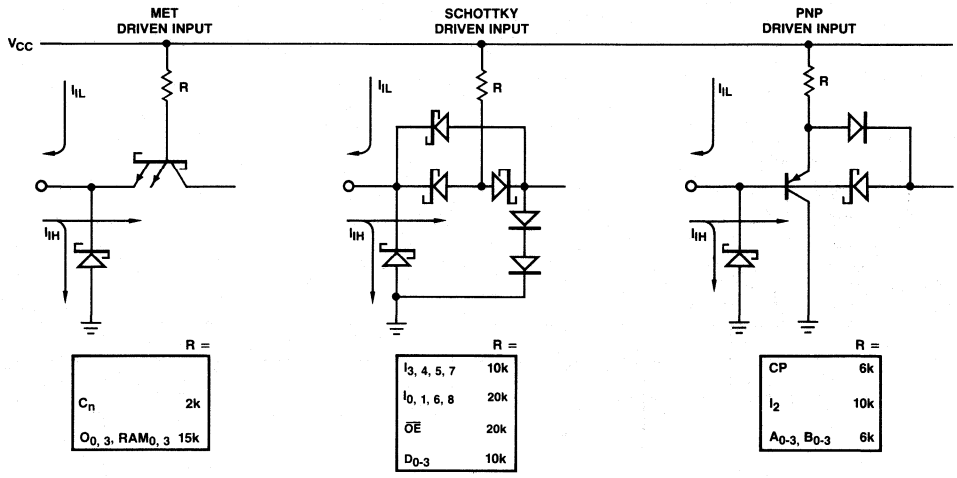
DATA LOOP		
① Register	Clock to Output	15
+ ② 2901B	A, B to $\overline{G}$, $\overline{P}$	50
+ ③ 2902	$\overline{G}_0\overline{P}_0$ to C_{n+z}	10
+ ④ 2901B	C_n to F_3, OVR	29
+ ⑤ XOR and MUX		21
+ ⑥ 2901B	RAM_3 Set-up	16
		141ns

CONTROL LOOP		
① Register	Clock to Output	15
+ ⑥ MUX	Select to Output	20
+ ⑦ 2910	CC to Output	45
+ ⑧ PROM	Access Time	55
+ ① Register	Set-up Time	5
		140ns

Minimum clock period = 141ns

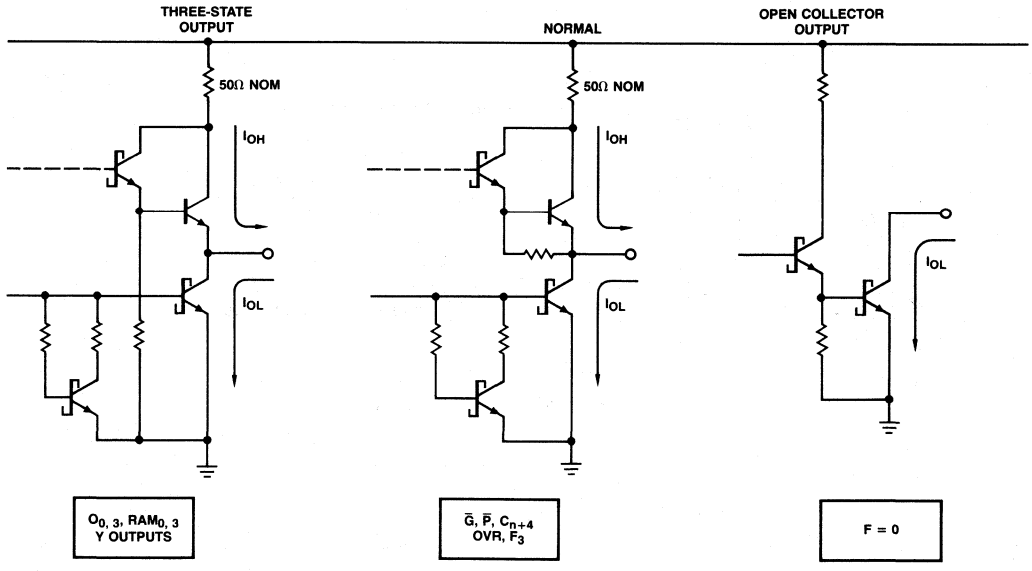
Figure 12 (Cont).

TTL INPUT/OUTPUT CURRENT INTERFACES



MPR-013

$C_I \approx 5.0pF$, all inputs



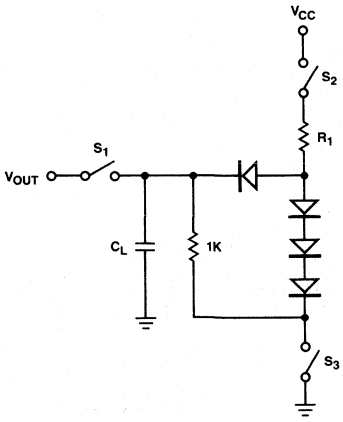
MPR-014

$C_O \approx 5.0pF$, all outputs

Figure 13.

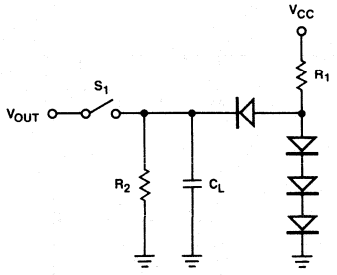
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2901B

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

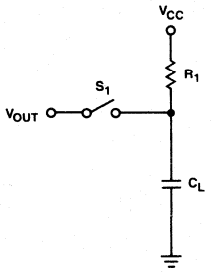
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



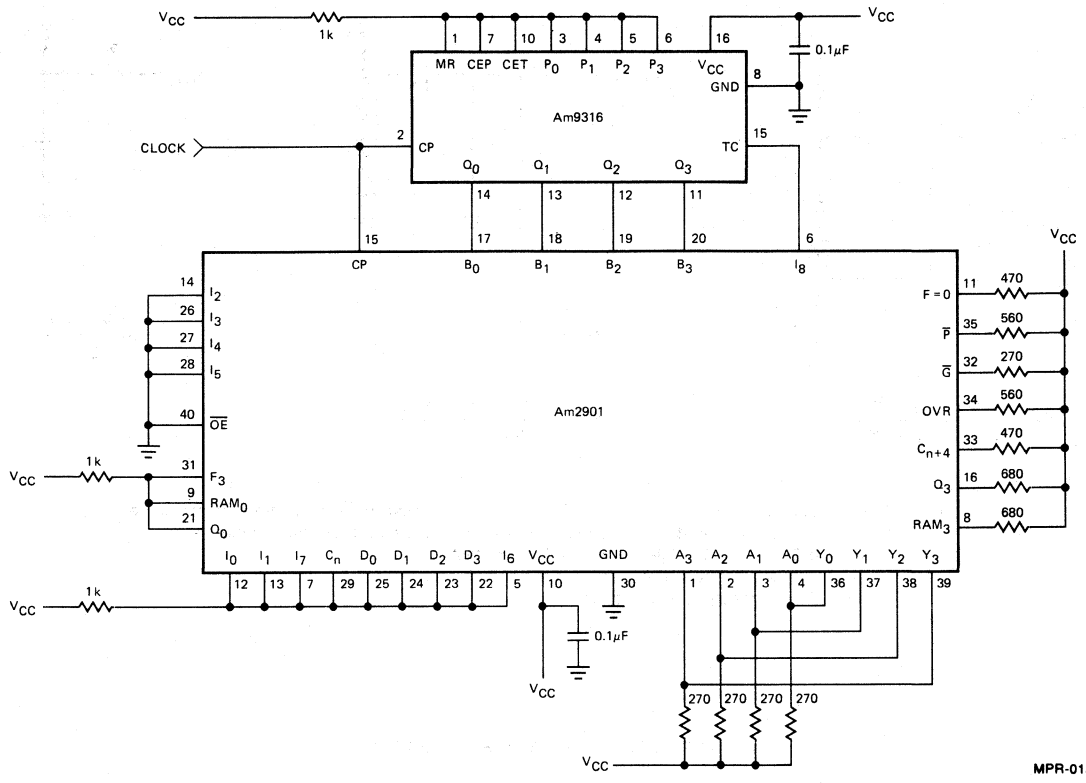
$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2901B

Pin #	Pin Label	Test Circuit	R_1	R_2
3	RAM_3	A	560	1K
5	RAM_0	A	560	1K
7	F = 0	C	270	–
13	Q_3	A	560	1K
18	Q_0	A	560	1K
28	F_3	B	620	3.9K
29	G	B	220	1.5K
30	C_{n+4}	B	360	2.4K
31	OVR	B	470	3K
32	P	B	470	3K
33-36	Y_{0-3}	A	220	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."



V_{CC} = 5.0 V
Frequency = 100 KHz
T_A = 125°C

This circuit conforms to MIL-STD-883, method 1015, condition D.

Figure 14. Life Test and Burn-in Circuit for Military Class B Parts. (Contact Factory for Commercial Burn-in Conditions)

USING THE Am2901

BASIC SYSTEM ARCHITECTURE

The Am2901 is designed to be used in microprogrammed systems. Figure 15 illustrates such an architecture. The nine instruction lines, the A and B addresses, and the D data inputs normally will all come from registers clocked at the same time as the Am2901. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions, typically 28 to 40 bits wide, which apply the proper control signals to the Am2901's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 microprogram sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially these bits are the "next instruction" control.

Note that with the microprogram register in-between the microprogram memory store and the Am2901's, an instruction accessed on one cycle is executed on the next cycle. As one instruction is executed, the next instruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2901's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

EXPANSION OF THE Am2901

The Am2901 is a four-bit CPU slice. Any number of Am2901's can be interconnected to form CPU's of 12, 16, 24, 36 or more bits, in four-bit increments. Figure 16 illustrates the interconnection of three Am2901's to form a 12-bit CPU, using ripple carry. Figure 17 illustrates a 16-bit CPU using carry lookahead, and Figure 18 is the general carry lookahead scheme for long words.

With the exception of the carry interconnection, all expansion schemes are the same. Refer to Figure 16. The Q_3 and RAM_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the Q_0 and RAM_0 pins of the adjacent more significant device. These connections allow the Q-registers of all Am2901's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to three-state multiplexers which can be controlled by the microcode to select the appropriate input signals to the shift inputs. (See Figure 19)

The open collector F = 0 outputs of all the Am2901's are connected together and to a pull-up resistor. This line will go HIGH if and only if the output of the ALU contains all zeroes. Most systems will use this line as the Z (zero) bit of the processor status word.

The overflow and F_3 pins are generally used only at the most significant end of the array, and are meaningful only when two's complement signed arithmetic is used. The overflow pin is the Exclusive-OR of the carry-in and carry-out of the sign bit (MSB). It will go HIGH when the result of an arithmetic

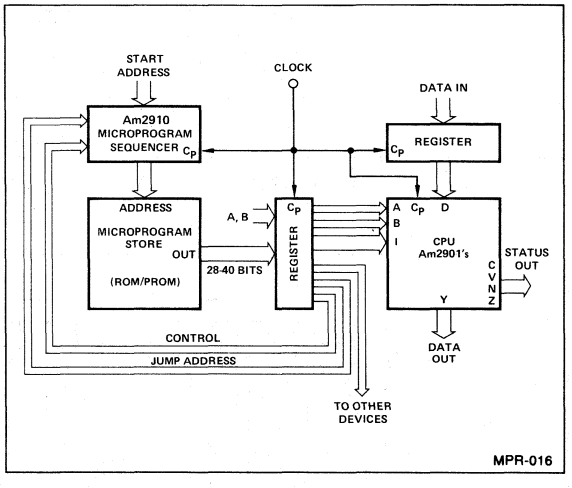


Figure 15. Microprogrammed Architecture Around Am2901's.

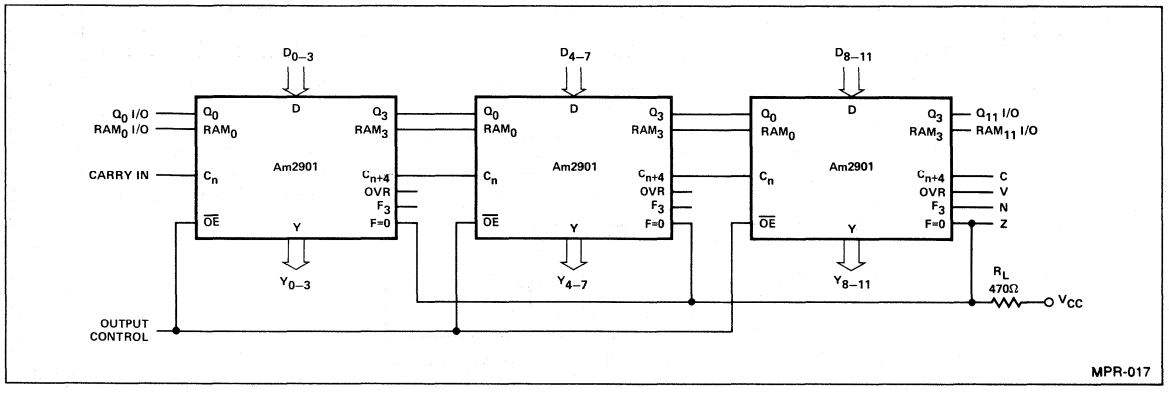


Figure 16. Three Am2901's used to Construct 12-Bit CPU with Ripple Carry. Corresponding A, B, and I Pins on all Devices are Connected Together.

operation is a number requiring more bits than are available, causing the sign bit to be erroneous. This is the overflow (V) bit of the processor status word. The F_3 pin is the MSB of the ALU output. It is the sign of the result in two's complement notation, and should be used as the Negative (N) bit of the processor status word.

The carry-out from the most significant Am2901 (C_{n+4} pin) is the carry-out from the array, and is used as the carry (C) bit of the processor status word.

Carry interconnections between devices may use either ripple carry or carry lookahead. For ripple carry, the carry-out (C_{n+4}) of each device is connected to the carry-in (C_n) of the next more significant device. Carry lookahead uses the Am2902 lookahead carry generator. The scheme is identical to that used with the 74181/74182. Users unfamiliar with this technique should refer to AMD's application note on Arithmetic Logic Units. Figures 17 and 18 illustrate single and multiple level lookahead.

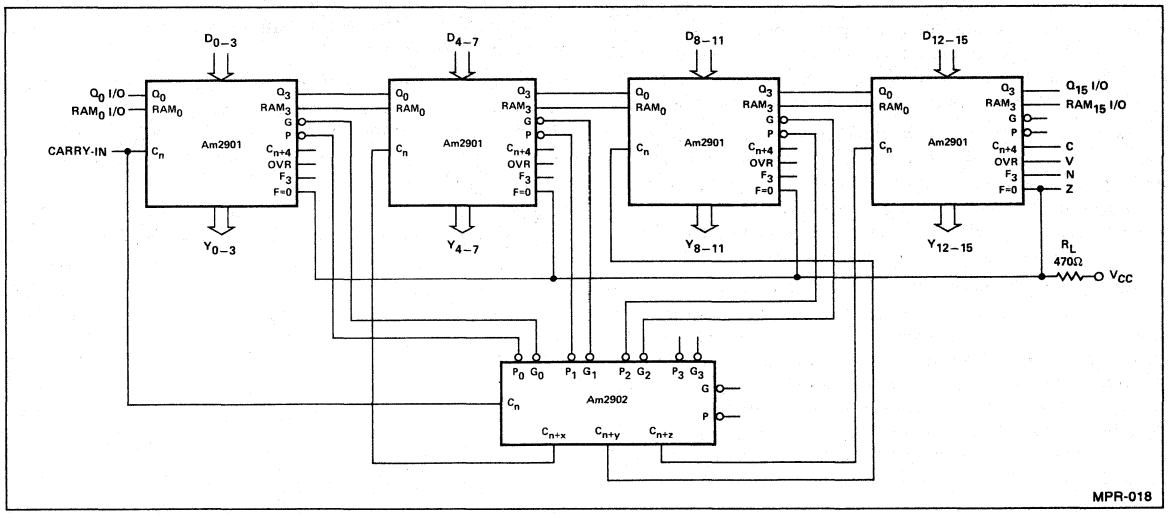


Figure 17. Four Am2901s in a 16-Bit CPU Using the Am2902 for Carry Lookahead.

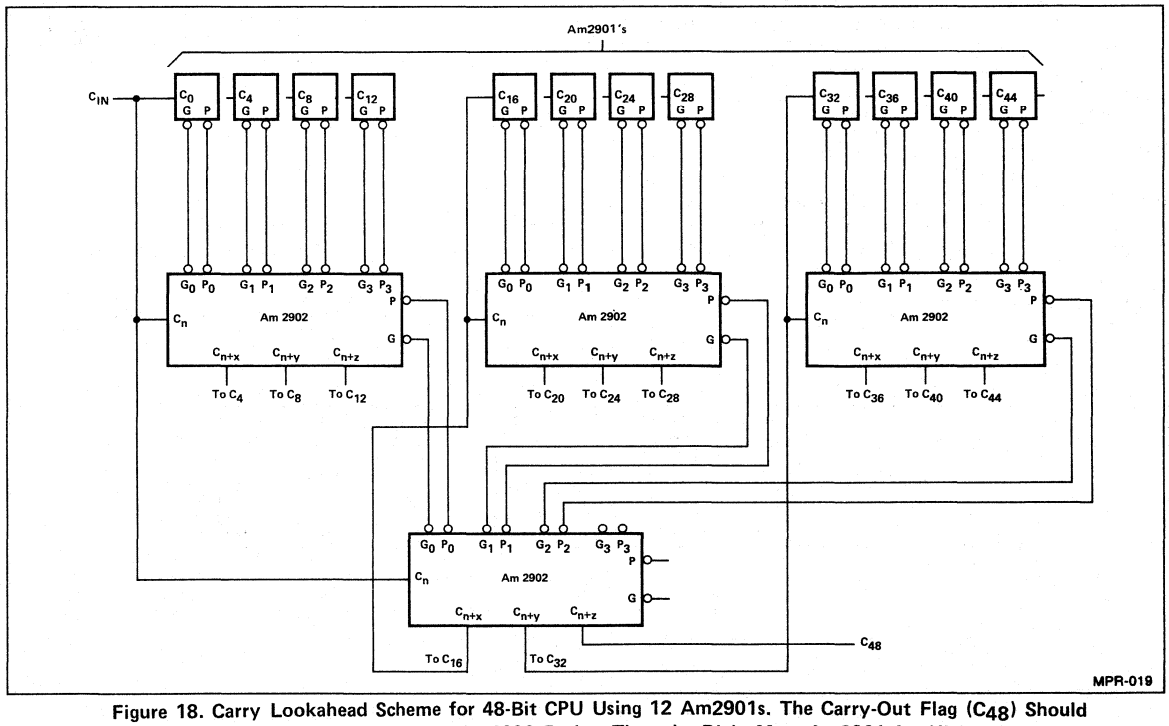


Figure 18. Carry Lookahead Scheme for 48-Bit CPU Using 12 Am2901s. The Carry-Out Flag (C_{48}) Should be Taken From the Lower Am2902 Rather Than the Right-Most Am2901 for Higher Speed.

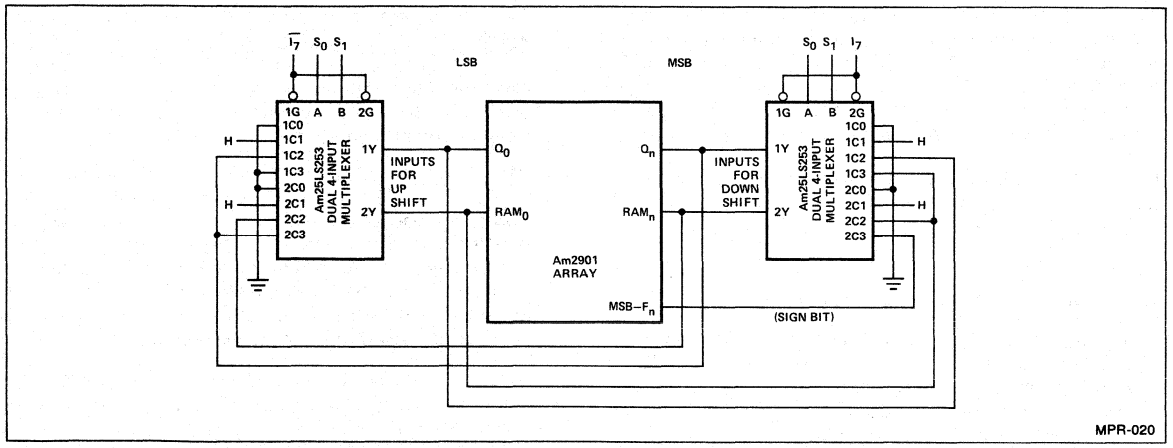


Figure 19. Three-State Multiplexers Used on Shift I/O Lines.

SHIFT I/O LINES AT THE END OF THE ARRAY

The Q-register and RAM left/right shift data transfers occur between devices over bidirectional lines. At the ends of the array, three-state multiplexers are used to select what the new inputs to the registers should be during shifting. The Am2904 includes these multiplexers in a single LSI chip. Figure 19 shows two Am25LS253 dual four-input multiplexers connected to provide four shift modes. Instruction bit I_7 (from the Am2901) is used to select whether the left-shift multiplexer or the right-shift multiplexer is active. The four shift modes in this example are:

Zero A LOW is shifted into the MSB of the RAM on a down shift. If the Q-register is also shifted, then a LOW is deposited in the Q-register MSB. If the RAM or both registers are shifted up, LOWs are placed in the LSBs.

One Same as zero, but a HIGH level is deposited in the LSB or MSB.

Rotate A single precision rotate. The RAM MSB shifts into the LSB on a right shift and the LSB shifts into the MSB on a left shift. The Q-register, if shifted, will rotate in the same manner.

Arithmetic A double-length Arithmetic Shift if Q is also shifted. On an up shift a zero is loaded into the Q-register LSB and the Q-register MSB is loaded into the RAM LSB. On a down shift, the RAM LSB is loaded into the Q-register MSB and the ALU output MSB (F_n, the sign bit) is loaded into the RAM MSB. (This same bit will also be in the next less significant RAM bit.)

Code			Source of New Data				Shift	Type
I_7	S_1	S_0	Q_0	Q_n	RAM_0	RAM_n		
H	L	L	0	Q_{n-1}	0	F_{n-1}	Up	Zero
H	L	H	1	Q_{n-1}	1	F_{n-1}		One
H	H	L	Q_n	Q_{n-1}	F_n	F_{n-1}		Rotate
H	H	H	0	Q_{n-1}	Q_n	F_{n-1}		Arithmetic
L	L	L	Q_1	0	F_1	0	Down	Zero
L	L	H	Q_1	1	F_1	1		One
L	H	L	Q_1	Q_0	F_1	F_0		Rotate
L	H	H	Q_1	F_0	F_1	$RAM_n = RAM_{n-1} = F_n$		Arithmetic

HARDWARE MULTIPLICATION

Figure 20 illustrates the interconnections for a hardware multiplication using the Am2901. The system shown uses two devices for 8 x 8 multiplication, but the expansion to more bits is simple — the significant connections are at the LSB and MSB only.

The basic technique used is the "add and shift" algorithm. One clock cycle is required for each bit of the multiplier. On each cycle, the LSB of the multiplier is examined; if it is a "1", then the multiplicand is added to the partial product to generate a new partial product. The partial product is then shifted one place toward the LSB, and the multiplier is also shifted one place toward the LSB. The old LSB of the multiplier is discarded. The cycle is then repeated on the new LSB of the multiplier available at Q_0.

The multiplier is in the Am2901 Q-register. The multiplicand is in one of the registers in the register stack, R_a. The product will be developed in another of the registers in the stack, R_b.

The A address inputs are used to address the multiplicand in R_a, and the B address inputs are used to address the partial product in R_b. On each cycle, R_a is conditionally added to R_b, depending on the LSB of Q as read from the Q_0 output, and both Q and the ALU output are shifted down one place. The instruction lines to the Am2901 on every cycle will be:

I_{876} = 4 (shift register stack input and Q register left)
I_{543} = 0 (Add)
I_{210} = 1 or 3 (select A, B or 0, B as ALU sources)

Figure 20 shows the connections for multiplication. The circled numbers refer to the paragraphs below.

1. The adjacent pins of the Q-register and RAM shifters are connected together so that the Q-registers of both (or all) Am2901s shift left or right as a unit. Similarly, the entire eight-bit (or more) ALU output can be shifted as a unit prior to storage in the register stack.

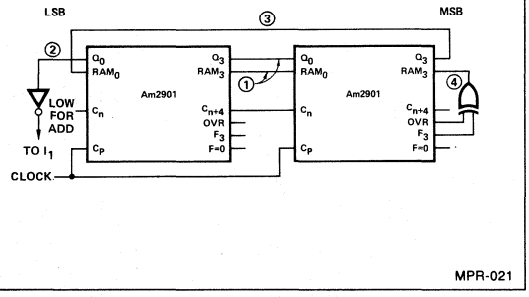


Figure 20. Interconnection for Dedicated Multiplication (8 by 8 Bit) (Corresponding A, B and I Connected Together).

2. The shift output at the LSB of the Q-register determines whether the ALU source operands will be A and B (add multiplicand to partial product) or 0 and B (add nothing to partial product. Instruction bit I_1 can select between A, B or 0, B as the source operands; it can be driven directly from the complement of the LSB of the multiplier.

3. As the new partial product appears at the input to the register stack, it is shifted left by the RAM shifter. The new LSB of the partial product, which is complete and will not be affected by future operations, is available on the RAM_0 pin. This signal is returned to the MSB of the Q-register. On each cycle then, the just-completed LSB of the product is deposited in the MSB of the Q-register; the Q-register fills with the least significant half of the product.

4. As the ALU output is shifted down on each cycle, the sign bit of the new partial product should be inserted in the RAM MSB shift input. The F_3 flag will be the correct sign of the partial product unless overflow has occurred. If overflow occurs during an addition or subtraction, the OVR flag will go HIGH and F_3 is not the sign of the result. The sign of the result must then be the complement of F_3. The correct sign bit to shift into the MSB of the partial product is therefore $F3 \oplus OVR$; that is, F_3 if overflow has not occurred and $\overline{F}_3$ if overflow has occurred. On the last cycle, when the MSB of the multiplier is examined, a conditional subtraction rather than addition should be performed, because the sign bit of the multiplier carries negative rather than positive arithmetic weight.

$$Y = -Y_i 2^i + Y_{i-1} 2^{i-1} + \ldots + Y_0 2^0$$

This scheme will produce a correct two's complement product for all multiplicands and multipliers in two's complement notation.

Figure 21 is a table showing the input states of the Am2901 for each step of a signed, two's complement multiplication. The Am2904 LSI chip conveniently implements the required shift linkages and the EX-OR function for this algorithm.

Initial Register States

R

0	Multiplier
1	Multiplicand
2	X
3	X

Am2901 Microcode

Program 2's Comp. Multiply

Date 8/5/75 By J. S.

Final Register States

R

0	Multiplier
1	Multiplicand
2	LSH Product
3	MSH Product

S, F →	D	Description	Repeat	Pin States (Octal)										Jump	
				A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	To	If
O ∨ A	Q	Move Multiplier to Q	–	0	X	0	3	4	X	X	X	X	X		
O ∧ B	B	Clear R_3	–	X	3	2	4	3	X	X	X	X	X		
(O+B)/2 (A+B)/2	B	Cond. Add & Shift	n–1	1	3	4	0	1 or 3 $I_1 = Q_0$ LO	0	–	RAM_0	–	$F_3 \forall OVR$		
(B–O)/2 (B–A)/2	B	Cond. Subt. & Shift	–	1	3	4	1	1 or 3 $I_1 = Q_0$ LO	1	–	RAM_0	–	$F_3 \forall OVR$		
O ∨ Q	B	Move LSH Prod. to R_2	–	X	2	2	3	2	X	X	X	X	X		

X = Don't Care S = Source F = Function D = Destination

Figure 21.

HARDWARE DIVISION

Division, unlike multiplication, is much more difficult to realize. One of these difficulties can be easily understood by visualizing a 2n-bit Dividend (X) and an n-bit Divisor (Y). The Quotient (Q) can range from 1 bit (when $X < Y$) to 2 n bits (when $Y = 1$), discarding the attempt to divide by 0. In most of the divide functions, the Remainder (R) is as important to find as is the Quotient – there is no equivalent to it in multiplication. Division becomes even more complicated when negative numbers are represented in the 2's complement notation. In the "everyday" decimal system, using Sign-and-Magnitude notation, dealing with negative numbers is relatively easy: The sign of the quotient is determined first and then a normal division is performed. Note that in this "normal" division we first "guess" the first digit of the quotient by comparing the most significant part of the dividend to the divisor. Then verify our guess by a multiplication (no "direct" division method is known), and continue to do so for all of the other digits, shifting the divisor to the right one place at a time.

The most straightforward division scheme (for unsigned numbers) is Subsequent Subtraction. The algorithm is as follows: Subtract divisor from dividend and increment a counter (initially reset to zero). Continue to do so as long as the Remainder is positive. When the Remainder becomes negative cancel the last step; i.e., add back divisor and decrement counter. The counter will contain the Quotient and the Remainder will be correct. The main drawback of this scheme is, of course, the great number of arithmetic operations needed. Again, when dealing with signed numbers, the subtraction should be substituted by addition and vice versa.

A more rapid division can be realized by calculating the Quotient digits instead of counting them. In this algorithm, the divisor is first subtracted from the most significant part of the dividend. If the remainder is positive, the quotient digit is "1," otherwise the subtraction is cancelled (by adding the divisor to the remainder) and the quotient digit will be "0." Now shift the remainder one place to the right (much like you do in a "paper and pencil" division) and repeat until all the quotient digits have been calculated. This algorithm is called "Restoring Division." When signed numbers are involved, inversion of the operations and the quotient digits will be necessary and correction should be performed in some cases. Some time is wasted in the Restoring Division because for every "0" digit in the quotient, two arithmetic operations are needed. This can be saved in the "Non-Restoring Division."

The basis of Non-Restoring Division is the same as in Restoring Division. Consider first unsigned (positive) numbers only. At the beginning, the divisor is subtracted from the most significant part of the dividend. If the result (first remainder) is positive (or zero), the first quotient digit is "1." Otherwise, the quotient digit is "0," but do not restore. Shift divisor one place to the right (or remainder to the left) and add if last quotient digit was "0;" otherwise subtract. Determine quotient digit as before and continue until all quotient digits have been computed. The remainder will be correct if it is non-negative, otherwise correction is needed by a restoring operation (on the remainder only). Extreme care should be taken of the number of bits and the value of the divisor. Assuming the divisor has n bits and the dividend as 2n bits, the above process develops n + 1 bits of the quotient. This will not be sufficient if the divisor is a small number and more digits are needed in the quotient. This condition can be easily detected as the most significant half of the dividend will be greater than the divisor in this case and division can then be terminated after setting the overflow flag. The flow chart for unsigned nonrestoring division is shown in Figure 25.

The unsigned division scheme can be applied to signed *positive* numbers without any change. When negative numbers are encountered, however, changes in the algorithm are necessary. The straightforward method of signed division seems to be "division in the first quadrant." In that scheme, negative numbers are 2's complemented to obtain positive numbers, remembering the changes done. If overflow occurs when the dividend is complemented (i.e., dividend is $-2^{2n} - 1$, the least negative number), the overflow flag can be set and an exit from the routine taken. This is due to the fact that $(-2^{2n} - 1)$ divided by any number of n-bits cannot be represented in n bits. On the other hand, if overflow occurs when the divisor is complemented, a more complex action is needed. In this case, the dividend and the divisor should be shifted right by one place and the shifted out bit should be stored in a flag, say "Z." At the same time, a flag, "W" should also be set to indicate that division by -2^n is being attempted. These actions need to be taken since the quotient might be representable in n bits. (Here instead of dividend = divisor quotient or remainder, we have [dividend /2] = [divisor /2] * quotient + [rem /2]. The remainder obtained should be shifted left and the bit Z be added to give the correct remainder.) The division is performed on possible numbers, and finally 2's complementing is done whenever necessary. Figure 22 is the flowchart for this algorithm.

Figure 23 is the Interconnection Diagram for Division Algorithm. It is assumed that the most significant half Dividend is in Register R_X (it will be lost during the division and replaced by the Remainder), the least significant half in the Q Register and that the Divisor is in Register R_Y. The Quotient will be generated in the Q register.

After checking the signs of the Dividend and Divisor, setting the flags and negating (using 23 or 24 octal as I_5 through I_0 ALU control bits) when necessary the overflow condition should be checked. If R_X is greater than , then R_Y, overflow occurs, hence the division can be terminated by setting the overflow flag.

The first step in the Division routine is a subtract, then shift the R_X and Q registers up. I_{876} will be 6 in octal while $I_{210} = 1$ in octal and $I_5 = I_4$ = LOW. Pulling the CL bit in the microcode to HIGH, both I_3 and C_n will be high and the ALU is performing a 2's complement subtract. The sign of the Remainder will be latched in the Status Register and the complement of it will be stored in the LSB of the Q register during the shift up operation, which also discards the sign bit of the Remainder.

Now repeating the same operation for all of the other bits of the Remainder with the CL bit in the microcode LOW will leave the control of I_3 to the (complemented) previous sign bit. If it was "0" ($R < 0$), I_3 and C_n will be HIGH and the ALU will subtract; if it was 1 ($R > 0$), I_3 and C_n will be LOW and the ALU will ADD, as required. In each up shift, the complement of the present sign bit will be placed at the right of the Quotient, again, as required.

At the end of the division, the sign bit of the Remainder should be examined and if it is HIGH, the Divisor should be added to it. This can be easily implemented (not depicted on Figure 23) by performing an unconditional ADD (with C_n LOW), letting I_2 LOW, I_0 HIGH and controlling I_1 by the complement of the sign of the Remainder, thus adding to the RX either RY (if $R_S = 1$) or zero (if $R_S = 0$). If the dividend and divisor were shifted right because the divisor was equal to -2^n, the true remainder is obtained by shifting the remainder left and adding the flag "Z." The above method generates n + 1 bits of the quotient ($q_n \ldots q_0$) of which $q_n = 0$, since most significant half of dividend is less than the divisor. The overflow flag should be set if $q_{n-1} = 1$ since $q_{n-1} \ldots q_0$ is an unsigned positive number.

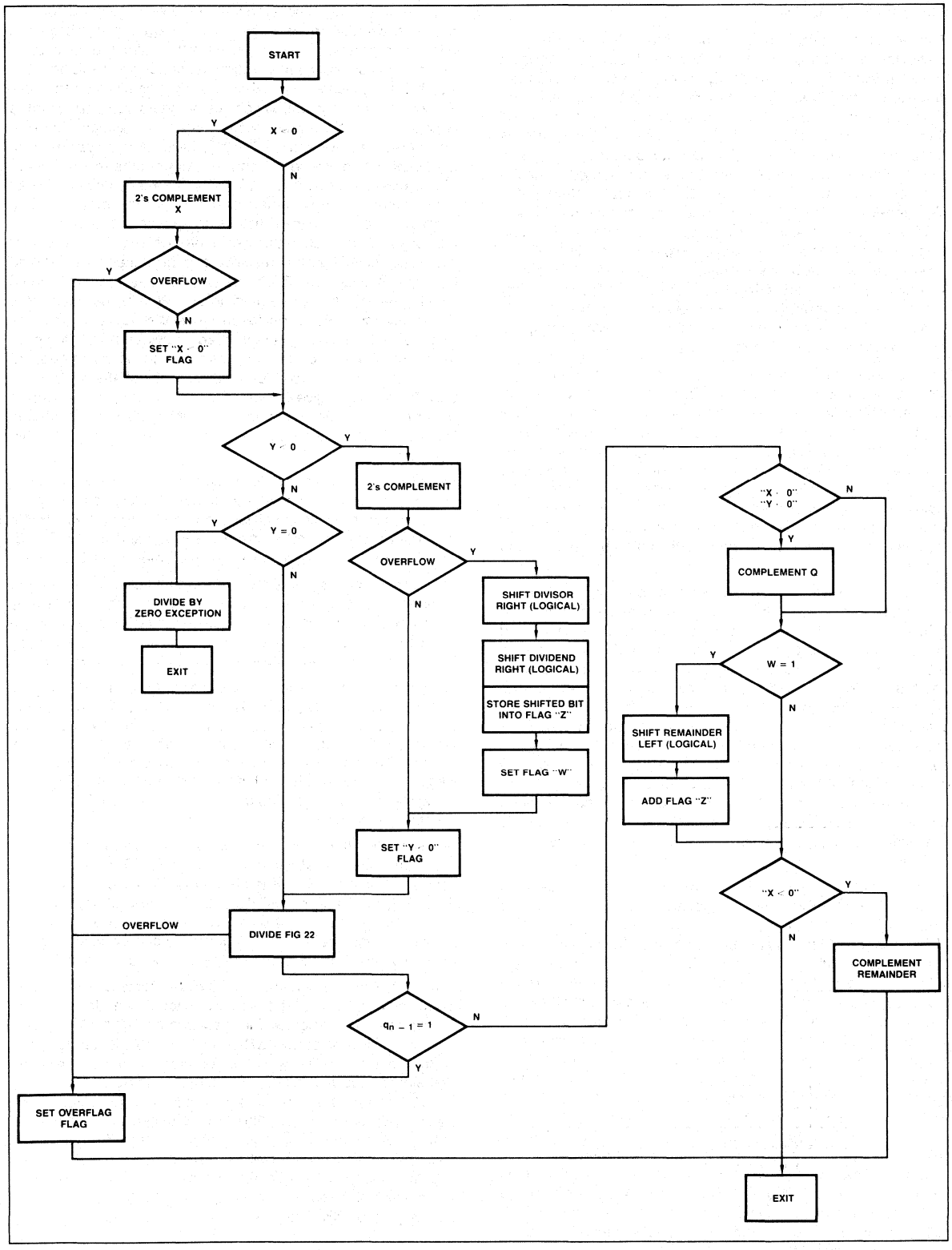


Figure 22. Flowchart for Division with Signed Numbers (Quotient = q_n, $q_{n-1} \ldots q_0$ where $q_n = 0$)

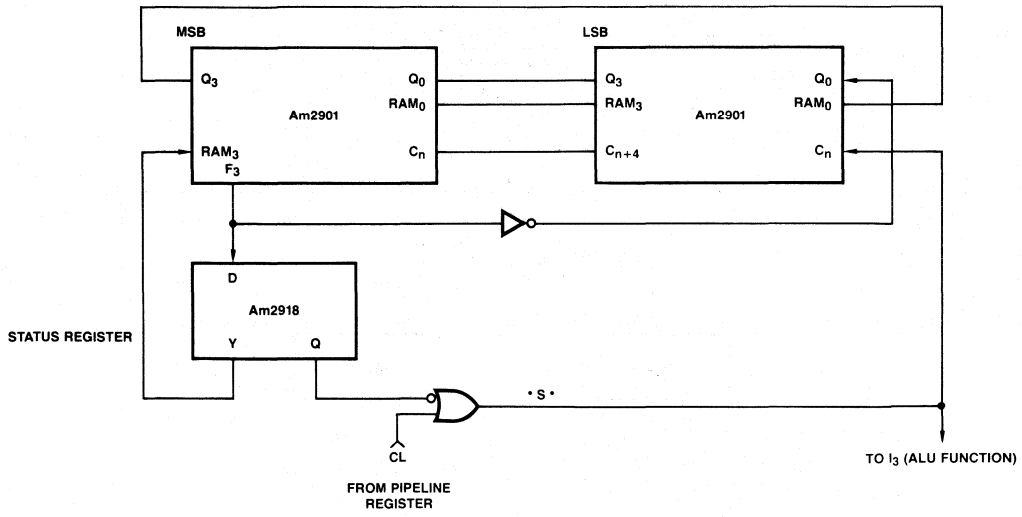


Figure 23. Interconnections for Dedicated Division

Initial Register Status

R

0	MSH Dividend
1	Divisor
Q	LSH Dividend

Am2901 Microcode

Program: 2's Complement Division

Final Register Status

R

0	Remainder
1	Divisor
Q	Quotient

S, F	D	Description	CL	Repeat	Pin Status (Octal) A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	Jump to	Jump if
(B−A) *2	B	First Subtract & Shift	1	–	1	0	6	1	1	1	F_3	X	0	X		
(B±A) *2	B	Loop Subtract/Add & Shift	0	N	1	0	6	1/0	1	1/0	F_3	X	0	X		
B+0	B	Correct Remainder	X	–	1	0	3	0	1/3	0	X	X	X	X		

k = Number of leading zeros of the Divisor
N = Number of bits in the Divisor

Figure 24. Am2901 Microcode for Dedicated Division

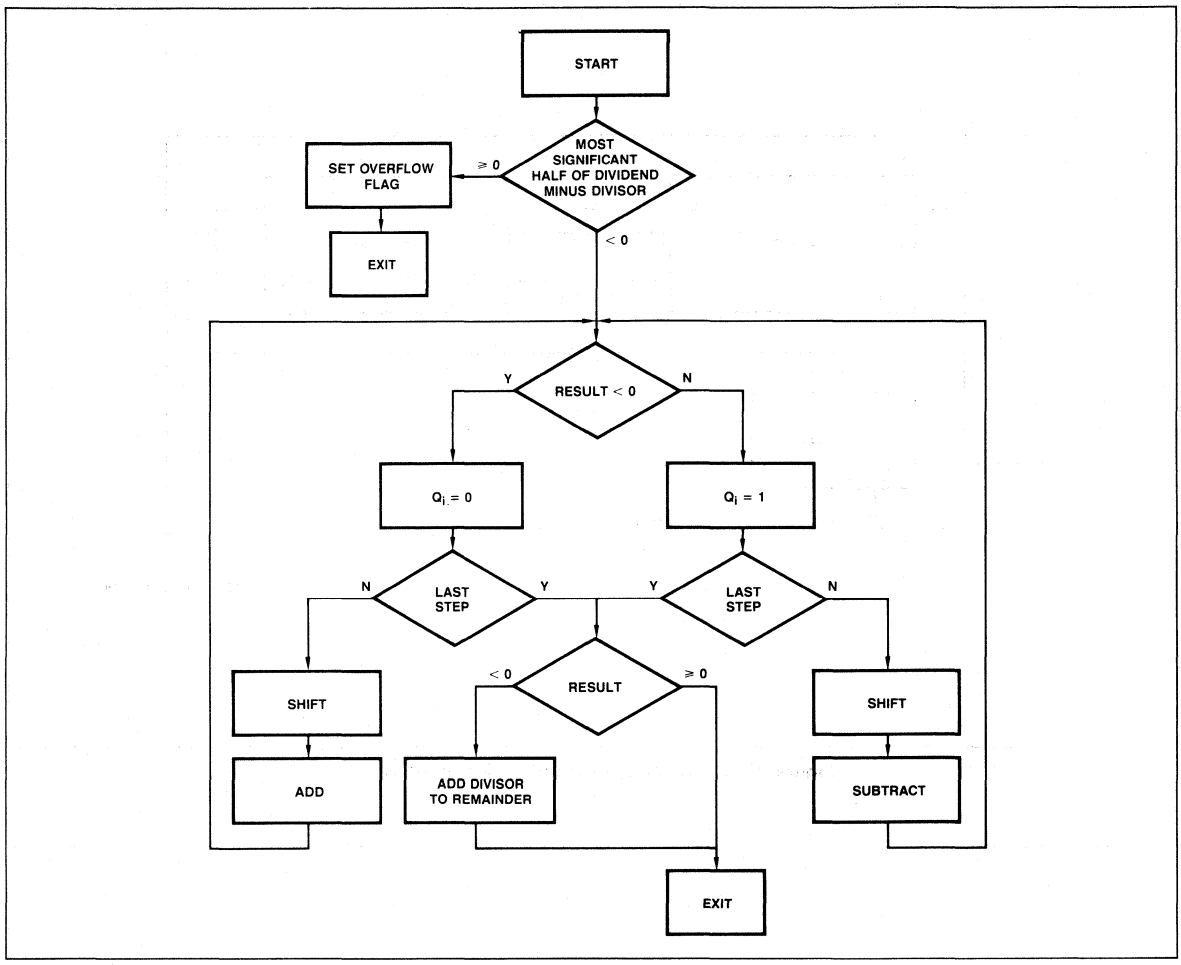


Figure 25. Flowchart for Nonrestoring Division (Unsigned Numbers)

Finally, the Quotient and/or Remainder should be 2's complemented again according to the flags. Complementation of the remainder cannot generate an overflow – because the maximum remainder after divide (Figure 25) is 0011 . . . 1 and the remainder correction when W = 1 can make the remainder at most 0111 . . . 1.

EXAMPLES OF SOME OTHER OPERATIONS

1. Byte Swapping

Occasionally the two halves of a 16-bit word must be swapped. D_{0-7} is interchanged with D_{8-15}. The quickest way to perform this operation is to rotate the word in RAM, shifting two bits at a time. Only four shift cycles are required. The same register is selected on both the A and B ports; the two are added together with carry-in connected to carry-out, producing a right shift of one place; then the ALU is shifted right one more place prior to storage.

Byte Swap of R_0

$A = B = 0$ I = 701 $RAM_0 = RAM_{15}$ $C_{IN} = C_{OUT}$

Repeat 4 times.

2. Instruction Fetch Cycle

Execution of a macroinstruction generally begins with an instruction fetch cycle. The current contents of the PC (in one of the registers) is the address of the macroinstruction to be fetched, and must be read out to the memory address register. Then the PC is incremented to point to the next macroinstruction. The macroinstruction obtained from memory is then loaded into the microprogram sequencer to cause a jump to the microcode for executing the instruction.

The PC can be read out and incremented in one cycle by using the Am2901 destination code 2, and addressing the PC with both the A and B addresses. The current value of PC will appear on the Y outputs, and PC+1 will be returned to the register. If the PC is in register 15, then:

A = B = 15, I = 203, Carry-in = 1

The PC will be on the Y outputs via the RAM A-port. On the clock LOW-to-HIGH transition, the program counter is incremented and the value on the Y outputs is loaded into the memory address register. During the following cycle, the memory is read and, on the next clock LOW-to-HIGH transition the instruction from the memory is dropped into the instruction register. The fetch operation requires only two microcycles.

Am2901C

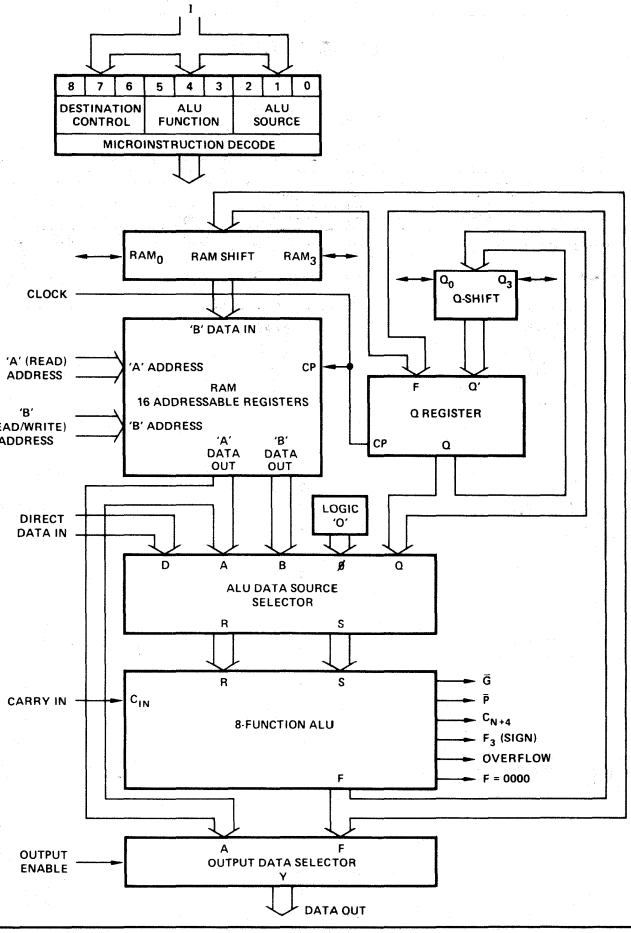
Four-Bit Bipolar Microprocessor Slice

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Third generation of Am2901 four-bit slice**
  Internal ECL circuitry and state-of-the-art process technology combined to provide fastest version of popular Am2901.
- **Plug-in replacement for Am2901, Am2901A, Am2901B**
  The Am2901C is a pin-for-pin replacement for earlier versions of the device. Only the switching speeds are changed.
- **Improved speed**
  25-30% speed improvement on the critical paths versus the Am2901B

MICROPROCESSOR SLICE BLOCK DIAGRAM



MPR-044

6

Am2902A
High-Speed Look-Ahead Carry Generator

DISTINCTIVE CHARACTERISTICS

- Provides look-ahead carries accross a group of four Am2901 or Am2903 microprocessor ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 4.5ns
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

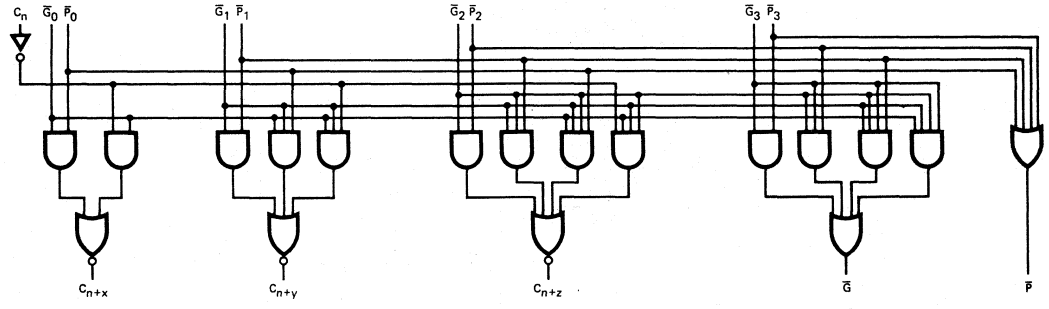
The Am2902A is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The Am2902A is generally used with the Am2901 bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

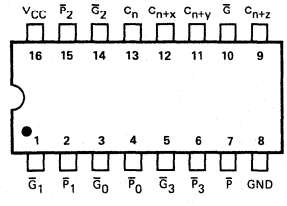
$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

LOGIC DIAGRAM



MPR-026

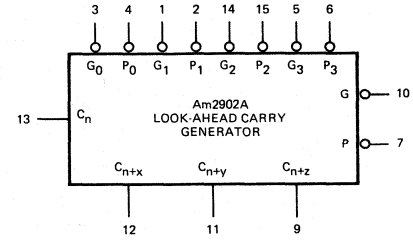
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-027

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-02

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2902AXC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2902AXM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	C_n			−2	mA
			$\overline{P}_3$			−4	
			$\overline{P}_2$			−6	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			−8	
			$\overline{G}_0, \overline{G}_2$			−14	
			$\overline{G}_1$			−16	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n			50	µA
			$\overline{P}_3$			100	
			$\overline{P}_2$			150	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			200	
			$\overline{G}_0, \overline{G}_2$			350	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 3)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All Outputs LOW	MIL		69	99	mA
			COM'L		69	109	
		V_{CC} = MAX. All Ouputs HIGH	MIL		35		mA
			COM'L		35		

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	C_n to C_{n+x}, C_{n+y}, or C_{n+z}		6.5	10	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			7	10.5		
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}		4.5	7	ns	
t_{PHL}			4.5	7		
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$		5	7.5	ns	
t_{PHL}			7	10.5		
t_{PLH}	$\overline{P}_i$ to $\overline{P}$		4.5	6.5	ns	
t_{PHL}			6.5	10		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Max.	T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	C_n to C_{n+x}, C_{n+y}, or C_{n+z}		13		15	ns	C_L = 50pF, R_L = 280Ω
t_{PHL}			14		16.5	ns	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}		8		9.5	ns	
t_{PHL}			9		11.5	ns	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$		12		16.5	ns	
t_{PHL}			12		13.5	ns	
t_{PLH}	$\overline{P}_i$ to $\overline{P}$		9.5		11.5	ns	
t_{PHL}			11		12	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

C_n Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth Am2901A microprocessor ALU input.

C_{n+j} Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n+1, n+2 and n+3 microprocessor ALU slices.

G_i, P_i Generate and propagate inputs respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n+1, n+2 and n+3 microprocessor ALU slices.

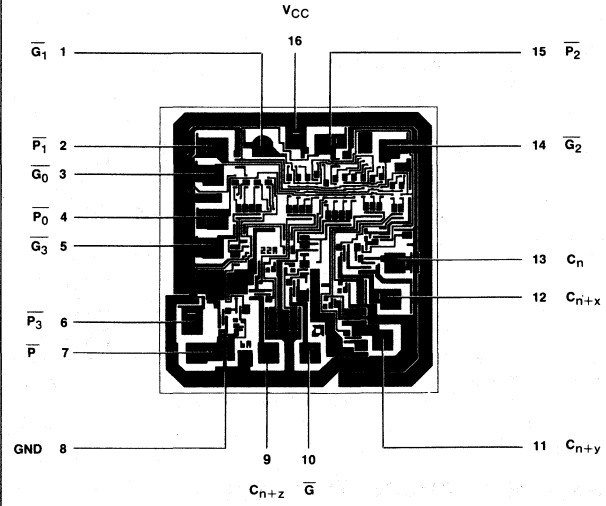
G, P Generate and propagate outputs respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H	H					L		
X	X	X	H	H	X	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
X	X		X	X	X	X	H	H				H	
X	X		X	X	H	H	H	X				H	
X	H		H	H	H	X	H	X				H	
H	H		H	X	X	X	H	X				L	
X	X		X	X	L	X	X	L				L	
X	X		L	X	X	L	X	L				L	
X	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

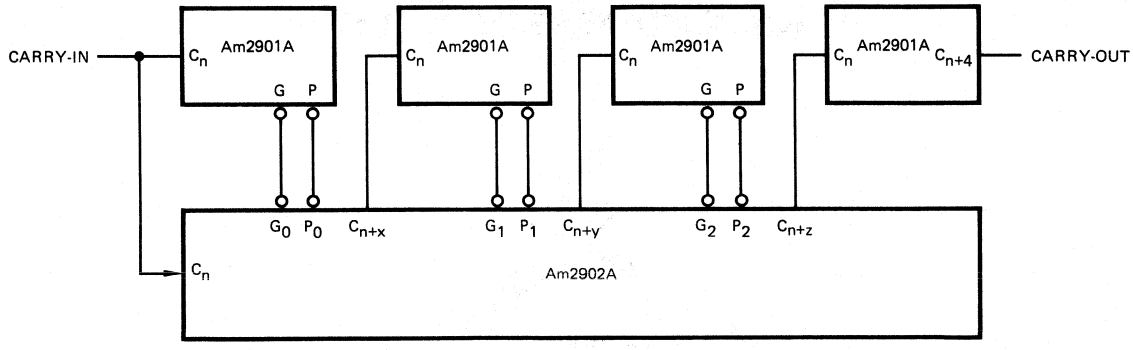
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Metallization and Pad Layout



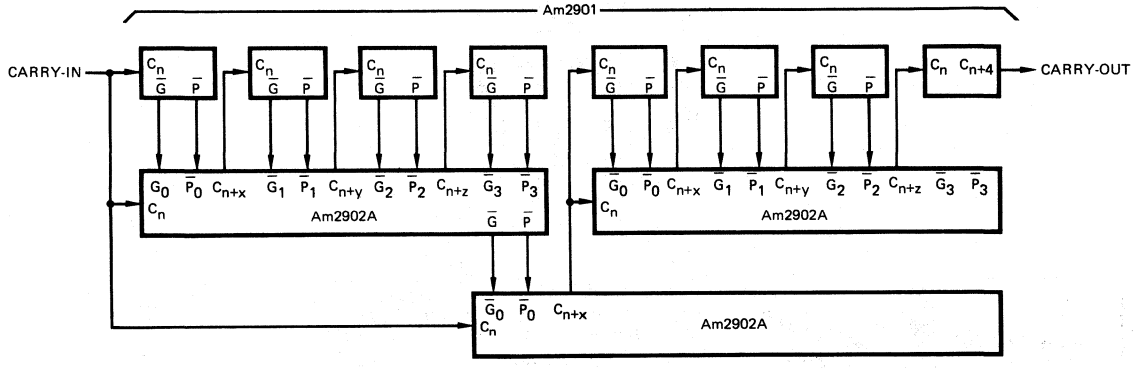
DIE SIZE 0.062" X 0.067"

APPLICATIONS



16-BIT CARRY LOOK-AHEAD CONNECTION.

MPR-028



32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

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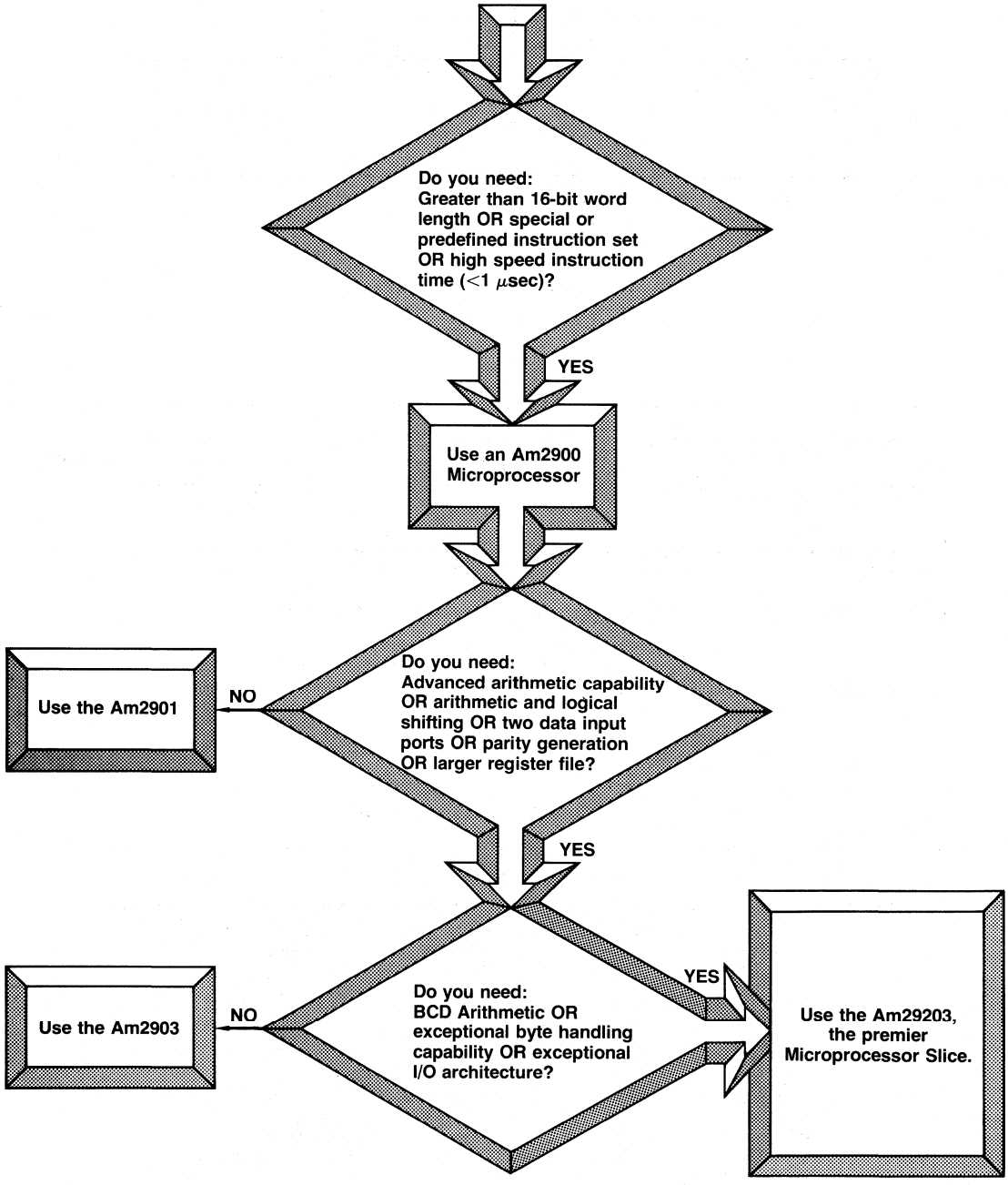
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2902APC	P-16	C	C-1
AM2902ADC	D-16	C	C-1
AM2902ADC-B	D-16	C	B-1
AM2902ADM	D-16	M	C-3
AM2902ADM-B	D-16	M	B-3
AM2902AFM	F-16	M	C-3
AM2902AFM-B	F-16	M	B-3
Am2902AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am2902AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Selecting the #1 Am2900 Microprocessor Slice



Am2903 • Am29203

The Superslice®

DISTINCTIVE CHARACTERISTICS

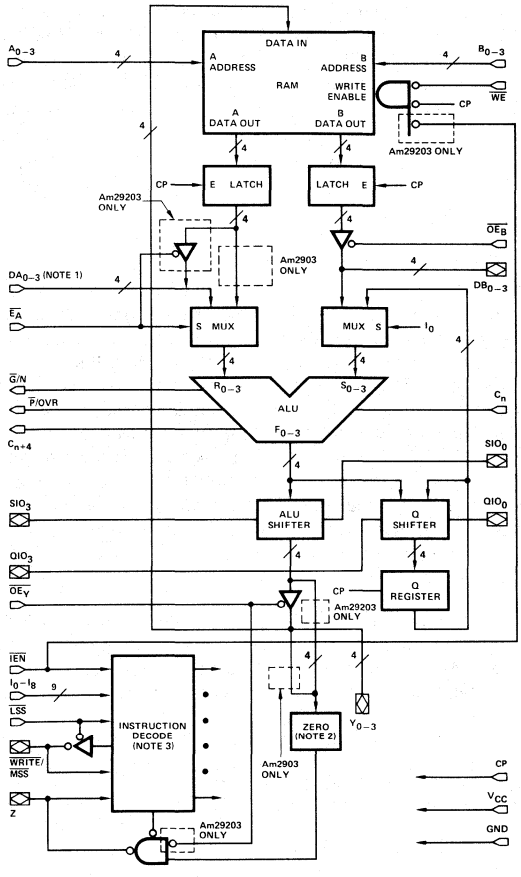
- Expandable Register File –
  Like the Am2901, the Am2903/29203 contains 16 internal working registers arranged in a two-address architecture. But the Am2903/29203 includes the necessary "hooks" to expand the register file externally to any number of registers.
- Built-in Multiplication Logic –
  Performing multiplication with the Am2901A requires a few external gates – these gates are contained on-chip in the Am2903/29203. Three special instructions are used for unsigned multiplication, two's complement multiplication and the last cycle of a two's complement multiplication.
- Built-in Division Logic –
  The Am2903/29203 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- Built-in Normalization Logic –
  The Am2903/29203 can simultaneously shift the Q Register and count in a working register. Thus, the mantissa and exponent of a floating-point number can be developed using a single microcycle per shift. Status flags indicate when the operation is complete.
- Built-in Parity Generation Circuitry –
  The Am2903/29203 can supply parity across the entire ALU output for use in error detection.
- Built-in Sign Extension Circuitry –
  To facilitate operation on different length two's complement numbers, the Am2903/29203 provides the capability to extend the sign at any slice boundary.
- BCD Arithmetic (Am29203 only) –
  Automatic BCD add and subtract and conversion between binary and BCD.
- Improved Byte Handling (Am29203 only) –
  Zero detection and register writing can be performed on a single byte rather than the whole word.
- Two Bidirectional Data Lines (Am29203 only) –

TABLE OF CONTENTS

GENERAL DESCRIPTION

The Am2903 is a four-bit expandable bipolar microprocessor slice. The Am2903 performs all functions performed by the industry standard Am2901 and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am2903. In addition to its complete arithmetic and logic instruction set, the Am2903 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The Am29203 is a similar device, but has additional I/O capability, more special instructions and will be at least 30% faster.

BLOCK DIAGRAM



Notes: 1. DA_{0-3} is input only on Am2903, but is I/O port on Am29203.
2. On Am2903, zero logic is connected to Y, after the $\overline{OE}_Y$ buffer.
3. On Am2903 $\overline{IEN}$ controls $\overline{WRITE}$. On Am29203 $\overline{WRITE}$ is not affected by $\overline{IEN}$.

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ARCHITECTURE OF THE Am2903 AND Am29203

The Am2903/29203 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPUs, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the Am2903/29203 allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function and destination. The Am2903/29203 is cascadable with full lookahead or ripple carry, has 3-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OE}_B$ three-state output enable, RAM data can be read directly at the Am2903 DB I/O port. On the Am29203, E_A provides the same feature at the DA port.

External data at the Am2903/29203 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am2903 high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{E}_A$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE}_B$ and I_0 inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am2903 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table I shows all possible pairs of ALU source operands as a function of the $\overline{E}_A$, $\overline{OE}_B$, and I_0 inputs.

When instruction bits I_4, I_3, I_2, I_1, and I_0 are LOW, the Am2903 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am2903 executes instructions other than the nine special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits. The Am29203 ALU is identical, but executes 16 special instructions.

TABLE 1. ALU OPERAND SOURCES

$\overline{E}_A$	I_0	$\overline{OE}_B$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW H = HIGH X = Don't Care

TABLE 2A. Am2903 ALU FUNCTIONS

I_4	I_3	I_2	I_1	Hex Code	ALU Functions	
L	L	L	L	0	I_0 = L	Special Functions
					I_0 = H	F_i = HIGH
L	L	L	H	1	F = S Minus R Minus 1 Plus C_n	
L	L	H	L	2	F = R Minus S Minus 1 Plus C_n	
L	L	H	H	3	F = R Plus S Plus C_n	
L	H	L	L	4	F = S Plus C_n	
L	H	L	H	5	F = $\overline{S}$ Plus C_n	
L	H	H	L	6	F = R Plus C_n	
L	H	H	H	7	F = $\overline{R}$ Plus C_n	
H	L	L	L	8	F_i = LOW	
H	L	L	H	9	F_i = $\overline{R}_i$ AND S_i	
H	L	H	L	A	F_i = R_i EXCLUSIVE NOR S_i	
H	L	H	H	B	F_i = R_i EXCLUSIVE OR S_i	
H	H	L	L	C	F_i = R_i AND S_i	
H	H	L	H	D	F_i = R_i NOR S_i	
H	H	H	L	E	F_i = R_i NAND S_i	
H	H	H	H	F	F_i = R_i OR S_i	

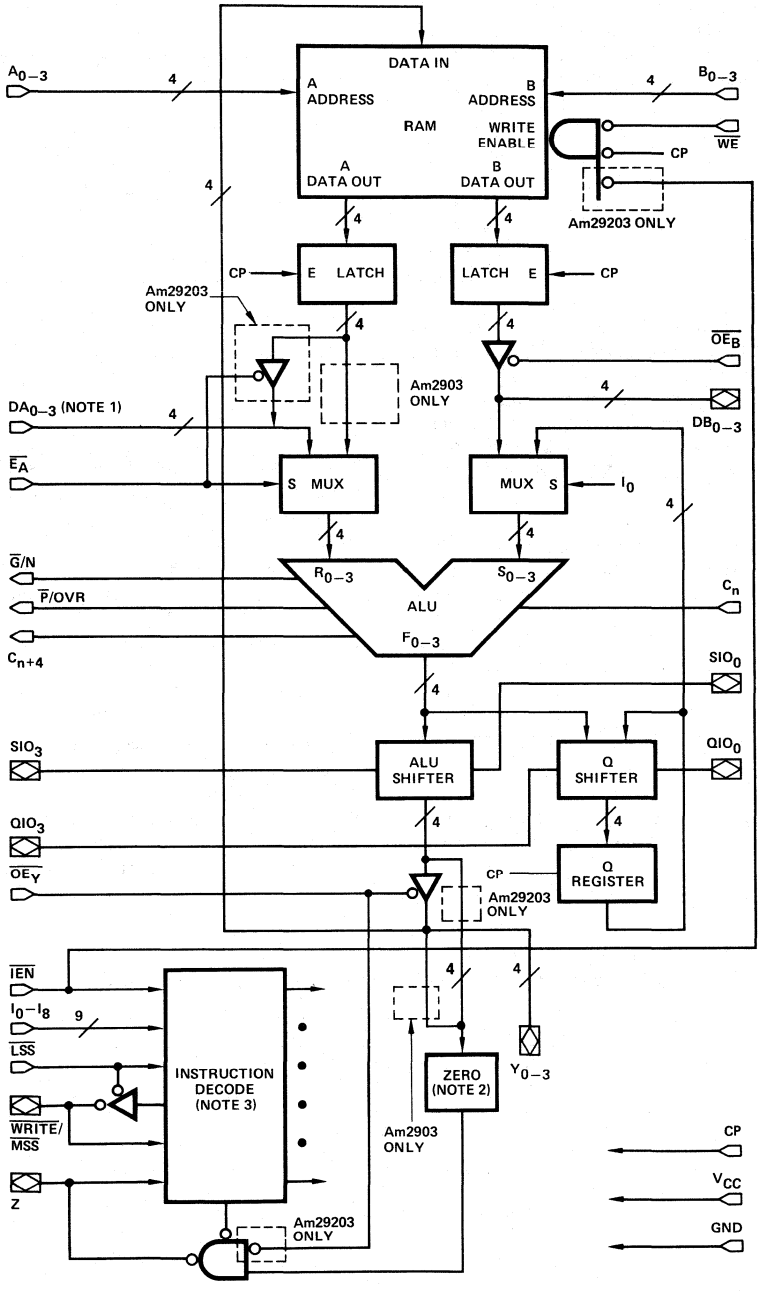
L = LOW H = HIGH i = 0 to 3

TABLE 2B. Am29203 ALU FUNCTIONS

I_4	I_3	I_2	I_1	I_0	ALU Functions
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	F = S Minus R Minus 1 Plus C_n
L	L	H	L	X	F = R Minus S Minus 1 Plus C_n
L	L	H	H	X	F = R Plus S Plus C_n
L	H	L	L	X	F = S Plus C_n
L	H	L	H	X	F = $\overline{S}$ Plus C_n
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	F = R Plus C_n
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	F = $\overline{R}$ Plus C_n
H	L	L	L	L	Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	F_i = $\overline{R}_i$ AND S_i
H	L	H	L	X	F_i = R_i EXCLUSIVE NOR S_i
H	L	H	H	X	F_i = R_i EXCLUSIVE OR S_i
H	H	L	L	X	F_i = R_i AND S_i
H	H	L	H	X	F_i = R_i NOR S_i
H	H	H	L	X	F_i = R_i NAND S_i
H	H	H	H	X	F_i = R_i OR S_i

L = LOW H = HIGH i = 0 to 3
X = LOW or HIGH

BLOCK DIAGRAM



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Notes: 1. DA_{0-3} is input only on Am2903, but is I/O port on Am29203.
2. On Am2903, zero logic is connected to Y, after the $\overline{OE_Y}$ buffer.
3. On Am2903, $\overline{IEN}$ controls $\overline{WRITE}$. On Am29203 $\overline{WRITE}$ is not affected by $\overline{IEN}$.

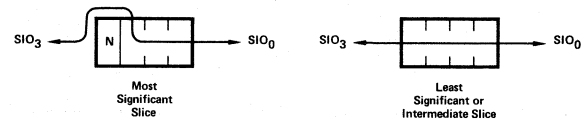
Am2903/29203s may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am2903/29203s are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals required for a lookahead carry scheme are generated by the Am2903/29203 and are available as outputs of the least significant and intermediate slices.

The Am2903/29203 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am2903/29203 instruction.

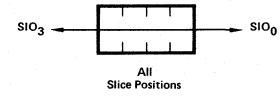
ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.



Am2903/29203 Arithmetic Shift Path



Am2903/29203 Logical Shift Path

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Figure A.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

A cascadable, five-bit parity generator/checker is designed into the Am2903/29203 ALU shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the Am2903/29203 applications section for a more detailed description of the Am2903/29203 sign extension and parity generation/checking capability:

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am2903/29203 executes instructions other than the special functions, the ALU shifter operation is determined by instruction bits $I_8I_7I_6I_5$. Table 3 defines the ALU shifter operation as a function of these four bits.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 OR I_4 = HIGH, $\overline{IEN}$ = LOW.

I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	$\overline{Write}$	Q Reg & Shifter Function	QIO_3	QIO_0
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices							
L	L	L	L	0	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2→Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log. 2Q→Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \forall F_2 \forall F_1 \forall F_0 \forall SIO_3$
$\forall$ = Exclusive OR

L = LOW
H = HIGH

Hi-Z = High Impedance

TABLE A. SPECIAL FUNCTIONS (Note 7)

(Hex) $I_8I_7I_6I_5$	I_4	(Hex) $I_3I_2I_1I_0$	Available On	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig Slice	SIO_3 Other Slices	SIO_0	Q Reg & Shifter Function	QIO_3	QIO_0	$\overline{WRITE}$
0	L	0	Am2903 Am29203	Unsigned Multiply	F = S + C_n if Z = L F = R + S + C_n if Z = H	Log F/2 → Y (Note 1)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
1	L	0	Am29203	BCD to Binary Conversion	(Note 4)	Log F/2 → Y	Input	Input	F_0	Log Q/2 → Q	Input	Q_0	L
1	H	0	Am29203	Multiprecision BCD to Binary	(Note 4)	Log F/2 → Y	Input	Input	F_0	Hold	Input	Q_0	L
2	L	0	Am2903 Am29203	Two's Complement Multiply	F = S + C_n if Z = L F = R + S + C_n if Z = H	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
3	L	0	Am29203	Decrement by One or Two	F = S − 2 + C_n	F → Y	Z	Z	Parity	Hold	Z	Z	L
4	L	0	Am2903 Am29203	Increment by One or Two	F = S + 1 + C_n	F → Y	Input	Input	Parity	Hold	Z	Z	L
5	L	0	Am2903 Am29203	Sign/Magnitude Two's Complement	F = $\overline{S}$ + C_n if Z = L F = $\overline{S}$ + C_n if Z = H	F → Y (Note 3)	Input	Input	Parity	Hold	Z	Z	L
6	L	0	Am2903 Am29203	Two's Complement Multiply, Last Cycle	F = S + C_n if Z = L F = S − R − 1 + C_n if Z = H	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
7	L	0	Am29203	BCD Divide by Two	(Note 4)	F → Y	Z	Z	Parity	Hold	Z	Z	L
8	L	0	Am2903 Am29203	Single Length Normalize	F = S + C_n	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
9	L	0	Am29203	Binary to BCD Conversion	(Note 5)	Log 2F → Y	F_3	F_3	Input	Log 2Q → Q	Q_3	Input	L
9	H	0	Am29203	Multiprecision Binary to BCD	(Note 5)	Log 2F → Y	F_3	F_3	Input	Hold	Q_3	Input	L
A	L	0	Am2903 Am29203	Double Length Normalize and First Divide Op	F = S + C_n	Log 2F → Y	$R_3 \forall F_3$	F_3	Input	Log 2Q → Q	Q_3	Input	L
B	L	0	Am29203	BCD Add	F = R + S + C_n BCD (Note 6)	F → Y	Q	Q	Z	Hold	Z	Z	L
C	L	0	Am2903 Am29203	Two's Complement Divide	F = S + R + C_n if Z = L F = S − R − 1 + C_n if Z = H	Log 2F → Y	$\overline{R_3 \forall F}$	F_3	Input	Log 2Q → Q	Q_3	Input	L
D	L	0	Am29203	BCD Subtract	F = R − S − 1 + C_n BCD (Note 6)	F → Y	Q	Q	Z	Hold	Z	Z	L
E	L	0	Am2903 Am29203	Two's Complement Divide Correction and Remainder	F = S + R + C_n if Z = L F = S − R − 1 + C_n if Z = H	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
F	L	0	Am29203	BCD Subtract	F = S − R − 1 + C_n BCD (Note 6)	F → Y	Q_3	Q	Z	Hold	Z	Z	L

Notes:
1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \forall$ OVR is is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \forall F_3$ is generated at the Y_3 output.
4. On each slice, F = S if magnitude of S_{0-3} is less than 8 and F = S minus 3 if magnitude of S_{0-3} is 8 or greater.
5. On each slice, F = S if magnitude of S_{0-3} is less than 5 and F = S plus 3 if magnitude of S_{0-3} is 5 or greater. Addition is module 16.
6. Additions and subtractions are BCD adds and subtracts. Results are undefined if R or S are not in valid BCD format.
7. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.

L = LOW
H = HIGH
X = Don't Care
Hi-Z = High Impedance
$\forall$ = Exclusive OR
Parity = $SIO_3 \forall F_3 \forall F_2 \forall F_1 \forall F_0$

Q Register

The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Double-length arithmetic and logical shifting capability is provided by the Am2903/29203. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the Am2903/29203 special functions and the operations which the Q Register and shifter perform for each. When the Am2903/29203 executes instructions other than the special functions, the Q Register and shifter operation is controlled by instruction bits $I_8I_7I_6I_5$. Table 3 defines the Q Register and shifter operation as a function of these four bits.

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. On the Am29203, the DA port is also bidirectional. The Y output buffers are enabled when the $\overline{OE_Y}$ input is LOW and are in the high impedance state when $\overline{OE_Y}$ is HIGH. The DB output buffers are

enabled when the $\overline{OE_B}$ input is LOW and the DA buffers are enabled when $\overline{E_A}$ is LOW. (On the Am2903 DA is input only; the pins are never outputs.)

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am2903 and Am29203 instructions. On the Am29203, the Z pin will be HIGH if $\overline{OE_Y}$ is HIGH, allowing zero detection on less than the full word.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}/\overline{MSS}$ input/output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the Am2903 instruction inputs.

On the Am2903, when $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the Am2903 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am2903 divide operation (see Figure B). On the Am29203, $\overline{IEN}$ controls internal writing, but does not affect $\overline{WRITE}$. The $\overline{IEN}$ signal can then be controlled separately at each chip to facilitate byte operations.

Programming the Am2903/29203 Slice Position

Tying the $\overline{LSS}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}/\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{WRITE}/\overline{MSS}$ pin becomes an input pin; tying the $\overline{WRITE}/\overline{MSS}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS). The $\overline{W}/\overline{MSS}$ pin must be tied HIGH through a resistor. $\overline{W}/\overline{MSS}$ and $\overline{LSS}$ should not be connected together. See Figure 2 of applications.

Am2903 SPECIAL FUNCTIONS

The Am2903 provides nine Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

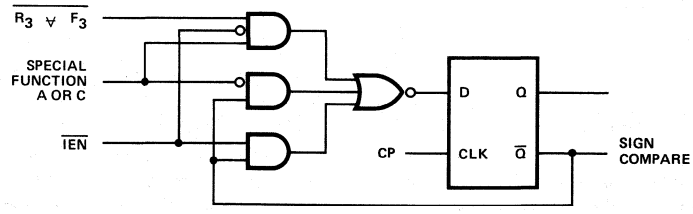
Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am2903. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

Refer to Am2903 applications section for a more detailed description of these Special Functions.



The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

Figure B. Sign Compare Flip-Flop

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TABLE 5. Am2903/Am29203 STATUS OUTPUTS

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	Available On	Gi (i = 0 to 3)	Pi (i = 0 to 3)	C_{n+4}	$\overline{P}$/OVR		$\overline{G}$/N		Z ($\overline{OE}_Y$ = LOW)		
							Most Sig Slice	Other Slices	Most Sig Slice	Other Slices	Most Sig Slice	Intermediate Slice	Least Sig Slice
X	0	X	Am2903/ Am29203	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	Am2903/ Am29203	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	Am2903/ Am29203	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	Am2903/ Am29203	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	Am2903/ Am29203	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	Am2903/ Am29203	0	$\overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	Am2903/ Am29203	0	R_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	Am2903/ Am29203	0	$\overline{R}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	Am2903/ Am29203	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	Am2903/ Am29203	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	Am2903/ Am29203	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	Am2903/ Am29203	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	Am2903/ Am29203	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	Am2903/ Am29203	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	Am2903/ Am29203	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	Am2903/ Am29203	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	Am2903/ Am29203	0 if Z = L $R_i \wedge S_i$ if Z=H	S_i if Z = L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	Am29203	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
1	8	L	Am29203	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
2	0	L	Am2903/ Am29203	0 if Z = L $R_i \wedge S_i$ if Z=H	S_i if Z = L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	Am29203	(Note 6)	(Note 7)	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
4	0	L	Am2903/ Am29203	(Note 1)	(Note 2)	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	Am2903/ Am29203	0	$\overline{S}_i$ if Z = L $\overline{S}_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3 if Z=L $F_3 \forall S_3$ if Z=H	$\overline{G}$	S_3	Input	Input
6	0	L	Am2903/ Am29203	0 if Z = L $\overline{R}_i \wedge S_i$ if Z=H	S_i if Z = L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	Am29203	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
8	0	L	Am2903/ Am29203	0	S_i	(Note 3)	$Q_2 \quad Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	0	L	Am29203	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	8	L	Am29203	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
A	0	L	Am2903/ Am29203	0	S_i	(Note 4)	$F_2 \quad F_1$	$\overline{P}$	F_3	$\overline{G}$	(Note 5)	(Note 5)	(Note 5)
B	0	L	Am29203	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	(Note 8)	(Note 8)	(Note 9)	(Note 9)	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
C	0	L	Am2903/ Am29203	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	Am29203	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
E	0	L	Am2903/ Am29203	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	Am29203	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$

Notes:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_i = S_i$.
3. At the most significant slice, $C_{n+4} = Q_3 \forall Q_2$. At other slices, $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \forall F_2$. At other slices, $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$.
6. If $\overline{LSS}$ is LOW, $G_0 = 0$ and $G_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = S_{0,1,2,3}$.
7. If $\overline{LSS}$ is LOW, $P_0 = S_0$ and $P_{1,2,3} = 1$. If $\overline{LSS}$ is HIGH, $P_{0,1,2,3} = 1$.
8. On All slices $\overline{P} = (\overline{P}_0 + \overline{P}_3)(\overline{P}_0 + \overline{G}_2)(\overline{P}_0 + \overline{G}_1 + \overline{P}_2)$
9. On all slices $\overline{G} = \overline{G}_3(\overline{G}_0 + \overline{G}_1 + \overline{P}_2)(\overline{G}_0 + \overline{G}_1)(\overline{P}_1 + \overline{G}_2)(\overline{P}_3 + \overline{P}_1 \cdot \overline{P}_2 \cdot \overline{G}_0)$.

L = LOW = 0
H = HIGH = 1
$\vee$ = OR
$\wedge$ = AND
$\forall$ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3 \quad G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2$

PIN DEFINITIONS

A_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.

B_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.

$\overline{WE}$ The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.

DA_{0-3} A four-bit external data input which can be selected as one of the Am2903 ALU operand sources; DA_0 is the least significant bit. On the Am29203, the DA path is bidirectional, operating as either an ALU source operand or as an external output for the RAM A-port.

$\overline{EA}$ A control input which, when HIGH selects DA_{0-3} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.

DB_{0-3} A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.

C_n The carry-in input to the Am2903/29203 ALU.

I_{0-8} The nine instruction inputs used to select the Am2903/29203 operation to be performed.

$\overline{IEN}$ The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the Am2903, $\overline{IEN}$ also controls $\overline{WRITE}$. On the Am29203, $\overline{WRITE}$ is not affected by $\overline{IEN}$, but internally disables the RAM write enable.

C_{n+4} This output generally indicates the carry-out of the Am2903/29203 ALU. Refer to Table 5 for an exact definition of this pin.

$\overline{G}$/N A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

$\overline{P}$/OVR A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z An open-collector input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO_0, SIO_3 Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO_0, QIO_3 Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.

$\overline{LSS}$ An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am2903/29203 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.

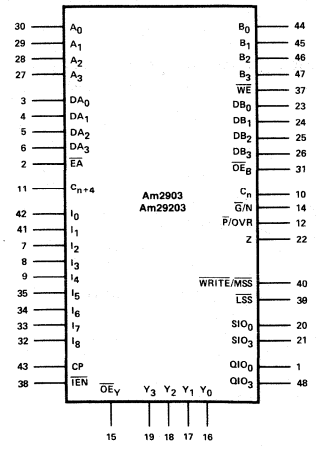
$\overline{WRITE}$/ $\overline{MSS}$ When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).

Y_{0-3} Four data inputs/outputs of the Am2903/29203. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.

CP The clock input to the Am2903/29203. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written into the RAM when CP is LOW.

LOGIC SYMBOL



V_{CC} = Pin 36
GND = Pin 13

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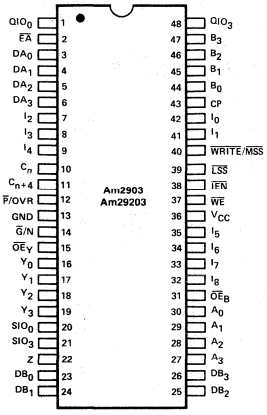
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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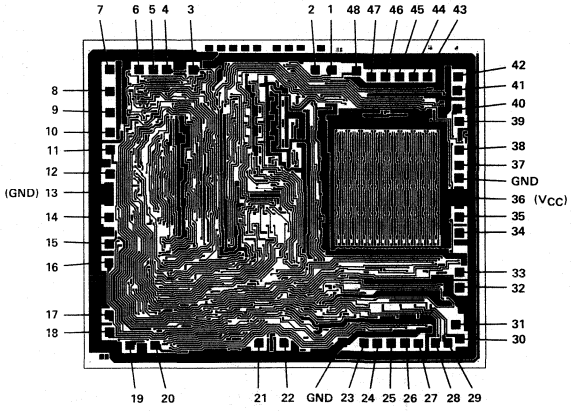
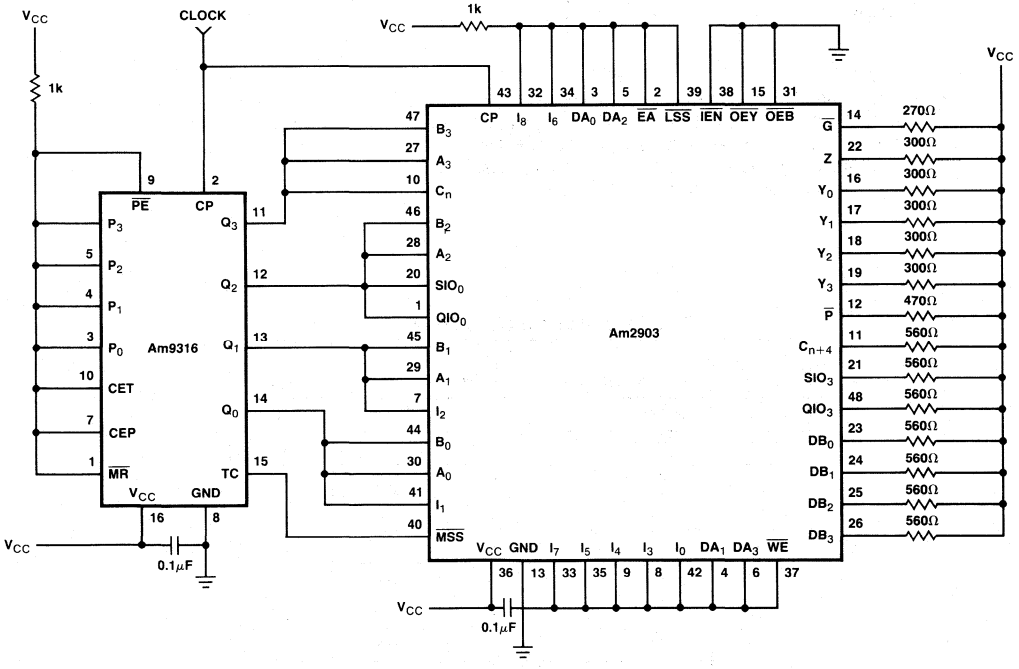
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.163" X 0.197"

Note: Pin numbers correspond to DIP package.

Am 2903



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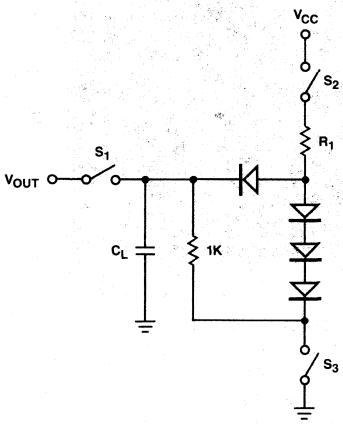
V_{CC} = 5.0V
Frequency = 100kHz
T_A = +125°C
All registers are 1/4 watt ±5%
This circuit conforms to MIL-STD-883, Methods 1005 and 1015, Condition D.
One Am9316 Can Drive Maximum of Five Am2903s.

Am2903 Burn-in and Life Test Circuit

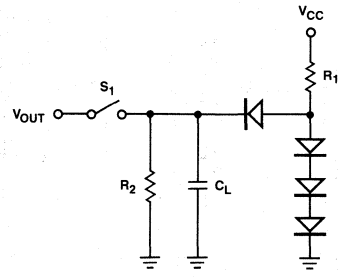
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2903

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

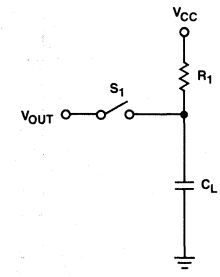
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in hand in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all A.C. tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2903

Pin#	Pin Label	Test Circuit	R_1	R_2
1	QIO_0	A	458	1K
11	C_{n+4}	B	478	3K
12	$\overline{P}$/OVR	B	383	3K
14	$\overline{G}$/N	B	212	1.5K
16-19	Y_{0-3}	A	241	1K
20	SIO_0	A	458	1K
21	SIO_3	A	458	1K
22	Z	C	281	–
23-26	DB_{0-3}	A	458	1K
40	$\overline{WRITE}/\overline{MSS}$	A	458	1K
48	QIO_3	A	458	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

OPERATING RANGES (over which DC, switching, and functional specifications apply)

Range	Part Number Suffix	Temperature	V_{CC}	V_{IH}	V_{IL}
COM'L	PC, PCB, DC, DCB, XC	T_A = 0 to 70°C	4.75 to 5.25V	2.0V	0.8V
MIL	DM, DMB, FM, FMB, XM	T_C = −55 to +125°C	4.50 to 5.50V	2.0V	0.3V

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

6

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am29203 Order Number	Am2903 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29203DC	AM2903DC	D-48	C	C-1
AM29203DC-B	AM2903DC-B	D-48	C	B-2 (Note 4)
AM29203DM	AM2903DM	D-48	M	C-3
AM29203DMB	AM2903DM-B	D-48	M	B-3
AM29203FM	AM2903FM	F-48	M	C-3
AM29203FMB	AM2903FM-B	F-48	M	B-3
Am29203XC	Am2903XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am29203XM	Am2903XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0-Y_3, $\overline{G}$/N		2.4			Volts
			I_{OH} = −800μA DB_{0-3}, $\overline{P}$/OVR SIO_0, SIO_3, QIO_0, QIO_3, $\overline{WRITE}$, C_{n+4}		2.4			
I_{CEX}	Output Leakage Current for Z Output (Note 4)	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} = or V_{IL}	Y_0, Y_1, Y_2 Y_3, Z	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)				
			DB_0, DB_1, DB_2, DB_3	I_{OL} = 12mA (COM'L)			0.5	
				I_{OL} = 8.0mA (MIL)				
			$\overline{G}$/N	I_{OL} = 18mA			0.5	
			$\overline{P}$/OVR	I_{OL} = 10mA			0.5	
			C_{n+4}, SIO_0 SIO_3, QIO_0 QIO_3, $\overline{WRITE}$	I_{OL} = 8.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V (Note 4)	C_n				−3.6	mA
			Y_0, Y_1, Y_2, Y_3				−1.13	
			I_0, I_1, I_2, I_3, I_4 DA_0, DA_1, DA_2, DA_3				−0.72	
			SIO_0, SIO_3, QIO_0, QIO_3, $\overline{MSS}$, DB_0, DB_1, DB_2, DB_3				−0.77	
			All other inputs				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Note 4)	C_n				200	μA
			Y_0, Y_1, Y_2, Y_3				110	
			I_0-I_4, DA_0-DA_3				40	
			SIO_0, SIO_3, QIO_0, QIO_3, DB_{0-3}, $\overline{MSS}$				90	
			All other inputs				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX., (Note 4)	Y_0-Y_3	V_O = 2.4V			110	μA
				V_O = 0.5V			−1130	
			DB_{0-3}, QIO_0, QIO_3, SIO_0, SIO_3, $\overline{WRITE}$/$\overline{MSS}$	V_O = 2.4V			90	
				V_O = 0.5V			−770	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	T_A = 25°C			220	335	mA
			COM'L	T_A = 0 to 70°C			350	
				T_A = 70°C			291	
			MIL	T_C = −55 to 125°C			395	
				T_C = 125°C			258	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-3}, DB_{0-3}, $SIO_{0,3}$, $QIO_{0,3}$ and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

n2903 SWITCHING CHARACTERISTICS

ı2903 switching characteristics are dependent on tempera-
e, voltage, and the operating mode of the device. The detailed
ta for the part is given in the 24 tables comprising Appendix A of this data sheet. For reference, one set of these tables is reproduced on this page and the next. For switching data for special functions and military devices, refer to Appendix A.

TABLE III A
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Standard Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	86	81	69	110	86	108	–	–	–	84	94	115
B Address	99	88	81	123	99	112	49	–	–	94	104	140
A Address (Logic Mode)	87	–	68	111	89	–	–	–	–	79	94	115
B Address	84	–	73	108	84	–	49	–	–	84	90	120
DA Inputs (Arith. Mode)	63	60	49	87	64	89	–	–	–	60	70	101
DB Inputs	61	59	47	85	62	84	–	–	–	62	68	98
DA Inputs (Logic Mode)	64	–	48	88	66	–	–	–	–	61	72	101
DB Inputs	55	–	32	79	57	–	–	–	–	52	61	93
$\overline{EA}$	59	53	42	83	59	83	–	–	–	57	64	98
C_n	40	30	–	64	40	58	–	–	–	38	46	67
I_0	52	48	36	76	52	63	–	49	*	50*	58*	93*
I_{4321}	71	65	72	95	69	84	–	49	*	66*	73*	105*
I_{8765}	42	–	–	66	–	–	–	50	60*	42*	45*	42*
$\overline{IEN}$	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	26	–	–	50	–	–	–	–	–	–	29	36
Clock	87	87	71	111	88	108	37	–	40	84	92	105
Y	–	–	–	24	–	–	–	–	–	–	–	–
$\overline{MSS}$	44	–	44	68	44	44	–	–	–	44	46	44

Note: A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

TABLE III B
Guaranteed Set-up and Hold Times
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions
CAUTION: READ NOTES TO TABLE B. NA = Not Applicable; no timing constraint.

To Output / From Input	With Respect to this Signal	HIGH-to-LOW		LOW-to-HIGH		Comment
		Set-up	Hold	Set-up	Hold	
Y	Clock	NA	NA	20	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	30	0	To Write into RAM
A, B as Sources	Clock	27	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	21	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	68	0	See Note 6

Notes:
1. For set-up times from all inputs not specified in Table B, the set-up time is computed by calculating the delay to stable Y outputs and then allowing the Y set-up time. Even if the RAM is not being loaded, the Y set-up time is necessary to set-up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

TABLE III C
Guaranteed Enable/Disable Times
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	31	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	65	60	ns
$\overline{LSS}$	$\overline{WRITE}$	31	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE III D
Guaranteed Clock and Write Pulse Characteristics
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Time CP and WE both LOW to Write	30	ns

CYCLE TIMES FOR 16-BIT SYSTEM FOR COMMON OPERATIONS

The illustration below shows a typical configuration using 4 Am2903 Superslices, an Am2902A carry lookahead chip, and the Am2904 for shift multiplexers, status registers, and carry-in control. For the system enclosed within the dashed lines, there are four major switching paths whose values for various kinds of cycles are summarized below, and shown on the timing waveform.

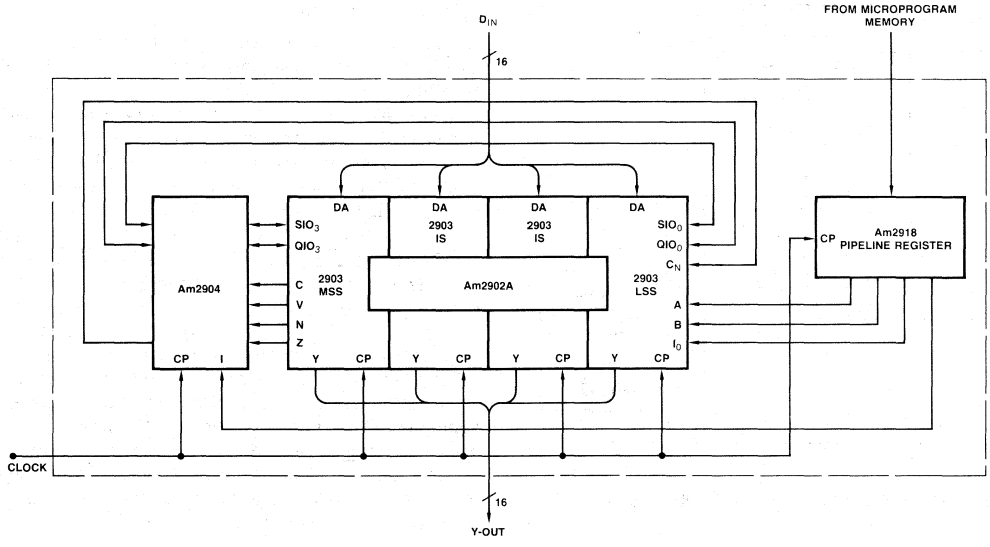
1. MICROCYCLE TIME (TCHCH).
   The minimum time which must elapse between a LOW-TO-HIGH clock transition and the next LOW-TO-HIGH clock transition.
2. DATA SET-UP TIME (TDVCH).
   The minimum time which must be allowed between valid, stable data on the D inputs and the clock LOW-TO-HIGH transition.
3. D TO Y (TDVYV).
   The maximum time required to obtain valid Y output data after the D inputs are valid. This is the combinational delay through the parts from D to Y.
4. CP TO Y (TCHYV).
   The maximum time required to obtain valid Y outputs after a clock LOW-TO-HIGH transition.

The types of cycles for which data is summarized are as follows:

1. Logic – Any logical operation without a shift.
2. Logic Rotate – Any logic operation with a rotate or shift.
3. Arithmetic – An add or subtract with no shift.
4. Multiply – The first cycle of a 2's complement multiply instruction. Subsequent cycles require less time.
5. Divide – The iterative divide cycle. The first divide instruction and the last divide (correction) instruction require less time.

Time in ns Over Commercial Operating Range

CYCLE	TCHCH	TDVCH	TDVYV	TCHYV
LOGIC	143	105	64	102
LOGIC ROTATE	180	143	123	160
ARITHMETIC	184	137	96	143
MULTIPLY	200	140	120	180
DIVIDE	228	167	128	189



16-Bit System with Am2903, Am2902A, Am2904

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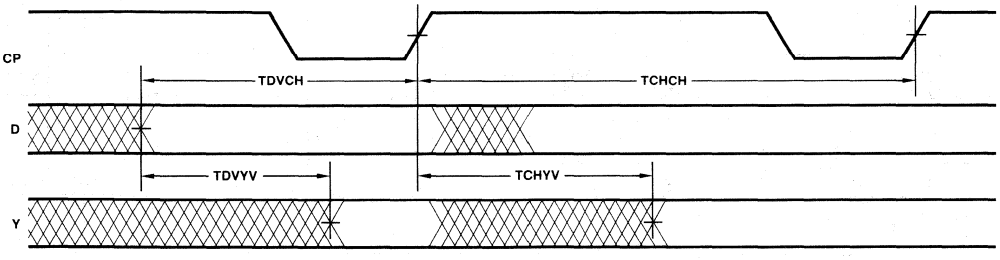

Timing Waveforms for Data In, Clock, and Y Out

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USING THE Am2903 AND Am29203

Except Where Otherwise Noted, All References to the Am2903 Also Apply to the Am29203.

Am2903 APPLICATIONS

The Am2903 is designed to be used in microprogrammed systems. Figure 1 illustrates a recommended architecture. The control and data inputs to the Am2903 normally will all come from registers clocked at the same time as the Am2903. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions which apply the proper control signals to the Am2903's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 Microprogram Sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially, these bits are the "next instruction" control.

One Level Pipeline Based System

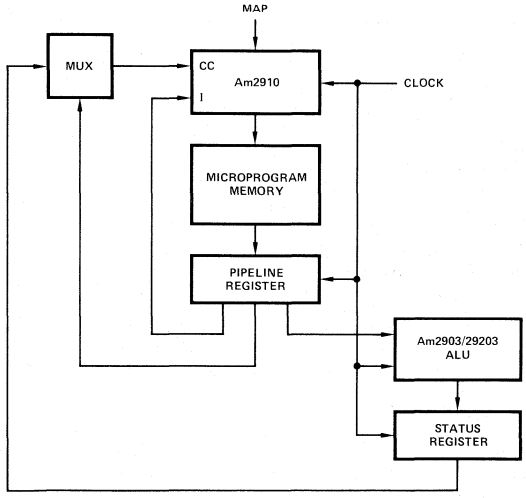

Figure 1. Typical Microprogram Architecture.

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Note that with the microprogram register in between the microprogram memory store and the Am2903's, a microinstruction accessed on one cycle is executed on the next cycle. As one microinstruction is executed, the next microinstruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2903's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

Expansion of the Am2903

The Am2903 is a four-bit CPU slice. Any number of Am2903's can be interconnected to form CPU's of 8, 16, 32, or more bits, in four-bit increments. Figure 2 illustrates the interconnection of four Am2903's to form a 16-bit CPU, using ripple carry.

With the exception of the carry interconnection, all expansion schemes are the same. The QIO_3 and SIO_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the QIO_0 and SIO_0 pins of the adjacent more significant device. These connections allow the Q Registers of all Am2903's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to a shift multiplexer which can be controlled by the microcode to select the appropriate input signals to the shift inputs.

Device 1 has been defined as the least significant slice (LSS) and its $\overline{LSS}$ pin has accordingly been grounded. The Write/Most Significant Slice ($\overline{WRITE}/\overline{MSS}$) pin of device 1 is now defined as being the Write output, which may now be used to drive the write enable ($\overline{WE}$) signal common to the four devices. Devices 2 and 3 are designated as intermediate slices and hence the $\overline{LSS}$ and $\overline{WRITE}/\overline{MSS}$ pins are tied HIGH. Caution: $\overline{W}/\overline{MSS}$ must be tied to V_{CC} through a resistor; $\overline{W}/\overline{MSS}$ and $\overline{LSS}$ may not be shorted directly together. Device 4 is designated the most significant slice ($\overline{MSS}$) with the $\overline{LSS}$ pin tied HIGH and the $\overline{WRITE}/\overline{MSS}$ pin held LOW. The open collector, bidirectional Z pins are tied together for detecting zero or for inter-chip communication for some special instruction. The Carry-Out (C_{n+4}) is connected to the Carry-In (C_n) of the next chip in the case of ripple carry. For a faster carry scheme, an Am2902 may be employed (as shown in Figure 3) such that the $\overline{G}$ and $\overline{P}$ outputs of the Am2903 are connected to the appropriate $\overline{G}$ and $\overline{P}$ inputs of the Am2902, while the C_{n+x}, C_{n+y}, and C_{n+z} outputs of the Am2902 are connected to the C_n input of the appropriate Am2903. Note that $\overline{G}$/N and $\overline{P}$/OVR pin functions are device dependent. The most significant slice outputs N and OVR while all other slices output $\overline{G}$ and $\overline{P}$.

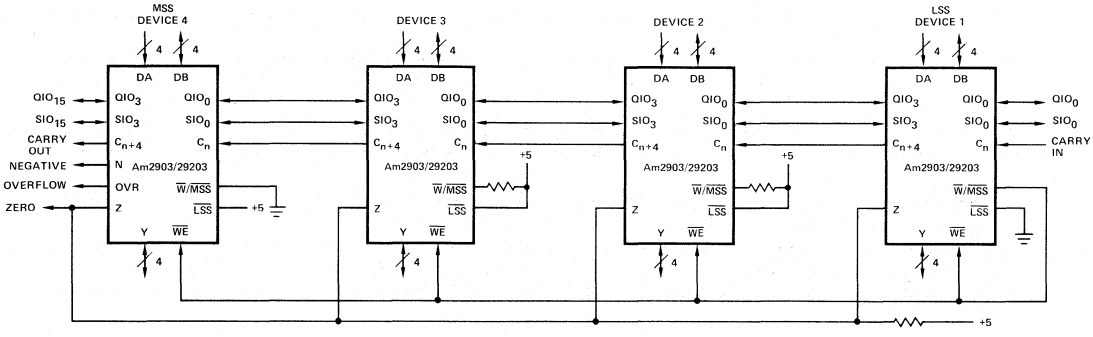

Figure 2. 16-Bit CPU with Ripple Carry.

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The $\overline{IEN}$ pin of the Am2903 allows the option of conditional instruction execution. If $\overline{IEN}$ is LOW, all internal clocking is enabled, allowing the latches, RAM, and Q Register to function. If $\overline{IEN}$ is HIGH, the RAM and Q Register are disabled. The RAM is controlled by $\overline{IEN}$ if $\overline{WE}$ is connected to the $\overline{WRITE}$ output.

It would be appropriate at this point to mention that the Am2903 may be microcoded to work in either two-or three-address architecture modes. The two-address modes allow A+B→B while the three-address mode makes possibleA+B→C. Implementation of a three-address architecture is made possible by varying the timing of $\overline{IEN}$ in relationship to the external clock and changing the B address as shown in Figure 4. This technique is discussed in more detail under Memory Expansion.

Parity

The Am2903 computes parity on a chosen word when the instruction bits I_{5-8} have the values of 4_{16} to 7_{16} as shown in Table 3. The computed parity is the result of the exclusive OR of the individual ALU outputs and SIO_3. Parity output is found on SIO_0. Parity between devices may be cascaded by the interconnection of the SIO_0 and SIO_3 ports of the devices as shown in Figure 3. The equation for the parity output at SIO_0 port of device 1 is given by $SIO_0 = F_{15} \forall F_{14} \forall F_{13} \forall \ldots \forall F_1 \forall F_0 \forall SIO_{15}$.

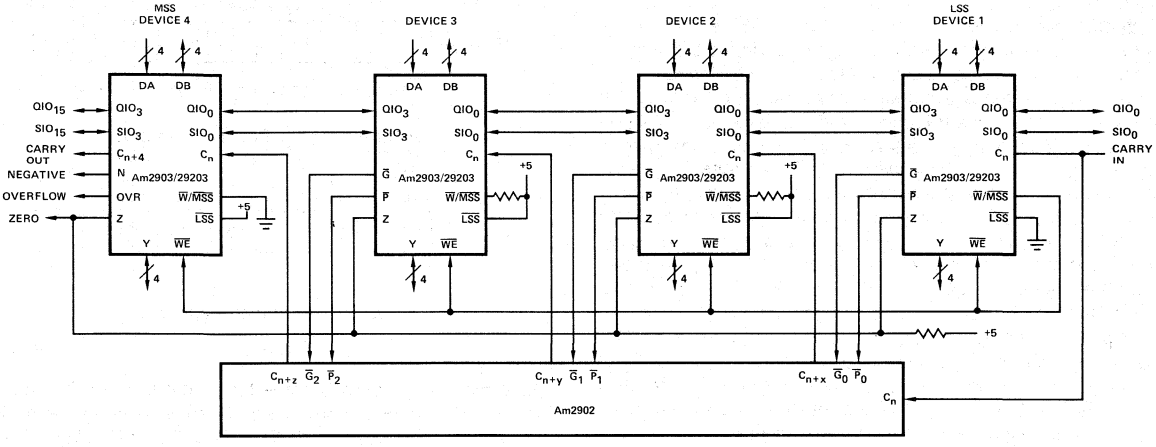


Figure 3. 16-Bit CPU with Carry Look Ahead.

MPR-037

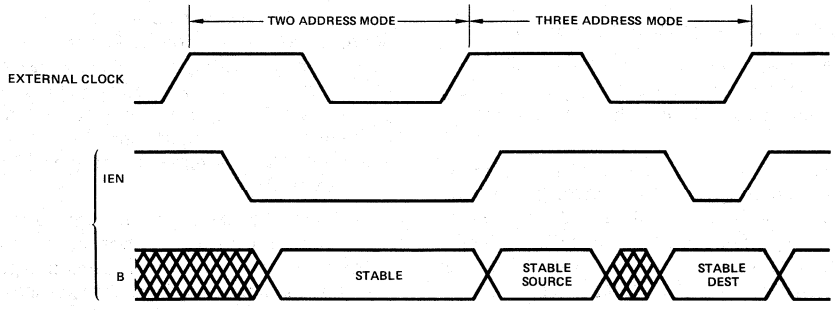


Figure 4. Relationship of $\overline{IEN}$ and Clock During Two Address and Three Address Modes.

MPR-038

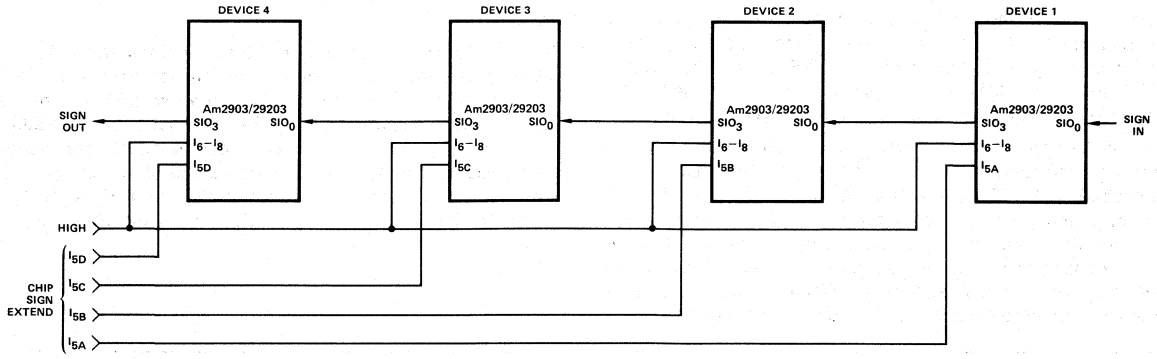


Figure 5. Sign Extend. MPR-039

Sign Extend

Sign extension across any number of Am2903 devices can be done in one microcycle. Referring again to the table of instructions (Table 3), the sign extend instruction (Hex instruction E) on I_{5-8} causes the sign present at the SIO_0 port of a device to be extended across the device and appear at the SIO_3 port and at the Y outputs. If the least significant bit of the instruction (bit I_5) is HIGH, Hex instruction F is present on I_{5-8}, commanding a shifter pass instruction. At this time, F_3 of the ALU is present on the SIO_3 output pin. It is then possible to control the extension of the sign across chip boundaries by controlling the state of I_5 when I_{6-8} are HIGH. Figure 5 outlines the Am2903 in sign extend mode. With I_{6-8} held HIGH, the individual chip sign extend is controlled by $I_{5A\text{-}D}$. If, for example, I_{5A} and I_{5B} are HIGH while I_{5C} and I_{5D} are LOW, the signal present at the boundaries of devices 2 and 3 (F_3 of device 2) will be extended across devices 3 and 4 at the SIO_3 pin of device 4. The output of the four devices will be available at their respective Y data ports. The next positive edge of the clock will load the Y outputs into the address selected by the B port. Hence, the results of the sign extension is stored in the RAM.

SPECIAL FUNCTIONS

When $I_{0-4} = 0$, the Am2903 is in the Special Function mode. In this mode, both the source and destination are controlled by I_{5-8}. The Special Functions are in essence special microinstructions that are used to reduce the number of microcycles needed to execute certain functions in the Am2903.

NORMALIZATION, SINGLE- AND DOUBLE-LENGTH

Normalization is used as a means of referencing a number to a fixed radix point. Normalization strips out all leading sign bits such that the two bits immediately adjacent to the radix point are of opposite polarity.

Normalization is commonly used in such operations as fixed-to-floating point conversion and division. The Am2903 provides for normalization by using the Single-Length and Double-Length Normalize commands. Figure 6a represents the Q Register of a 16-bit processor which contains a positive number. When the Single-Length Normalize command is applied, each positive edge of the clock will cause the bits to shift toward the most significant bit (bit 15) of the Q Register. Zeros are shifted in via the QIO_0 port. When the bits on either side of the radix point (bits 14 and 15) are of opposite value, the number is considered to be normalized as shown in Figure 6b. The event of normalization is externally indicated by a HIGH level on the C_{n+4} pin of the most significant slice (C_{n+4} MSS = Q_3 MSS $\forall$ Q_2 MSS).

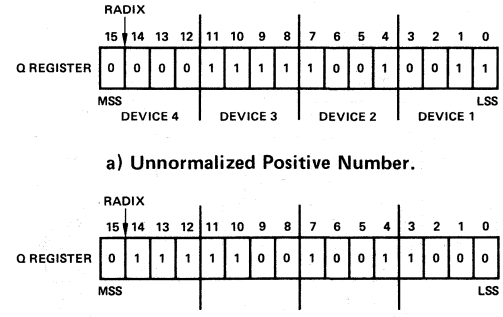
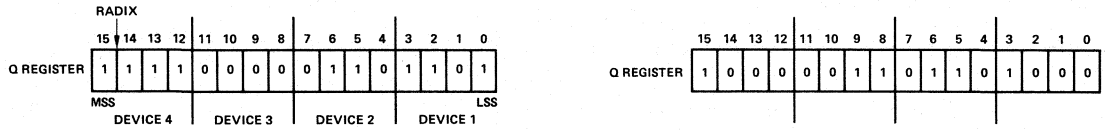


Figure 6. MPR-040

There are also provisions made for a normalization indication via the OVR pin one microcycle before the same indication is available on the C_{n+4} pin (OVR = Q_2 MSS $\forall$ Q_1 MSS). This is for use in applications that require a stage of register buffering of the normalization indication.

Since a number comprised of all zeros is not considered for normalization, the Am2903 indicates when such a condition arises. If the Q Register is zero and the Single-Length Normalization command is given, a HIGH level will be present on the Z line. The sign output, N, indicates the sign of the number stored in the Q register, Q_3 MSS. An unnormalized negative number (Figure 7a) is normalized in the same manner as a positive number. The results of single-length normalization are shown in Figure 7b. The device interconnection for single-length normalization is outlined in Figure 8. During single length normalization, the number of shifts performed to achieve normalization can be counted and stored in one of the working registers. This can be achieved by forcing a HIGH at the C_n input of the least significant slice, since during this special function the ALU performs the function [B] + C_n and the result is stored in B.

Normalizing a double-length word can be done with the Double-Length Normalize command which assumes that a user-selected RAM Register contains the most significant portion of the word to be normalized while the Q Register holds the least significant half (Figure 9). The device interconnection for double-length normalization is shown in Figure 10. The C_{n+4}, OVR, N, and Z outputs of the most significant slice perform the same functions in double-length normalization as they did in single-length normalization except that C_{n+4}, OVR, and N are derived from the output of the ALU of the most significant slice in the case of double-length normalization, instead of the Q Register of the most significant



a) Unnormalized Negative Single Length Number.

b) Normalized Negative Single Length Number.

Figure 7.

MPR-041

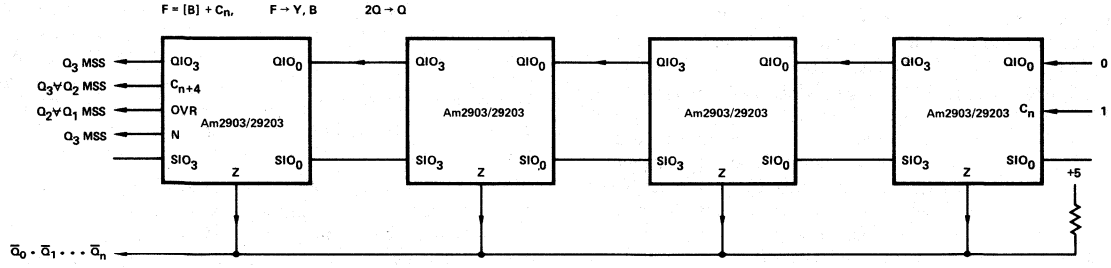


Figure 8. Single Length Normalize.

MPR-042

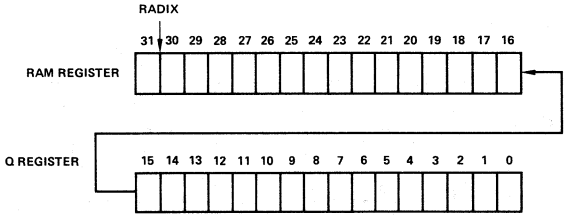


Figure 9. Double Length Word.

MPR-043

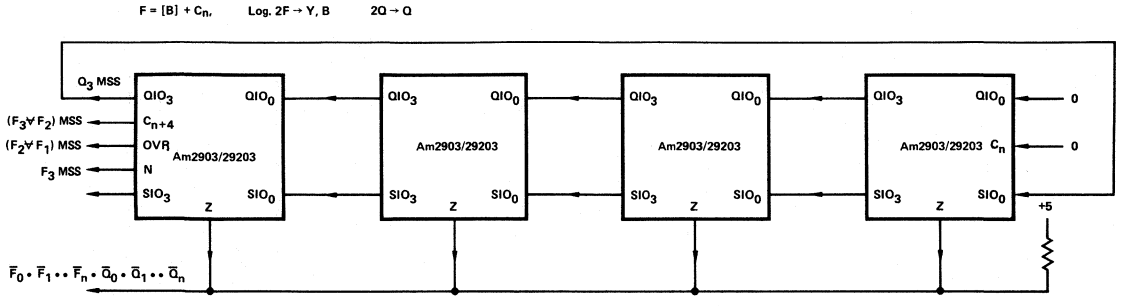


Figure 10. Double Length Normalize.

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slice as in single-length normalization. A high-level Z line in double-length normalization reveals that the outputs of the ALU and Q Register are both zero, hence indicating that the double-length word is zero.

When double-length normalization is being performed, shift counting is done either with an extra microcycle or with an external counter.

SIGN MAGNITUDE, TWO'S COMPLEMENT CONVERSION

As part of the special instruction set, the Am2903 can convert between two's complement and sign/magnitude representations. Figure 11 illustrates the interconnection needed for sign magnitude/two's complement conversion. The word to be converted is applied to the S input port of the ALU (from the RAM B port or the DB I/O port). The C_n input of device 1 is connected to the Z pin. The sign bit (S_3MSS) is brought out on the Z line and informs the other ALU's if the conversion is being performed on a negative or positive number. If the number to be converted is the most negative number in two's complement [i.e., 100 . . . 00 (-2^n)], an overflow indication will occur. This is because -2^n is one greater than any number that can be represented in sign magnitude notation and hence an attempted conversion to sign magnitude from -2^n will cause an overflow. When minus zero in sign magnitude notation (100 . . . 0) is converted to two's complement notation, the correct result is obtained (0 . . .0).

INCREMENT BY ONE OR TWO

Incrementation by One or Two is made possible by the Special Function of the same name. This command is quite useful in the case of byte addressable words. Referencing Figure 12, a word may be incremented by one if C_n is LOW or incremented by two if C_n is HIGH.

UNSIGNED MULTIPLY

This Special Function allows for easy implementation of unsigned multiplication. Figure 13 is the unsigned multiply flow chart. The algorithm requires that initially the RAM word addressed by Address port B be zero, that the multiplier be in the Q Register, and that the multiplicand be in the register addressed by Address port A. The initial conditions for the execution of the algorithm are that: 1) register R_0 be reset to zero; 2) the multiplicand be in R_1; and 3) the multiplier be in R_2. The first operation transfers the multiplier, R_2, to the Q Register. The Unsigned Multiply instruction is then executed 16 times. During the Unsigned Multiply instruction, R_0 is addressed by RAM address port B and the multiplicand is addressed by RAM address port A.

When the unsigned Multiply command is given, the Z pin of device 1 becomes an output while the Z pins of the remaining devices are specified as inputs as shown in Figure 15. The Z output of device 1 is the same state as the least significant bit of the multiplier in the Q Register. The Z output of device 1 informs the ALU's of all the slices, via their Z pins, to add the partial product (referenced by the B address port) to the mul-

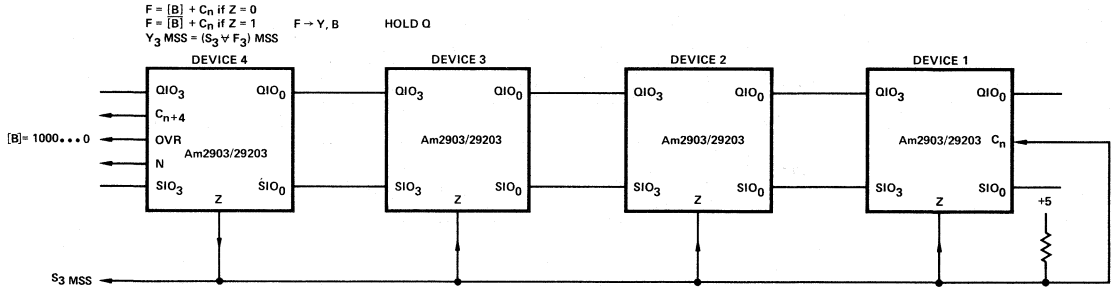


Figure 11. 2's Complement ⟷ Sign/Magnitude.

MPR-045

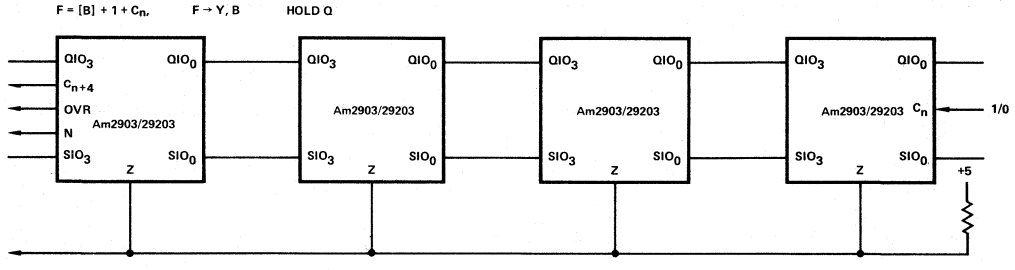


Figure 12. Increment by 2/1.

MPR-046

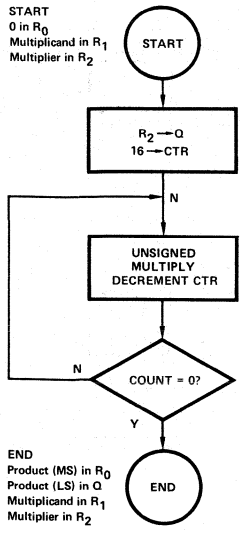


Figure 13. Unsigned 16 X 16 Multiply Flowchart.

tiplicand (referenced by the A address port) if Z = 1. If Z = 0, the output of the ALU is simply the partial product (referenced by the B address port). Since C_n is held LOW, it is not a factor in the computation. Each positive-going edge of the clock will internally shift the ALU outputs toward the least significant bit and simultaneously store the shifted results in the register selected by the B address port, thus becoming the new partial sum. During the down shifting process, the C_{n+4} generated in device 4 is internally shifted into the Y_3 position of device 4. At this time, one bit of the multiplier will down shift out of the QIO_0 ports of each device into the QIO_3 port of the next less significant slice. The partial product is shifted down between chips in a like manner, between the SIO_0 and SIO_3 ports, with SIO_0 of device 1 being connected to QIO_3 of device 4 for purposes of constructing a 32-bit long register to hold the 32-bit product. At the finish of the 16 x 16 multiply, the most significant 16 bits of the product will be found in the register referenced by the B address lines while the least significant 16 bits are stored in the Q Register. Using a typical Computer Control Unit (CCU), as shown in Figure 16, the unsigned multiply operation requires only two lines of microcode, as shown in Figure 17, and is executed in 17 microcycles.

TWO'S COMPLEMENT MULTIPLICATION

The algorithm for two's complement multiplication is illustrated by Figure 14. The initial conditions for two's complement multiplication are the same as for the unsigned multiply operation. The Two's Complement Multiply Command is applied for 15 clock cycles in the case of a 16 x 16 multiply. During the down shifting process the term N∀OVR generated in device 4 is internally shifted into the Y_3 position of device 4. The data flow shown in Figure 15 is still valid. After 15 cycles, the sign bit of the multiplier is present at the Z output of device 1. At this time, the user must place the Two's Complement Multiply Last cycle command on the instruction lines. The interconnection for this instruction is shown in Figure 18. On the next positive edge of the clock, the Am2903 will adjust the partial product, if the sign of the multiplier is negative, by subtracting out the two's complement representation of the multiplicand. If the sign bit is positive, the partial product is not adjusted. At this point, two's complement multiplication is completed. Using a typical CCU, as shown in Figure 16, the two's complement multiply operation requires only three lines of microcode, as shown in Figure 19, and is executed in 17 microcycles.

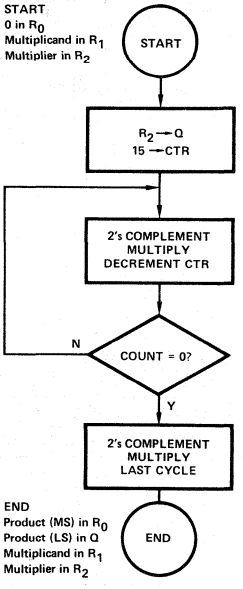
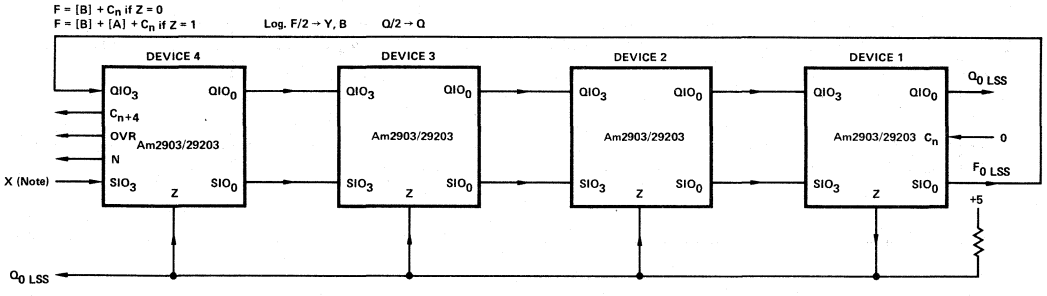


Figure 14. 2's Complement 16 X 16 Multiply.



Note: For unsigned multiply, C_{n+4} MSS is internally shifted into position Y_3 MSS; 2's complement multiply N∀OVR is internally shifted into position Y_3 MSS.

Figure 15. Multiply.

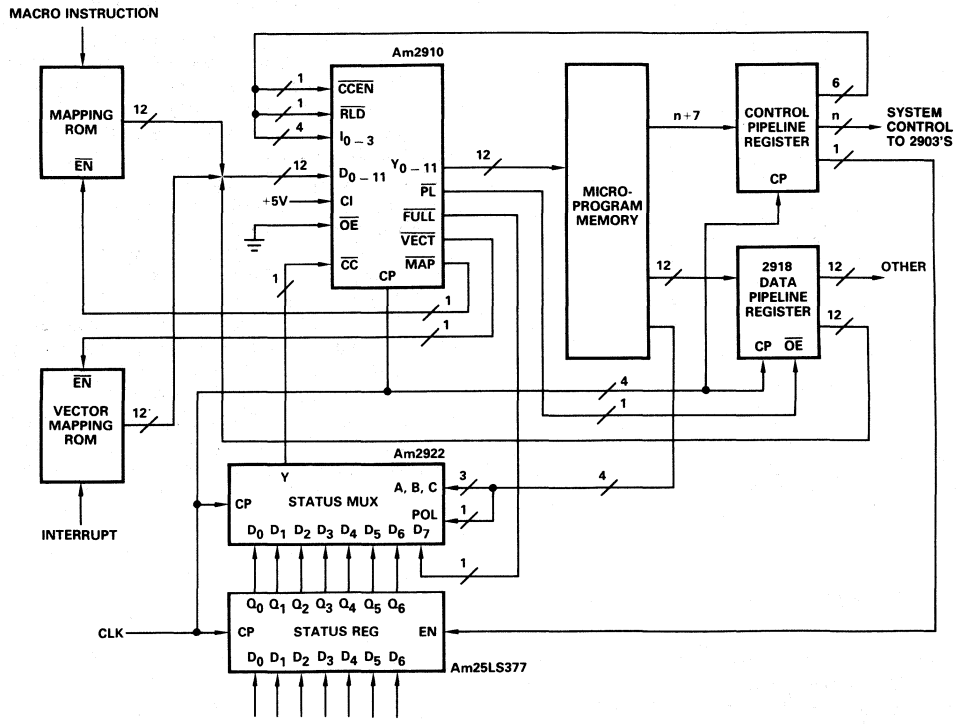


Figure 16. Typical Computer Control Unit (CCU).

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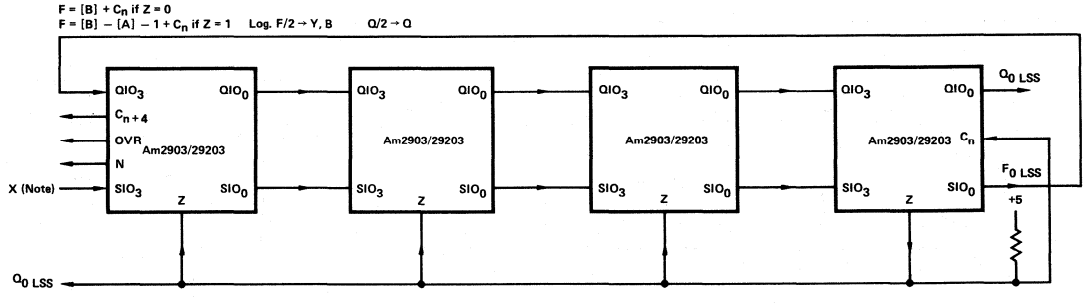
Micro Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	I_4-I_1	I_8-I_5	$\overline{OEB}$	$\overline{OEY}$	A_3-A_0	B_3-B_0	C_n	Comment
n	LDCT	$00F_{16}$	H	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	0	0	0	R_1	R_0	0	Unsigned Multiply

Figure 17. Micro Code for Unsigned 16 X 16 Multiply.



Note: N ∀ OVR is internally shifted into position Y_3 MSS.

Figure 18. 2's Complement Multiply, Last Cycle.

MPR-051

Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	$I_4 - I_1$	$I_8 - I_5$	$\overline{OEB}$	$\overline{OEY}$	$A_3 - A_0$	$B_3 - B_0$	C_n	Comment
n	LDCT	$00E_{16}$	X	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	2	0	0	R_1	R_0	0	2's Complement Multiply
n+2	X	X	0	0	6	0	0	R_1	R_0	Z	2's Complement Multiply (Last Cycle)

Figure 19. Microcode for 2's Complement 16 x 16 Multiply.

TWO'S COMPLEMENT DIVISION

Three instructions in the Am2903 perform a correct two's complement division, regardless of the sign of the divisor and the dividend. This type of division, also known as four-quadrant division, offers different preamble and postamble checks for fractional division and for integer division.

The general-purpose divide algorithm, shown in Fig. 20, applies to fractional division. For ease of explanation, assume a 16-bit divisor and a 32-bit dividend. The algorithm starts by checking whether the divisor is zero. If it is, division cannot be performed and the operation is aborted. If the divisor is not zero, the algorithm checks whether the dividend is zero, in which case both the quotient and remainder are zero and the division is complete.

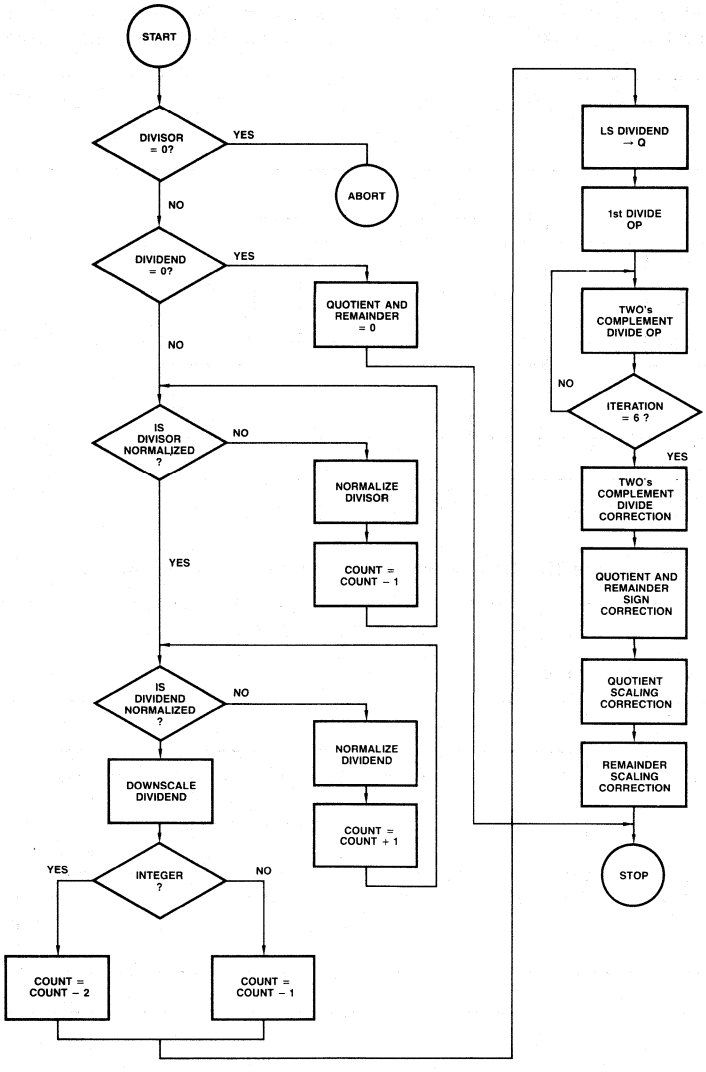


Figure 20. Division Flow Chart – Double Precision Divide.

In all other cases, the algorithm checks for divisor and dividend normalization. A binary number is deemed normalized when it is shifted up until the most significant bit is different from the immediately adjacent bit. Normalization has two main advantages. First, shifting out leading "sign" bits in the dividend lengthens the dividend and thus increases the accuracy of the final quotient and remainder. Counting the number of shifts gives an inverse multiplication factor that is later used to multiply the final quotient and remainder to obtain their true, scaled values.

Normalizing is also an effective way of lining up the most significant bit of the divisor with the most significant bit of the dividend; thereafter, it is easy to downshift the dividend arithmetically, making it less than the divisor. This step assures that the result is always representable as a fraction.

The normalization of the divisor begins after the Am2903 checks that it is not already normalized; the check takes only one microcycle. If the divisor is not normalized, a single-length normalization command is executed while a counter, initially set to zero, is decremented by one. Normalization is repeated – and rechecked – until the divisor is normalized. During each iteration, the counter is decremented to keep track of decreases in the dynamic range of the quotient and remainder.

The next step in the algorithm is the check for dividend normalization. Unless the dividend is already normalized, it has to undergo a double-length normalization. The counter is incremented by one, and another check for normalization follows. The counter increments to show that each normalization loop has increased the dynamic range of quotient and remainder. When the dividend is normalized, the algorithm proceeds.

At this point, the most significant bits of divisor and dividend are lined up. To ensure that the divisor is larger than the most significant portion of the dividend, the dividend is scaled down by down-shifting with sign fill and decrementing the counter.

After the least-significant portion of the dividend is placed in a general-purpose register, the algorithm uses one of the Am2903's divide commands, which determines the sign bit of the quotient. The road is now clear for the two's-complement-divide command, which yields a quotient bit each time it is executed – in the case of the 16-bit divisor and a 32-bit dividend, fourteen times. The interconnections between the slices for the divide operations are shown in Figures 21, 21b, 21c for a 16-bit system. The intermediate slices may be removed for systems of smaller widths.

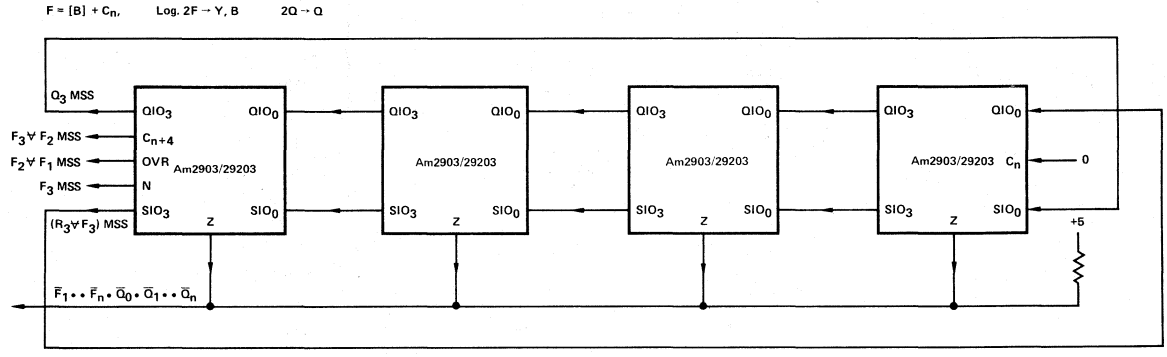


Figure 21a. Double Length Normalize/First Divide Operation MPR-053

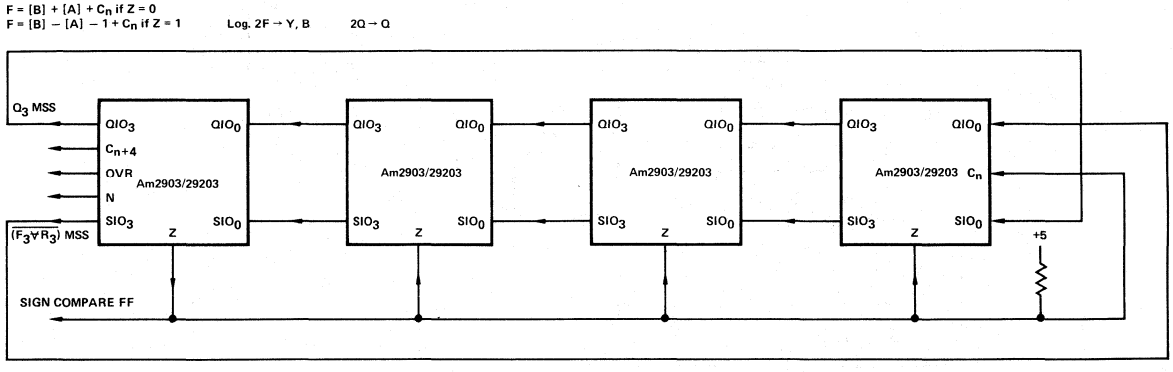


Figure 21b. 2's Complement Divide MPR-054

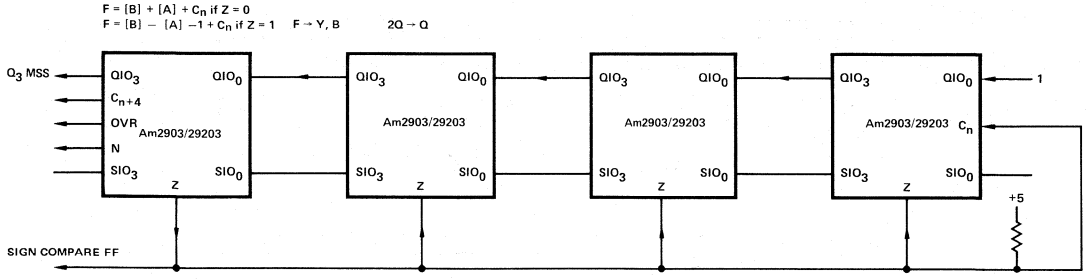


Figure 21c. 2's Complement Divide Correction

MPR-055

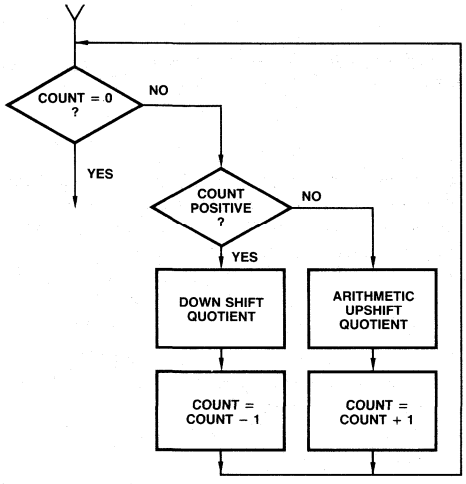


Figure 22. A counter keeps track of bit-shifting during normalization, then scales the quotient back to its proper value, again by shifting bits.

Repeated execution of the two's-complement-divide commands is followed by a single two's-complement-divide correction. This Am2903 instruction corrects the quotient automatically to assure that quotient times divisor plus the remainder equals the dividend.

Integer division uses the same general algorithm as fractional division, but a few modifications are necessary because integers and real numbers are represented differently (Figure 23a). In a fractional word, the most significant bit is the sign; the next bit is one-half (2^{-1}); the next is one-quarter (2^{-2}); and so on. The least significant (right-most) bit in the word is $2^{-(n-1)}$. For an integer, on the other hand, the left-most bit in a word is the sign, followed by the highest power of 2, namely 2^{n-1}, and following bits decrease toward the right-most bit in the word, which is 2^0.

With an n-bit dividend, the algorithm in Figure 20 takes into account all but the last bit of the dividend (Figure 23b). Since the algorithm works from left to right on the dividend, it can drop the last bit for a fractional divide. In most cases, the least-significant bit of a dividend is so small that its omission is of little or no consequence. However, if the least-significant bit of an integer is dropped, the algorithm treats the next-to-least-significant bit (with weighting of 2^1 as if it were the least-significant bit (representing 2^0). The algorithm therefore "reads" a word, which is equal in value to the original word, but shifted down one place – in effect,

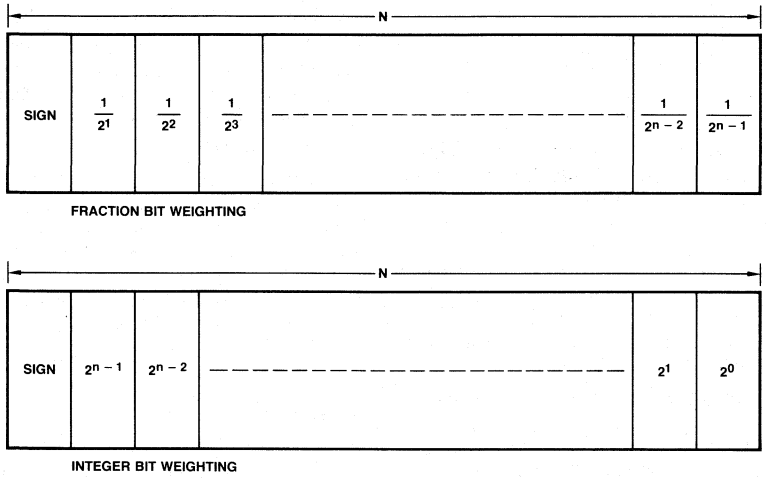


Figure 23a. Fractional (that is, real) numbers and integers are each represented differently in the computer. Since the described algorithm is designed for fractional division, corrective steps are needed with integers. The number N in this illustration is either 8 or 16.

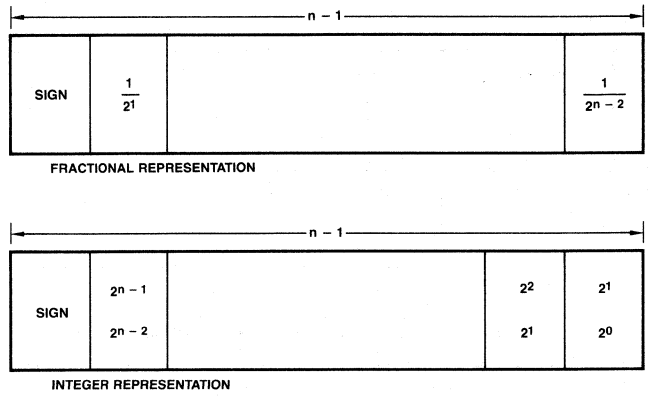


Figure 23b. The divide algorithm disregards the last bit of a fractional dividend. For integer division, however, the algorithm interprets each bit at only half its real value (highlighted). Without corrections, a wrong remainder results.

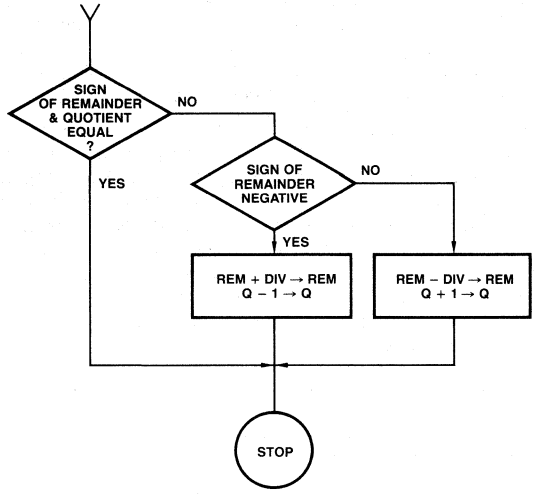


Figure 23c. For integer division, the sign (and value) of the remainder may not be correct (see Table 1). The shown algorithm makes the proper corrections.

divided by 2. To obtain the correct result for an integer divide using the Am2903's algorithm, the initial dividend must be shifted up one place. Or the divide operation could use an upshifted dividend and, as a final step, correct quotient and remainder by upshifting both one place.

Another deviation from the algorithm in Figure 20 immediately follows dividend normalization and downscaling. The algorithm requires that the most significant portion of the dividend be less than the divisor; integer-division requires that the dividend be upshifted one place before the first divide operation. To satisfy both conditions, the dividend is not physically shifted up in the integer divide; instead, the algorithm decrements the scaling count by two places to make it always less than the divisor.

While the divide algorithm in the Am2903 guarantees an algebraically correct answer, it does not guarantee that the sign of the remainder is the same as the sign of the dividend. If a user wants the signs to be equal, he must check the condition and apply a correction factor. Table A outlines the steps to correct remainder and quotient if the signs of the dividend and the remainder are different; Figure 23c is a flow chart of the procedure.

For an integer divide, the quotient-scaling routine in Figure 22 is expanded so that the same operations are applied to the remainder as to the quotient. The remainder of an integer division may be used for further operations. In fractional-division, however, the remainder is usually discarded.

The algorithm for this step is shown in Figure 22. It begins by examining the count obtained in the normalization and performing the required downscaling operations. If the count is neither zero nor positive, then the quotient must be arithmetically upshifted to compensate for the normalization of the divisor. Arithmetic upshifting is another of the Am2903's special commands. It causes all data to be shifted around the sign bit. The procedure is repeated until the count register shows zero.

If, at the initial check, the count register is found to be positive instead of negative, the quotient receives a downshift with sign fill. After the down-shifting of the quotient, the count register is decremented by one, and the process is repeated until the count register shows zero.

A microprogrammed implementation of the integer-divide algorithm consists of two Am2903 slices, forming an 8-bit wide system. The Am2903s are controlled by an Am2910 microprogram sequencer via an Am29775 PROM. An Am2904 (status and shift control unit) takes care of the interconnection between the most significant slice (MSS) and the least significant slice (LSS), and also handles the status of the Am2909 array.

AN EXAMPLE

For the following example, the divisor is 8 bits and the dividend is 16 bits. Assume that the division is already in the Q-register of the Am2903 and that two of the 16 RAM registers, R_B and R_T, contain the most and the least significant bits of the dividend. A copy of the most significant half of the dividend is in register R_D. Register R_M contains a mask constant with the value 80H. The microcode

TABLE A. INTEGER REMAINDER AND QUOTIENT CORRECTION

Positive dividend Negative remainder	10 ÷ 4 = 3 REM = −2	Positive dividend Positive remainder	10 ÷ 3 = 3 REM = 1
Remiander + divisor → Quotient − 1→	Remainder →2 Quotient →2	OK	
Negative dividend Negative remainder	−13 ÷ 6 = −2 REM = −1	Negative dividend Positive remainder	−3 ÷ 5 = −1 REM = 2
OK		Remainder − divisor→ Quotient + 1→	Remainder → −3 Quotient → 0

for integer division consists of the four fields in Table B. These fields show the next instruction for the Am2910; the contents of the pipeline register data field, which is used for jump addresses and loop counter data; the function that the Am2903 is performing; and the function that the Am2904 is performing.

The mnemonics for the Am2910 are as follows: CONT means continue to next instruction; CJP means jump to address contained in pipeline register data field if the CC input to the sequencer is LOW, else continue to the next instruction; PUSH indicates that a loop in the microprogram starts at the next address, to be executed the number of times given by the value in the pipeline field. RFCT is used with the PUSH command as a loop terminator to indicate that the next address coming from the sequencer will be the one at the top of the loop.

The ABORT address in the pipeline field refers to user-defined code. STOP indicates the end of the algorithm. In the Am2904 function field, STORE STATUS shows that the status bits of the Am2903 are to be stored in the machine status register M. The status bits can be tested individually at the CT output of the Am2904.

HOLD STATUS means that the status register is not allowed to change on the current microcycle. The function LINK R_B WITH Q allows the two registers to be connected as a double-length register. LINK R_B, LINK Q connects each register to itself to form a ring shifter.

In the Am2903 function field, the SL NORM* indicates that a single-length normalization is being executed but the results are not stored; SL NORM stores the results. For double-length normalization, SL is replaced by DL.

The complete procedure becomes readily apparent in the steps of a simple division, for instance, 2046 divided by 32. The microcode will normally start at an arbitrary location n. However, this example uses relative address, starting at 0 and corresponding to the steps in Table B. The initial register contents are as follows:

Divisor in Q = 00100000
Most significant half of dividend in R_B = 00001000
Least significant half of dividend in R_T = 00000000
Copy of R_B in R_D = 00001000
R_m = 10000000.

Execution of the integer division then proceeds according to the microcode instructions:

(0): A nonzero indication is stored in register M_Z of the Am2904 since the divisor is not zero.
(1): The nonzero indication in M_Z is tested in the 2910 and is true; there is no ABORT. A nonzero indication for the most significant half of the dividend is stored in register M_Z.
(2): Since the most significant half of the dividend is nonzero jump to (6).
(6): A normalization command is executed on the divisor in Q; no results are stored. The normalization indication of the MSS is stored in M_C of the 2904.
(7): The normalization counter R_X is set to zero.
(8): The divisor goes through a normalization step and is found to be normalized. The normalization count in R_X is decremented by one, to −1. Execution jumps to (12).
(12). The normalized divisor is placed in R_A of the Am2903. R_A now contains 01000000.
(13): The least significant half of the dividend is placed in Q, which now contains 00000000.
(14): Double-length normalize command is in the Am2903 with no results being stored. Normalization indication is stored in M_C of the Am2904. Word-equal-zero is stored in M_Z of the Am2904.
(15): The dividend is checked for zero.
(16): The dividend is checked to see if it is already normalized.
(17): The dividend is shifted up and checked for normalization. Its value is now 00010000 00000000.
(18): Since the dividend was found not to be normalized on the last step, it is placed in the normalization loop, where it is again shifted up. The normalization indicated on the previous step is tested and found not to have occurred. The dividend is now 00100000 00000000.
(19): The normalization counter is incremented by one so that it now contains zero. A jump to the top of the loop at (18) is performed. After two more iterations, the dividend is 10000000 00000000. The count in R_X is 1. Execution is again at address (18) and the indication that normalization has been achieved causes a jump to (20).
(20): Since the dividend has been overshifted by one place while in the normalization loop, it must shift down with sign-in.
(21): The normalization counter R_X is incremented by one so that it now contains 2.
(22): The dividend is downshifted by one so that the most significant portion is less than the divisor. The dividend is now 00100000 00000000.
(23): The normalization counter is decremented by 2 (adjustment for an integer divide.) R_X now contains 0.
(24): The sign of the quotient is found to be 0.
(25): The program executes six iterations of two's complement divide. During execution, the lower half of the divided is shifted out of Q and the quotient bits are shifted in. The quotient at the end of six iterations is 00100000.
(26): The correction-cycle instruction is applied to the Am2903; the quotient in Q is now 01000001 and the remainder in R_B is 11000000.
(27): The indication that the normalization count is zero is stored in M_Z of the Am2904.
(28): Proceed to sign correction
(34): Mask the sign of the dividend in R_D and place the results in R_D, which now contains 00000000.
(35): Mask the sign of the remainder of R_B and place the results in R_T. The content of R_T is now 10000000.

(36): Compare R_D and R_T. The nonzero indication found at the Z-pin of the Am2903 is stored in M_Z of the Am2904.

(37): Find the sign of the remainder again and store it in M_Z of the Am2904.

(38): Since the remainer is found to be negative when M_Z is tested, jump to (41).

(41): Add remainder to normalized divisor and get a new remainder: 11000000 plus 01000000 gives 00000000 as the new contents of the remainder in R_B.

(42): Decrement the quotient by one, which makes it 01000000, or 64 in decimal notation. The division of 2048 by 32 is now complete.

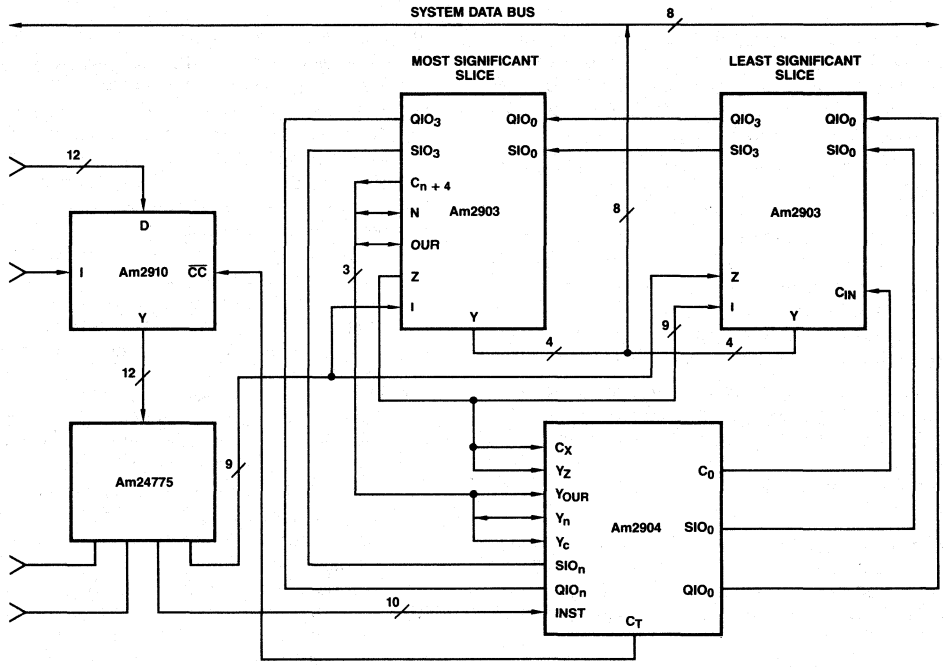


Figure 24. The complete divider consists of two Am2903 4-bit slices, controlled by an Am2904 microprogram sequencer, in cooperation with the Am24775 PROM containing the microcode. An Am2910 keeps track of the most and least significant bytes of the dividend.

TABLE B. CODE GENERATED FOR A SAMPLE DIVISION

Relative Micro-Program Address	Am2910 Instruction	Pipeline Register Data	Am2903 Function	Am2904 Function	Comments
0*	CONT	X	$[Q] \rightarrow$ Y Bus	Store status	Check if the divisor is zero
1	CJP	Abort	$[R_B] \rightarrow$ Y Bus	Store status, $M_Z \rightarrow C_T$	Abort if divisor is zero
2	CJP	6	$[R_T] \rightarrow$ Y Bus	Store status, $M_Z \rightarrow C_T$	If MSH dividend not zero then skip 2
3	CJP	6	PASS	Store status, $\overline{M}_Z \rightarrow C_T$	If LSH dividend not zero then skip 2
4	CONT	X	$0 \rightarrow [Q]$	Hold status	Set quotient to zero
5	CJP	STOP	$0 \rightarrow [R_B]$	Hold status, $Z \rightarrow C_T$	Set remainder to zero and stop
6	CONT	X	SL NORM*	Store status, Link Q-reg.	Begin divisor normalization checks
7	CJP	12	$0 \rightarrow [R_X]$	$M_C \rightarrow C_T$, Hold status	Initialize normalization count reg; end norm procedure if divisor is normalized
8	CJP	12	SL NORM, $[R_X] - 1 \rightarrow [R_X]$	$M_{OUR} \rightarrow C_T$, Store status	If normalized after first shift, end procedure
9	CJP	9	SL NORM, $[R_X] - 1 \rightarrow [R_X]$	$M_{OUR} \rightarrow C_T$, Store status	Loop until normalized
10	CONT	X	$[Q/2] \rightarrow [Q]$	$M \rightarrow QIO_n$, Hold status	"Denormalize" divisor
11	CONT	X	$[R_X] + 1 \rightarrow [R_X]$	Store status	"Denormalize" divisor
12	CONT	X	$[Q] \rightarrow [R_A]$	Store status	Return normalized divisor to R_A
13	CONT	X	$[R_T] \rightarrow [Q]$	Store status	Place lower half of dividend in Q for normalization
14	CONT	X	DL NORM*	Store status	Begin dividend normalization checks
15	CJP	4	PASS	$M_Z \rightarrow C_T$, Hold status	If dividend is zero, end normalization
16	CJP	22	PASS	$\overline{M}_C \rightarrow C_T$, Hold status	Check for normalization
17	CJP	21	DL NORM	$M_{OUR} \rightarrow C_T$, Store status	Begin normalization
18	CJP	20	DL NORM	$\overline{M}_{OUR} \rightarrow C_T$, Store status	Start normalize loop
19	CJP	18	$[R_X] + 1 \rightarrow [R_X]$	$0 \rightarrow C_T$, Hold status	Increment normalization shift count
20	CONT	X	$R_BQ/2 \rightarrow R_BQ$	$M_n \rightarrow SIO_n$, Store status	"Denormalize" dividend
21	CONT	X	$[R_X] + 1 \rightarrow [RX]$	Store status	Increment normalization shift count
22	CONT	X	$R_BQ/2 \rightarrow R_BQ$	Store status	Make dividend less than divisor
23	CONT	X	$[R_X] - 2 \rightarrow [R_X]$	Store status	Adjust normalization count for integer divide
24	PUSH	#6	1st Divide OP	Link R_B with Q, $Q \rightarrow C_O$	Find sign of quotient
25	RFCT	X	2's Complement Divide	Link R_B with Q, $C_X \rightarrow C_O$	Calculate quotient bits
26	CONT	X	2's Complement Divide Corr.	Store status, $C_X \rightarrow C_O$	Divide correction
27	CONT	X	$[R_X] \rightarrow$ Y Bus	Store status	Check if normalization count is 0
28	CJP	34	$[R_M] \bullet [R_X] \rightarrow$ Y Bus	$\overline{M}_Z \rightarrow C_T$, Store status	Check sign of count with mask; if count is zero, proceed to sign correction code
29	CJP	32	PASS	$\overline{M}_Z \rightarrow C_T$ Store status	If sign of count is negative, skip 2 lines
30	CONT	X	$R_B/2 \rightarrow R_B$, $Q/2 \rightarrow Q$	Link F, Link Q, Store status	Down-shift quotient and remainder
31	CJP	27	$[R_X] - 1 \rightarrow R_X$	$0 \rightarrow C_T$, Store status	Decrement, shift, count and jump top of loop
32	CONT	X	$2R_B \rightarrow R_B$, $2Q \rightarrow Q$	Link R_B, Link Q, Store status	Up-shift quotient and remainder
33	CJP	27	$[R_X] + 1 \rightarrow R_X$	$0 \rightarrow C_T$, Store status	Increment shift count and jump to top of loop
34	CONT	X	$[R_A] \bullet [R_D] \rightarrow R_D$	Store status	Begin sign correction code, find sign of dividend
35	CONT	X	$[R_M] \bullet [R_B] \rightarrow R_T$	Store status	Find sign of remainder
36	CONT	X	$[R_{T1}] + [R_D] \rightarrow Y$	Store status	Compare sign of dividend and remainder
37	CJP	STOP	$[R_M]\ [R_B] \rightarrow Y$	$M_Z \rightarrow C_T$, Store status	If signs compare then finished; check sign of remainder
38	CJP	41	PASS	$\overline{M}_Z \rightarrow C_T$, Store status	If remainder is negative, skip 2 lines
39	CONT	X	$R_B - R_A \rightarrow R_B$	Store status	Find new remainder
40	CJP	STOP	$[Q] + 1 \rightarrow [Q]$	$0 \rightarrow C_T$, Store status	Find new quotient; jump to exit
41	CONT	X	$R_B + R_A \rightarrow R_B$	Store status	Find new remainder
42	CONT	X	$[Q] - 1 \rightarrow [Q]$	Store status	Find new quotient
STOP					

*Initially: Divisor in Q. MSH Dividend in R_0. LSH Dividend in R_1.

TRIPLE PRECISION DIVIDE

It is possible to do multiple-precision divide operations beyond the double precision divide shown above. For example, to do a triple precision divide for a 16-bit CPU, the upper two thirds of the dividend are stored in R_1 and Q as in the case for double precision divide. The lower third of the dividend is stored in a scratch register, R_5. After checking that the magnitude of the divisor is greater than the magnitude of the dividend, using the same tests as defined in Figure 20, the procedure is as follows:

1. Execute a Double Length Normalize/First Divide Operation instruction.
2. Execute the Two's Complement Divide instruction fifteen times.
3. Transfer the contents of Q, the most significant half of the quotient, to R_2.
4. Transfer R_5 to Q.
5. Execute the Two's Complement Divide instruction fifteen times.
6. Execute the Two's Complement Divide Correction and Remainder instruction.

The upper half of the quotient is then in R_2, the lower half of the quotient is in Q and the remainder is in R_1. The flow chart for this is shown in Figure 25. This technique can be expanded for any precision which is required.

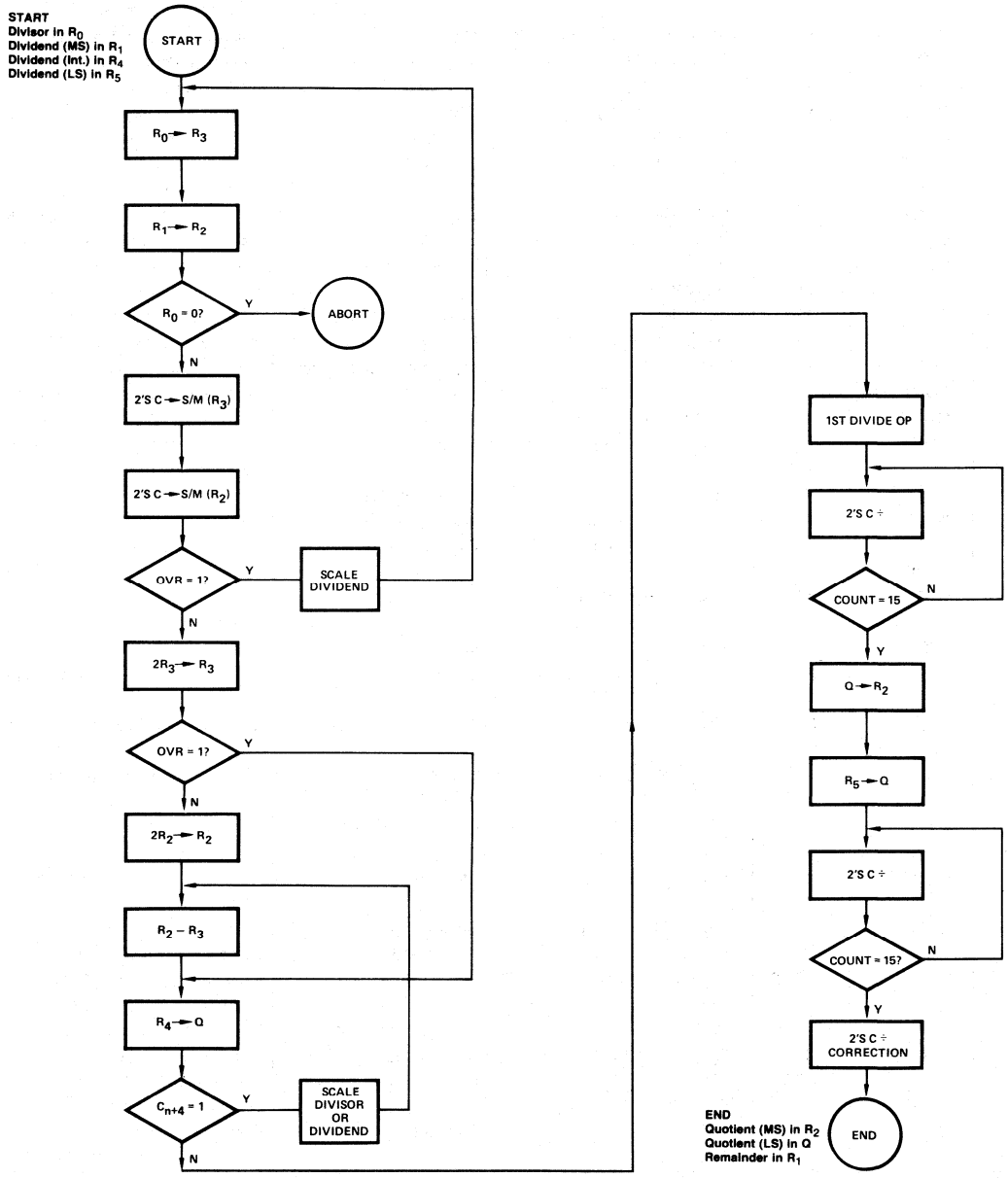


Figure 25. Division Flow Chart – Triple Precision Divide. MPR-056

BYTE SWAP

The multi-port architecture of the Am2903 allows for easy implementation of high- and low-order byte swapping. Figure 26 outlines a byte swap implementation utilizing two data ports. Initially, the lower order 8-bit byte is stored in devices 1 and 2, while the high-order byte is in devices 3 and 4. When the user wishes to exchange the two bytes, the register location of the desired word is placed on the B address port. When the byte swap line is brought LOW, the bytes to be swapped will be flowing from the DB ports of the Am2903 through the Am2958/2959 Three-state Buffers. The outputs of the three-state buffers are permuted such that the byte swap is achieved. The resultant permuted data is presented to the DA ports of the Am2903 where it is re-loaded into the memories of the Am2903 on the next positive edge of CP using the source and function commands of F = A plus C_n (C_n = 0) for the Am2958 or F = A plus C_n (C_n = 0) for the Am2959 and the destination command F Y, B.

A higher speed technique for achieving the byte swap operation is illustrated in Figure 27. Instead of inputting the permuted data via the DA ports, the permuted data is entered via the Y input/output ports with $\overline{OE}_Y$ held HIGH. This technique bypasses the ALU, thus allowing faster operation. The Am2903 destination command F → Y, B should be used.

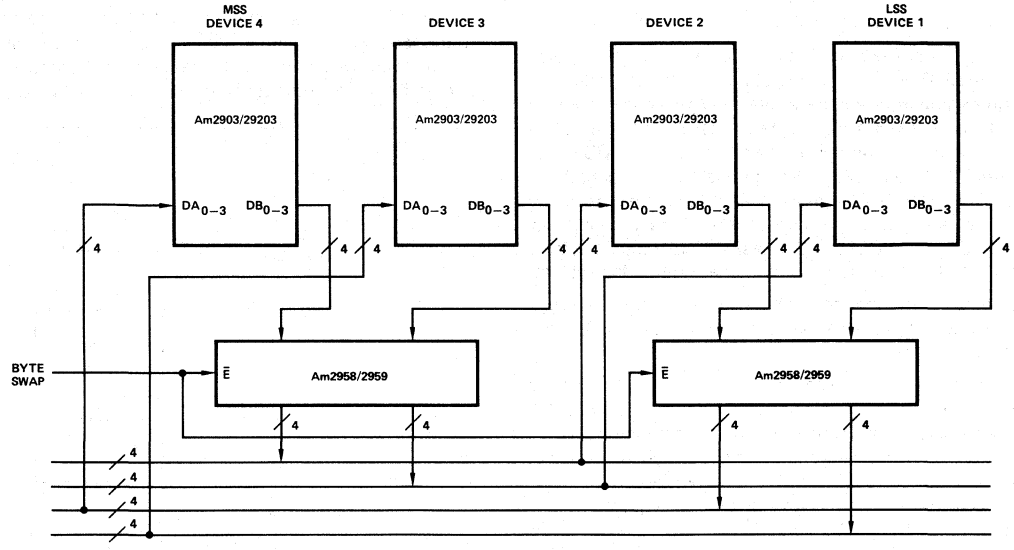


Figure 26. Byte Swap. MPR-057

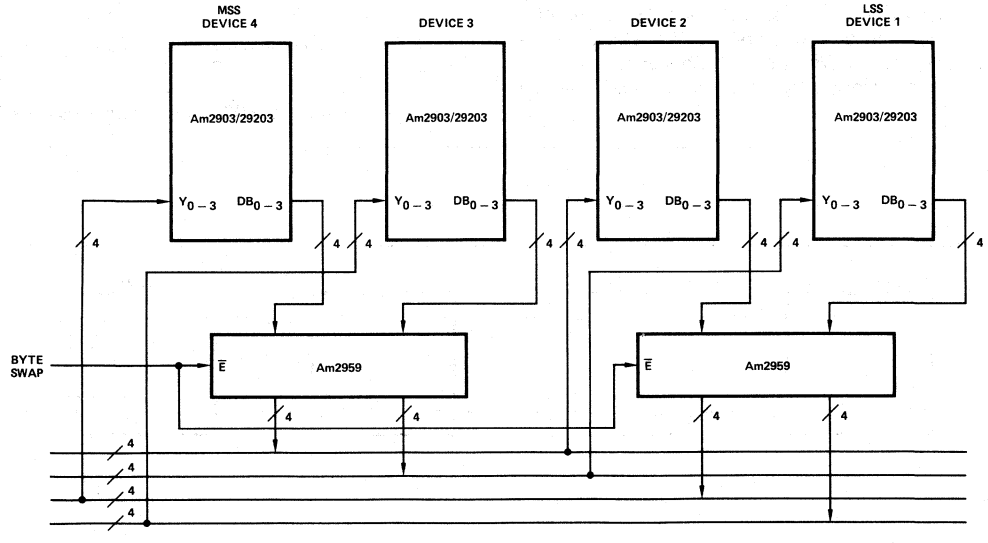


Figure 27. High Speed Byte Swap. MPR-058

BCD OPERATIONS WITH THE Am29203

BCD FUNCTIONS

Binary Coded Decimal (BCD) numbers are a means to represent decimal numbers in binary form such that each digit is represented by four bits of its equivalent binary value. They are useful in applications where there is a considerable amount of interaction with the decimal number representation. The value of the four binary bits corresponding to each BCD digit does not exceed nine.

As part of the special instruction set, the Am29203 can convert numbers between binary and BCD representations. It also performs basic arithmetic operations on BCD numbers.

BINARY TO BCD CONVERSION

This instruction, when executed several times, allows conversion from binary to BCD numbers. Using the same number of bits, the binary representation of numbers has a larger range of values than a BCD representation. Hence, care must be taken to see that the value of the binary number does not exceed the BCD range before using this instruction. Multiprecision representations where the width of the BCD number is larger than the width of the system, allows a larger range on numbers. The binary number may be stored as multiprecision as well. Usually multiprecision representations are integer multiples of the width of the system.

Figure 28 shows a flow chart for a single precision conversion in a 16-bit wide system. It involves executing the Binary to BCD conversion instruction 16 times.

In case of single-precision, this instruction requires that the binary number be present in the Q register and uses one of the RAM registers for storing the BCD number during and after the conversion. The RAM register is cleared before use. Each instruction is composed of two steps. The first step adds a binary value of three to each BCD digit which is five or greater as a preadjustment for a shift which follows. This addition is performed independently over each slice and the carry bits from each slice are ignored. The second step shifts up the Q register and the RAM register with the interconnections as in Figure 29, for a 16-bit system. The Am29203 executes both the steps in one microcycle. The number of shifts have to be a multiple of four to obtain a meaningful result.

The Am29203 also has another special instruction to facilitate multiprecision Binary to BCD conversions. This instruction referred to as "Multiprecision Binary to BCD Conversion" does the same action as the "Binary to BCD Conversion" except for the shifting of the Q register.

The flow chart for the simplest double precision Binary to BCD conversion algorithm in a 16-bit system is shown in Figure 30. Initially the Q register stores the most significant half of the binary number. Two registers R0 and R1, which are both cleared initially, are used for storing the most significant and least significant half of the BCD number after conversion respectively. The shift for each binary bit requires two microcycles. The Binary to BCD conversion instruction is executed first of R1 and the most significant bit from R1 that is shifted out is stored as the Mc or carry bit of the Am2904. The shift linkages for this step are shown in Figure 31. Next the Multiprecision Binary to BCD conversion instruction is executed so that R0 is also adjusted and the Mc or carry bit is shifted in. These two instructions together account for one equivalent shift of the double precision number as a whole. After 16 such shifts, the Q register is loaded with the least significant half of the binary number and the same operations are performed again 16 times. Once the single precision binary number is converted to a double precision BCD number, then the algorithm can be terminated after 16 shifts of the binary number.

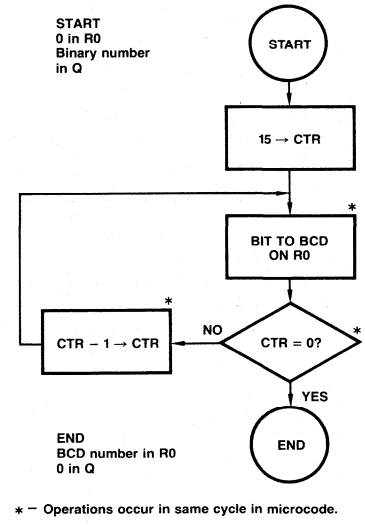


Figure 28. Binary to BCD Conversion – Single Precision

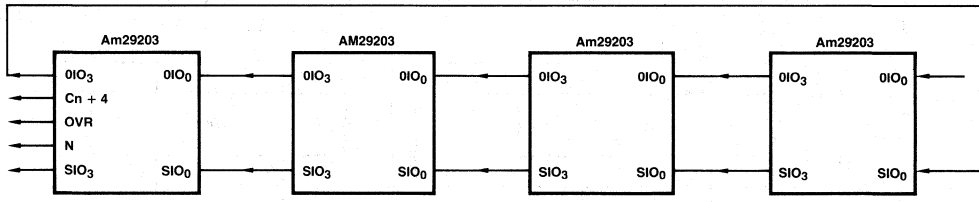
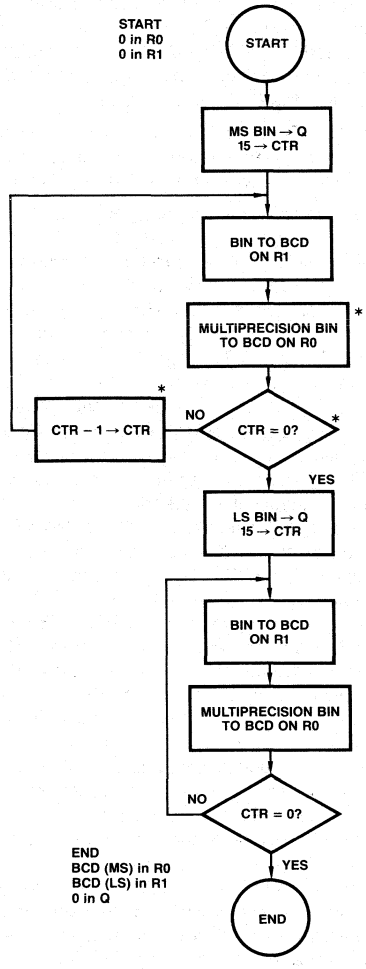


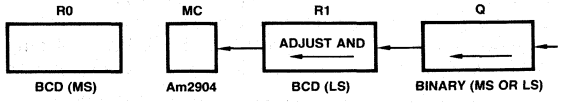
Figure 29. Binary to BCD Conversion



* – Operations occur in same cycle in microcode.

Figure 30. Double Precision 16-Bit Binary to BCD Conversion

a) Binary to BCD on R1



b) Multiprecision Binary to BCD on R0

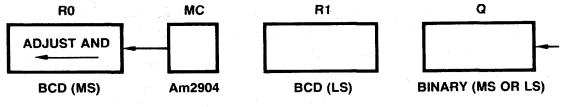
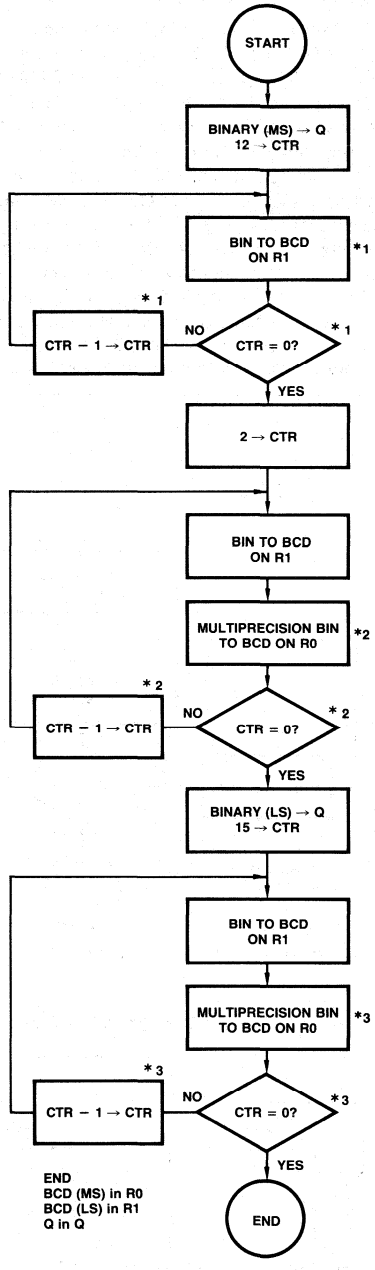


Figure 31. Shift Linkages During Double Precision Binary to BCD Conversion

The above algorithm can be made more efficient by noting that the shifting of R0 is not necessary for the first few cycles.

This is because mostly zeros are shifted into the already cleared register for the most part of the first 16 shifts of the double precision number. The flow chart for implementing this on double precision representations in a 16-bit system is shown in Figure 32. The most significant half of the binary number is first loaded in the Q register. For the first 13 cycles it is sufficient to shift only the



* – Operations occur in same cycle in microcode.

Figure 32. 16-Bit Double Precision Binary to BCD Conversion

6

R1 register during conversion. After this both R0 and R1 have to be shifted as cascaded registers. This is because the value of the largest unsigned 16-bit binary number is 65535 and thus requires 19 bits for representing in BCD. As a result, a non-zero bit may be shifted out of R1 after 13 shifts and it is necessary to start shifting R0 as well after this. After the first 16 shifts on the Q register, the least significant binary number is loaded in Q and 16 more double precision shifts are done. The shift-linkages while shifting R0 and R1 are same as the previous case and are shown in Figure 31.

BCD TO BINARY CONVERSIONS

The BCD to Binary conversion instruction essentially reverses the steps of the Binary to BCD instruction described earlier. The BCD number is initially present in one of the RAM registers and the Q register is used during the conversion to store the binary equivalent. The BCD to Binary conversion algorithm requires that the BCD number first be shifted one bit down and then an adjustment done on the BCD digits, which subtracts three from each BCD digit which is eight or greater. However, since the Am29203 has its shifter after the ALU section, the BCD to Binary conversion instruction first performs the adjustment for a previous shift and then performs the shift in preparation for the next instruction. A flow chart for this conversion is shown in Figure 33. The BCD number in R0 is first shifted down one bit to load its least significant bit into the most significant bit of the Q register. After this, the BCD to Binary conversion instruction is executed 15 times to perform the necessary adjustments and shifts successively. The interconnections are shown in Figure 34. Thus, 16 shifts and 15 adjustments are performed on the 16-bit number. The adjustment on the final shift is not required as the binary number is fully formed anyway and the BCD number is zero at this stage.

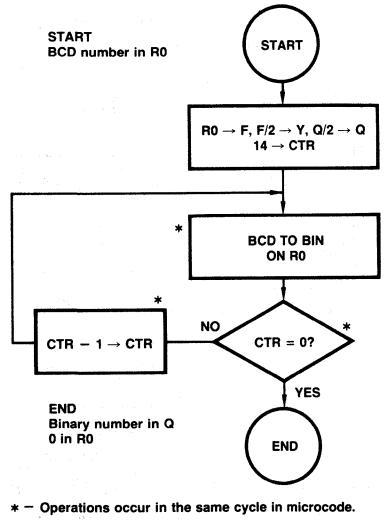


Figure 33. BCD to Binary Conversion – Single Precision

As in the case of the Binary to BCD conversion instruction, it may be noted that the adjustment is done independently over each slice and the carry bits play no role in this adjustment.

The scheme for converting multiprecision BCD numbers to binary is similar to the one outlined in the Binary to BCD conversion section. The simplest, but not the most efficient scheme, uses the flow chart shown in Figure 35 for a double precision number in a 16-bit system. The shift linkages are shown in Figure 36. Initially, the most significant half of the BCD number is stored in R0 and the least significant half is in R1. The Q register is used for storing a part of the binary equivalent during and after the conversion. The BCD number as a whole has to be first shifted down one bit. First R0 is downshifted with the linkages shown in Figure 36a so that its least significant bit is collected in the Mc or carry flip-flop of the Am2904. Then R1 and Q are shifted down as shown in Figure 36b so that Mc is loaded in the MSB of R1. The next two instructions perform the adjustment on this shift and also downshift the adjusted numbers by one bit in preparation for the next adjust and shift. The Multiprecision BCD to Binary conversion instruction is executed on R0 so as to adjust and downshift R0 and its LSB is stored in Mc as shown in Figure 36c. The BCD to Binary conversion instruction following this adjusts R1 and downshifts R1 and Q with Mc being loaded into the MSB of R1 as shown in Figure 36d. These two instructions are performed 15 times in a loop. As a result, R0 and Q get shifted 16 times including the initial shift. Since the contents of R0 are now zeros, it is no longer necessary to shift it further. The Q register contains the least significant half of the binary result which is transferred to R2. After this the BCD to Binary conversion is performed on R1, 16 times with the linkages shown in Figure 36e, so that a zero is input in the MSB of R1. The most significant half of the binary number is available in the Q register at the end of the operation. The double precision BCD to Binary Conversion Algorithm can be made more efficient for certain statistical distribution of numbers. This is possible when it is recognized that the most significant half of the BCD number is equal to zero in the beginning and only a single precision conversion is required on the least significant half. Also when the contents of R0, which initially contains the most significant half of the BCD number, become zero before the first 16 cycles, it is no longer necessary to perform a shifting on it.

One such algorithm is outlined in Figure 37. The initial and final contents of the registers are the same as in Figure 35. Initially, it is tested to see if R0 is equal to zero. If it is, then a single precision conversion is performed on R1 so that the least significant half of the binary equivalent is available in the Q register. This is then transferred to R2 and Q is loaded with a zero. If R0 is not zero, then it is downshifted into Mc as shown in Figure 36a, and the

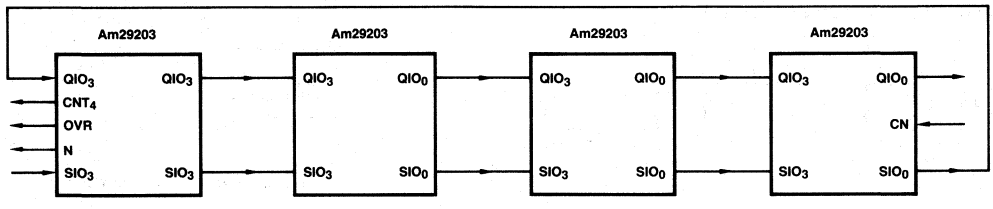


Figure 34. BCD to Binary Conversion

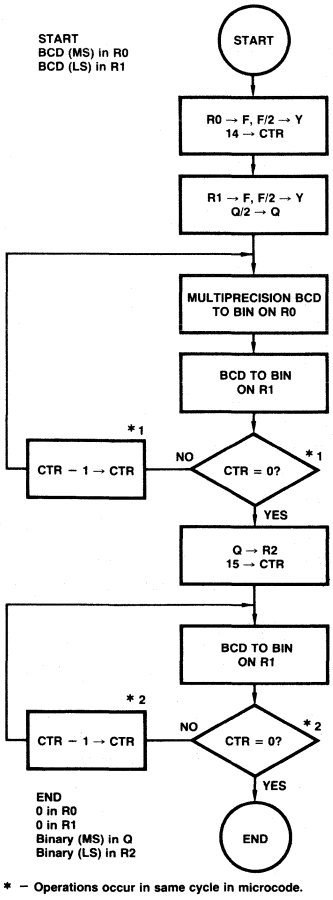


Figure 35. Simple 16-Bit Double Precision BCD to Binary Conversion

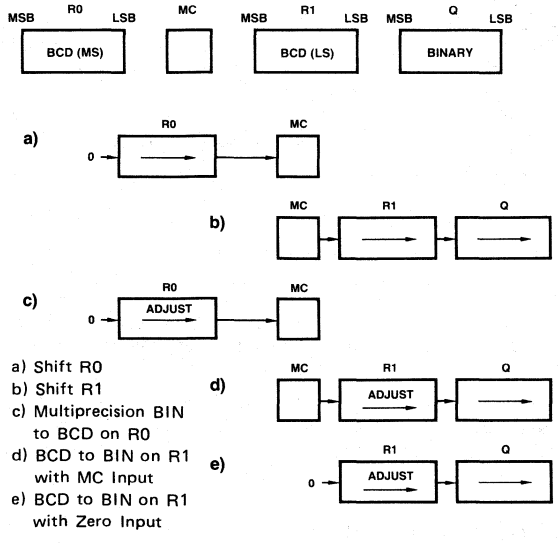


Figure 36. Shift Linkages for Double Precision Binary to BCD Conversion

status is loaded in this step to see if the shifted number had reached zero. R1 cascaded with Q is then downshifted into MC as shown in Figure 36b, and the status is not loaded in this step so that the previously set status can be used for a conditional branch later on while executing a loop. The Multiprecision BCD to binary conversion is performed on R0 and a simultaneous branch is taken if the previously loaded status indicated R0 to be zero. If R0 is non-zero then the algorithm does a double precision conversion on R0 and R1 15 times. The status is set while shifting R0 and is left unchanged while shifting R1 so that a branch can be taken when R0 becomes zero. If it does, the conversion is performed on R1 alone for the remaining cycles. After the first 16 shifts on R1 it may be necessary to unload the Q register in to R2 before completing the last 16 cycles of conversion. This algorithm trades off the number of lines of microcode for a statistically faster conversion. This happens whenever small numbers are being dealt with more frequently in a system where multiprecision numbers may also be required less often. The advantage increases with wider systems.

DIVIDE BY TWO ADJUST

This instruction is useful in dividing BCD numbers by two. It should be used after an instruction which shifts the number down by one bit. The instruction essentially performs a correction on the downshifted number to obtain a valid BCD representation again. The correction performed is identical to the BCD to Binary conversion instruction, but no shifting is done.

DECREMENT BY ONE OR TWO

This function available in the Am29203 does not require the storing of commonly used constants such as one or two in the RAM registers or memory. The instruction decrements by one when Cn is high and by two when Cn is low. The instruction is also useful for addressing byte addressable memories in a 16-bit wide system.

BCD ADD AND SUBTRACT

The Am29203 provides instructions to add or subtract two BCD numbers in one microcycle. There are two subtract instructions whereby the R and S operands can be subtracted from each other. When the BCD addition or subtraction is performed on BCD numbers the result is a valid BCD number. The result is undefined if either of the operands is an invalid BCD representation, so considered when any of the groups of four bits over a slice has a value greater than nine.

The Carry, Propagate and Generate signals have a different significance in BCD arithmetic as compared to binary arithmetic. During addition, the Carry output from a slice indicates that the result of the addition was greater than nine over the slice and that a one should be added to the next BCD digit. In order to speed up the addition process, the Look-Ahead Carry Generator, Am2902, can still be used as before. In case of BCD additions, Propagate signifies that the result equals nine and if there is a carry input to the slice then the carry will have to be propagated out of the slice. The Generate signal while performing additions signifies that the result is already greater than nine and a carry output needs to be generated whether or not the carry input exists. The state of the Propagate signal for results greater than nine does not matter because the Generate signal produces a carry output anyway. In case of subtract operations, the Carry output may be interpreted as a "borrow". Borrowing is necessary in BCD arithmetic when the digit to be subtracted is larger than the digit it is subtracted from. If both the digits are equal then a borrow from a higher digit is not necessary unless the previous digit borrows too. This is equivalent to a propagation of the borrow signal and is indicated on the Propagation line. Whenever borrowing is necessary, irrespective of the previous digit, then the Generate signal is active.

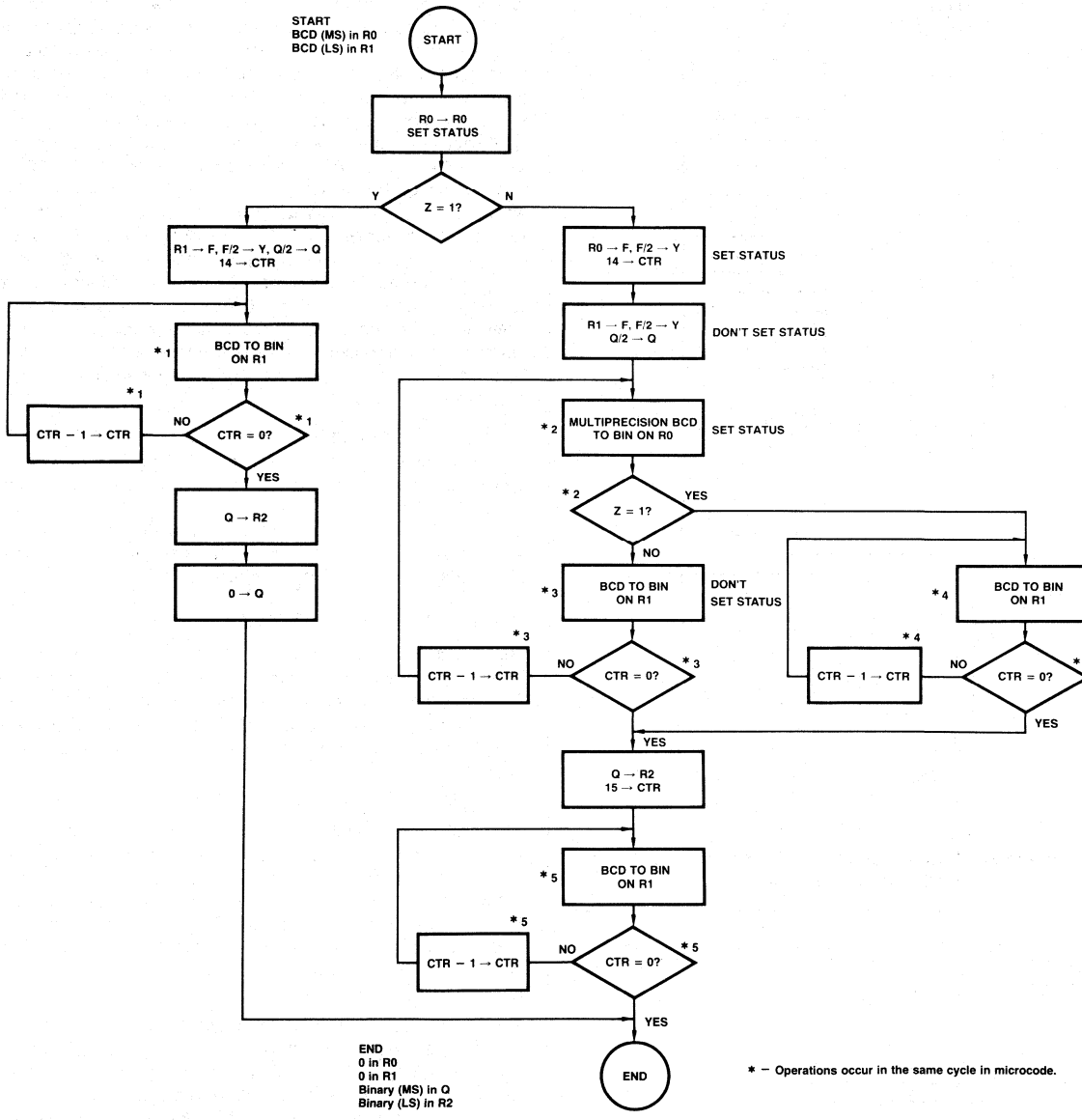


Figure 37. Statistically Efficient 16-Bit Double Precision BCD to Bin Conversion

Generate overrides the Propagate and whenever Generate is active and the state of the Propagate does not matter. The Carry output signal, Cn + 4, goes low whenever a borrowing is done from a higher order digit.

WORD/BYTE OPERATIONS

The Am29203 allows for Word/Byte Operations. Figure 38 pictures a 16-bit system which is capable of doing word or byte (lower half of word) operations.

In the Byte mode the BYTE/$\overline{\text{WORD}}$ line is HIGH which in turn asserts a LOW on the $\overline{\text{W}}/\overline{\text{MSS}}$ input of Device 2 making it the MSS device. At the same time the multiplexer selects the status flags of Device 2. The $\overline{\text{IEN}}$ and $\overline{\text{OE}}_Y$ of Devices 4 and 3 are forced HIGH which disables them from writing into RAM or onto the Y bus.

In the word mode Device 4 is the $\overline{\text{MSS}}$ device and the multiplexer selects its status flags. The $\overline{\text{IEN}}$ inputs are brought low which enables writing in to RAM. The $\overline{\text{OE}}_Y$ is also allowed to go low.

MEMORY EXPANSION

Both the Am2903 and Am29203 allow for a theoretically infinite memory expansion, but the technique is slightly different. (The Am29203 allows writing less than a full word, e.g., a byte.) Fig-

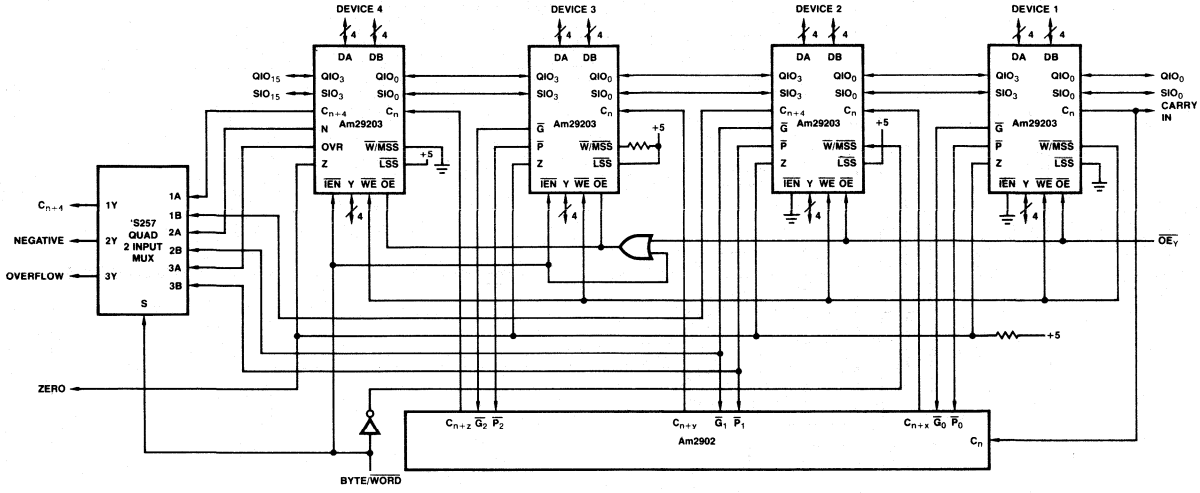


Figure 38. Connections for Word/Byte Operations (Am29203 Only). MPR-719

ure 39, *Am2903 and Am29705,* pictures a 4-bit slice of a system which has 48 words of RAM and 16 words of ROM. RAM storage is provided by the Am2903 and the Am29705s. The Am29705 RAM is functionally identical to the Am2903 RAM. The Am27S19 is used to store constants and masks and is addressable from address port A only. The system is organized around five data buses. Inter-bus communication may be done through the Am29705s or the Am2903. The memory addressing scheme specifies the data source for the R input of the ALU eminating from the register locations specified by address field A. A_{0-3} addresses 16 memory locations in each chip while address bits A_{4-6} are decoded and used for the output enable for the desired chip. The B address field is used to select the S input of the ALU and the C field is used to specify the register location where the result of the ALU operation is to be stored.

Bits B_{0-3} are for source register addressing in each chip. Bits B_4 and B_5 are used for chip output enable selection. C_{0-3} access the 16 destination addresses on each chip while bits C_4 and C_5 control the Write Enable of the desired chip. The source and destination register address are multiplexed such that when the clock is HIGH, the source register address is presented to the B address ports of the RAM's. The Instruction Enable ($\overline{IEN}$) is HIGH at this time. The data flows from the Y port or the internal B port as selected by the decoder whose inputs are B_4 and B_5. When the clock goes LOW, the data eminating from the selected Y outputs of the Am29705's and the RAM outputs of the Am2903 are latched and the destination address is now selected for use by the RAM address lines. When the destination address stabilizes on the address lines, the $\overline{IEN}$ pin is brought LOW. The $\overline{WRITE}$ output of the Am2903 will now go LOW, enabling the decoder sourced by address bits C_4 and C_5. The selected decoder line will go LOW, allowing the desired memory location to be written into. To switch between two- and three-address architecture, the user simply makes the source and destination addresses the same; i.e., $B_{0-3} = C_{0-3}$ and $B_{4-5} = C_{4-5}$. For two-address architecture, the MUX is removed from the circuit.

Memory Expansion with the Am29203

The expansion scheme using the Am29203 and Am29705 is only slightly different from that for the Am2903, and is illustrated in Figure 40. The difference is due to the fact that the WRITE signal from the Am29203 is not internally gated by IEN. This gating is performed external to the Am29203, either in a gate or, as shown in Figure 40, by using the enable on the chip select decoder. The advantage of separating the write signal from the $\overline{IEN}$ signal is that writing can be controlled over less than the full word length. For example, in a 16-bit system, the lower two devices can have one $\overline{IEN}$ signal and the upper two devices a second $\overline{IEN}$ signal. Controlling these two signals separately allows data to be written in either byte without disturbing the other byte. The 2- and 3-address architecture is handled in the same way as with the Am2903.

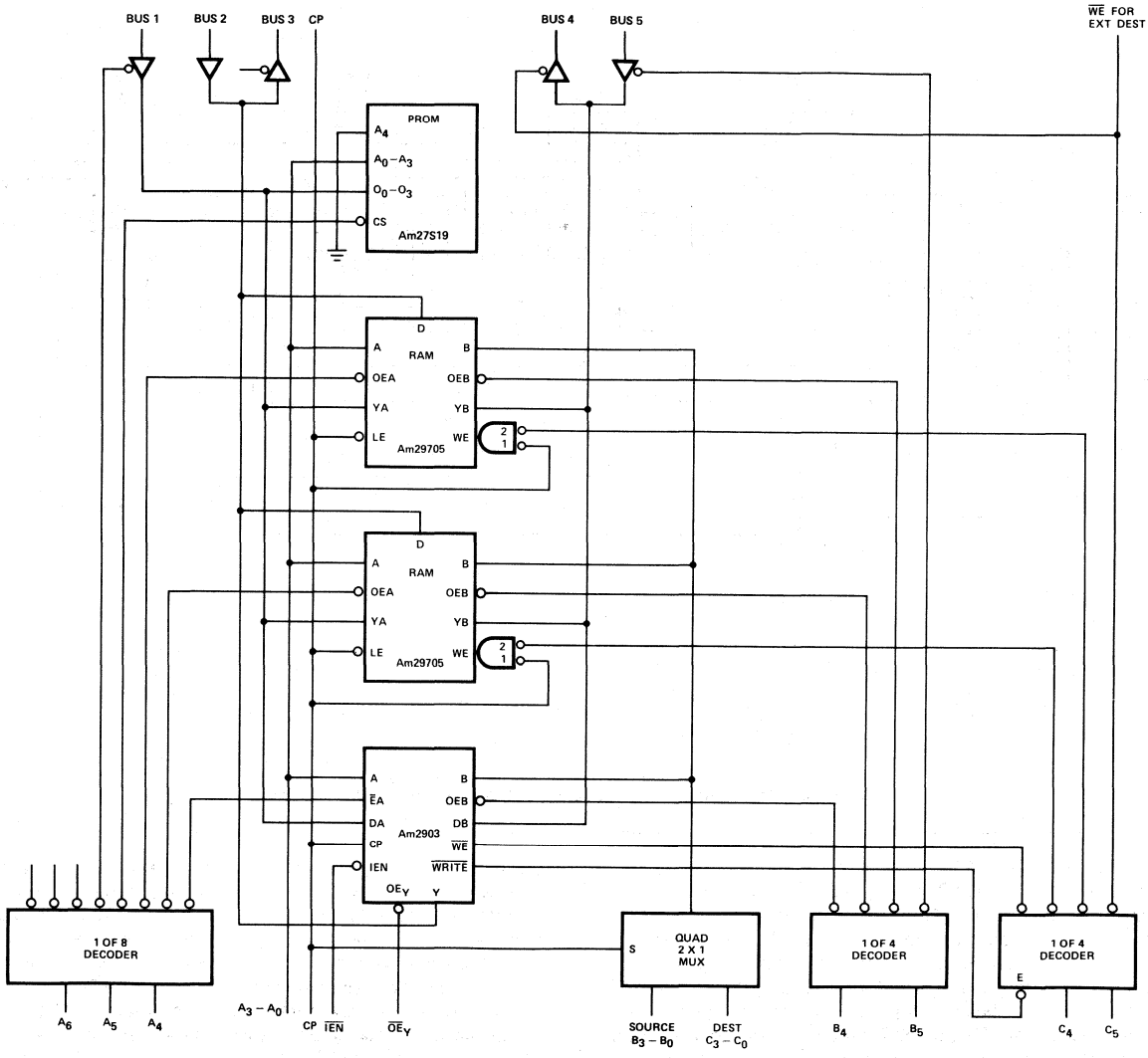


Figure 39. Expanded Memory on Am2903

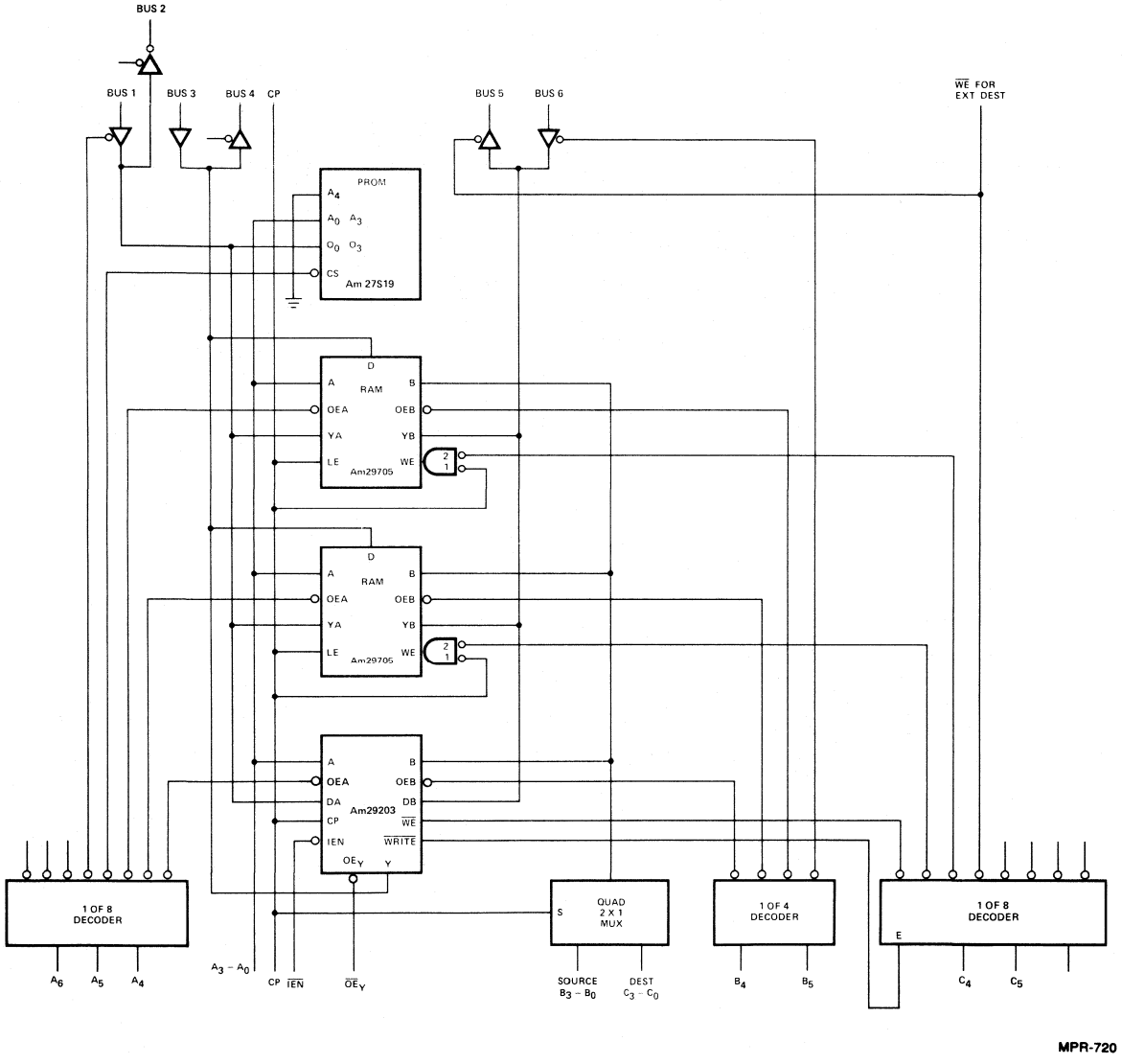


Figure 40. Expanded Memory for Am29203

APPENDIX A

Am2903 SWITCHING CHARACTERISTICS

The switching characteristics of the Am2903 are a function of the power supply voltage, the temperature, and the operating mode of the device. The data has been condensed onto the tables on the following 24 pages. The first sets of tables define the speeds of the device for all operations except the special functions (where I_{43210} = 00000). The remaining tables define the speeds of the combinational paths for each of the special functions. Set-up and hold times do not change for the special functions. An index to the AC tables is shown below. The roman numeral identifies the conditions:

I = room temperature typical
II = room temperature guaranteed
III = guaranteed commercial operating range
IV = guaranteed military operating range

The letter designates the type of data:

A = standard function combinational delays
B = set-up and hold times
C = Enable/Disable times
D = clock and write pulses
E = special function combinational delays

Data is shown in Tables E in bold face where different from the data given in Tables A. Except where otherwise noted, data is taken with inputs switching between 0V and 3.0V at 1V/ns, with the measurement point at 1.5V. Outputs are measured at 1.5V and are loaded with C_L = 50pF and maximum DC load.

INDEX TO SWITCHING TABLES

Table	Data Type	Typical/ Guaranteed	Conditions	Applicable to
I A	Combinational Delays	Typical	5.0V, 25°C	Standard functions
II A	Combinational Delays	Guaranteed	5.0V, 25°C	Standard functions
III A	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Standard functions
III B	Set-up and Hold Times	Guaranteed	4.75 to 5.25V, 0°C to +70°C	All functions
III C	Enable/Disable Times	Guaranteed	4.75 to 5.25V, 0°C to +70°C	All functions
III D	Write Pulse and Clock	Guaranteed	4.75 to 5.25V, 0°C to +70°C	All functions
III E-0	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Unsigned multiply instruction
III E-2	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Two's complement multiply instruction
III E-4	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Increment by one or two instruction
III E-5	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Sign magnitude/two's complement conversion
III E-6	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Two's complement multiply, last cycle
III E-8	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Single-length normalize
III E-A	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	First divide operation (dbl. length norm.)
III E-C	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Two's complement divide
III E-E	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Two's complement divide, correction
IV A	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Standard functions
IV B	Set-up and Hold Times	Guaranteed	4.5 to 5.5V, −55°C to +125°C	All functions
IV C	Enable/Disable Times	Guaranteed	4.5 to 5.5V, −55°C to +125°C	All functions
IV D	Write Pulse and Clock	Guaranteed	4.5 to 5.5V, −55°C to +125°C	All functions
IV E-0	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Unsigned multiply instruction
IV E-2	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Two's complement multiply instruction
IV E-4	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Increment by one or two instruction
IV E-5	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Sign magnitude/two's complement conversion
IV E-6	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Two's complement multiply, last cycle
IV E-8	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Single-length normalize
IV E-A	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	First divide operation (dbl. length norm.)
IV E-C	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Two's complement divide
IV E-E	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Two's complement divide, correction

TABLE I A
Typical Combinational Delays
T_A = 25°C, V_{CC} = 5.0V
Standard Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	54	48	43	66	54	67	–	–	–	52	58	74
B Address	63	56	52	75	62	71	31	–	–	61	66	90
A Address (Logic Mode)	54	–	42	66	55	–	–	–	–	49	59	74
B Address	53	–	45	63	53	–	31	–	–	53	56	76
DA Inputs (Arith. Mode)	40	36	30	52	40	55	–	–	–	37	43	62
DB Inputs	38	35	28	50	38	52	–	–	–	38	41	61
DA Inputs (Logic Mode)	40	–	29	52	40	–	–	–	–	38	43	62
DB Inputs	34	–	20	46	35	–	–	–	–	34	38	57
$\overline{EA}$	39	32	26	51	39	52	–	–	–	36	42	61
C_n	25	18	–	37	25	35	–	–	–	22	28	41
I_0	33	29	22	43	33	38	–	33	*	33 *	36 *	59 *
I_{4321}	46	42	44	57	44	52	–	33	*	42 *	47 *	68 *
I_{8765}	28	–	–	40	–	–	–	32	36 *	27 *	28 *	27 *
$\overline{IEN}$	–	–	–	–	–	–	–	12	–	–	–	–
SIO_3, SIO_0	15	–	–	–	–	–	–	–	–	–	17	20
Clock	55	53	44	67	57	67	23	–	25	53	60	66
Y	–	–	–	12	–	–	–	–	–	–	–	–
$\overline{MSS}$	28	–	28	40	28	28	–	–	–	28	30	28

Note: A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

TABLE III A
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Standard Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	86	81	69	110	86	108	–	–	–	84	94	115
B Address	99	88	81	123	99	112	49	–	–	94	104	140
A Address (Logic Mode)	87	–	68	111	89	–	–	–	–	79	94	115
B Address	84	–	73	108	84	–	49	–	–	84	90	120
DA Inputs (Arith. Mode)	63	60	49	87	64	89	–	–	–	60	70	101
DB Inputs	61	59	47	85	62	84	–	–	–	62	68	98
DA Inputs (Logic Mode)	64	–	48	88	66	–	–	–	–	61	72	101
DB Inputs	55	–	32	79	57	–	–	–	–	52	61	93
$\overline{EA}$	59	53	42	83	59	83	–	–	–	57	64	98
C_n	40	30	–	64	40	58	–	–	–	38	46	67
I_0	52	48	36	76	52	63	–	49	*	50*	58*	93*
I_{4321}	71	65	72	95	69	84	–	49	*	66*	73*	105*
I_{8765}	42	–	–	66	–	–	–	50	60*	42*	45*	42*
$\overline{IEN}$	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	26	–	–	50	–	–	–	–	–	–	29	36
Clock	87	87	71	111	88	108	37	–	40	84	92	105
Y	–	–	–	24	–	–	–	–	–	–	–	–
$\overline{MSS}$	44	–	44	68	44	44	–	–	–	44	46	44

Note: A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

TABLE III B
Guaranteed Set-up and Hold Times
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions
CAUTION: READ NOTES TO TABLE B. NA = Not Applicable; no timing constraint.

To Output / From Input	With Respect to this Signal	HIGH-to-LOW		LOW-to-HIGH		Comment
		Set-up	Hold	Set-up	Hold	
Y	Clock	NA	NA	20	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	30	0	To Write into RAM
A, B as Sources	Clock	27	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	21	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	68	0	See Note 6

Notes:
1. For set-up times from all inputs not specified in Table B, the set-up time is computed by calculating the delay to stable Y outputs and then allowing the Y set-up time. Even if the RAM is not being loaded, the Y set-up time is necessary to set-up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

TABLE III C
Guaranteed Enable/Disable Times
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	31	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	65	60	ns
$\overline{LSS}$	$\overline{WRITE}$	31	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE III D
Guaranteed Clock and Write Pulse Characteristics
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Time CP and WE both LOW to Write	30	ns

TABLE III E-0
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Unsigned Multiply Instruction
(I_{8765} = 0_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**102**	88	–	–	99	112	49	–	–	94	–	–
	IS, LSS	99	88	81	–	–	–	49	–	–	94	–	–
DA, DB Inputs	MSS	**65**	60	–	–	64	89	–	–	–	62	–	–
	IS, LSS	63	60	49	–	–	–	–	–	–	62	–	–
$\overline{EA}$	MSS	**73**	53	–	–	59	83	–	–	–	57	–	–
	IS, LSS	59	53	42	–	–	–	–	–	–	57	–	–
C_n	MSS	**45**	30	–	–	40	58	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**94**	**95**	–	–	**87**	**102**	–	–	*	**70***	*	–
	IS	**94**	**95**	**80**	–	–	–	–	–	*	**70***	*	–
	LSS	**94**	**95**	**80**	**42**	–	–	–	49	*	**70***	*	–
I_{4321}	MSS	**102**	**96**	–	–	**92**	**110**	–	–	*	**72***	*	–
	IS	**102**	**96**	**81**	–	–	–	–	–	*	**72***	*	–
	LSS	**102**	**96**	**81**	**43**	–	–	–	49	*	**72***	*	–
I_{8765}	MSS	**102**	**90**	–	–	**77**	**84**	–	–	*	**72***	*	–
	IS	**102**	**90**	**84**	–	–	–	–	–	*	**72***	*	–
	LSS	**102**	**90**	**84**	**46**	–	–	–	50	*	**72***	*	–
Clock	MSS	**91**	87	–	–	88	108	37	–	40	84	–	–
	IS, LSS	87	87	71	**53**	–	–	37	–	40	84	–	–
Z	MSS	**74**	**62**	–	–	**70**	**78**	–	–	–	**71**	–	–
	IS	**74**	**62**	**48**	–	–	–	–	–	–	**71**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$S + R + C_n$ if $Z = 1$
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-2
Guaranteed Combinational Delays
T_A = 0° to +70°C, V_{CC} = 4.75 to 5.25V
Two's Complement Multiply Instruction
(I_{8765} = 2_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**106**	88	–	–	99	112	49	–	–	94	–	–
	IS, LSS	99	88	81	–	–	–	49	–	–	94	–	–
DA, DB Inputs	MSS	**78**	60	–	–	64	89	–	–	–	62	–	–
	IS, LSS	63	60	49	–	–	–	–	–	–	62	–	–
$\overline{EA}$	MSS	**85**	53	–	–	59	83	–	–	–	57	–	–
	IS, LSS	59	53	42	–	–	–	–	–	–	57	–	–
C_n	MSS	**58**	30	–	–	40	58	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**104**	**95**	–	–	**89**	**102**	–	–	*	**68***	*	–
	IS	**104**	**95**	**78**	–	–	–	–	–	*	**68***	*	–
	LSS	**104**	**95**	**78**	**42**	–	–	–	49	*	**68***	*	–
I_{4321}	MSS	**112**	**95**	–	–	**94**	**108**	–	–	*	**71***	*	–
	IS	**112**	**95**	**78**	–	–	–	–	–	*	**71***	*	–
	LSS	**112**	**95**	**78**	**43**	–	–	–	49	*	**71***	*	–
I_{8765}	MSS	**98**	**84**	–	–	**76**	**100**	–	–	*	**71***	*	–
	IS	**98**	**84**	**82**	–	–	–	–	–	*	**71***	*	–
	LSS	**98**	**84**	**82**	**46**	–	–	–	50	*	**71***	*	–
Clock	MSS	**100**	87	–	–	88	108	37	–	40	84	–	–
	IS, LSS	87	87	71	**53**	–	–	37	–	40	84	–	–
Z	MSS	**90**	**62**	–	–	**69**	**78**	–	–	–	**71**	–	–
	IS	**90**	**62**	**48**	–	–	–	–	–	–	**71**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$R + S + C_n$ if $Z = 1$
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-4
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Increment by One or Two Instruction
(I_{8765} = 4_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mod	MSS	99	88	–	123	99	112	49	–	–	–	–	140
	IS, LSS	99	88	81	123	–	–	49	–	–	–	–	140
DA, DB Inputs	MSS	63	60	–	87	64	89	–	–	–	–	–	101
	IS, LSS	63	60	49	87	–	–	–	–	–	–	–	101
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	40	30	–	64	40	58	–	–	–	–	–	67
	IS, LSS	40	30	–	64	40	58	–	–	–	–	–	67
I_0	MSS	**66**	**60**	–	**90**	**71**	**82**	–	–	*	*	*	**103***
	IS	**66**	**60**	**58**	**90**	–	–	–	–	*	*	*	**103***
	LSS	**66**	**60**	**58**	**90**	–	–	–	49	*	*	*	**103***
I_{4321}	MSS	**71**	**60**	–	**95**	**72**	**80**	–	–	*	*	*	**102***
	IS	**71**	**60**	**58**	**95**	–	–	–	–	*	*	*	**102***
	LSS	**71**	**60**	**58**	**95**	–	–	–	49	*	*	*	**102***
I_{8765}	MSS	**71**	**60**	–	**95**	**72**	**82**	–	–	*	*	*	**102***
	IS	**71**	**60**	**58**	**95**	–	–	–	–	*	*	*	**102***
	LSS	**71**	**60**	**58**	**95**	–	–	–	50	*	*	*	**102***
Clock	MSS	87	87	71	111	88	108	37	–	40	–	–	105
	IS, LSS	87	87	71	111	88	108	37	–	40	–	–	105
Z	MSS	Z is an output											
	IS, LSS	Z is an output											
Y	Any	–	–	–	24	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + 1 + C_n$

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-5
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Sign Magnitude/Two's Complement Conversion
(I_{8765} = 5_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**138**	88	–	**70**	**138**	112	49	–	–	–	–	140
	IS, LSS	99	88	81	–	–	–	49	–	–	–	–	140
DA, DB Inputs	MSS	**98**	60	–	**40**	**98**	89	–	–	–	–	–	101
	IS, LSS	63	60	49	–	–	–	–	–	–	–	–	101
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	**79**	30	–	–	**79**	58	–	–	–	–	–	67
	IS, LSS	40	30	–	–	–	–	–	–	–	–	–	67
I_0	MSS	**102**	**78**	–	**46**	**100**	**112**	–	–	*	*	*	**131***
	IS	**102**	**78**	**70**	–	–	–	–	–	*	*	*	**131***
	LSS	**102**	**78**	**70**	–	–	–	–	49	*	*	*	**131***
I_{4321}	MSS	**102**	**78**	–	**46**	**100**	**103**	–	–	*	*	*	**131***
	IS	**102**	**78**	**72**	–	–	–	–	–	*	*	*	**131***
	LSS	**102**	**78**	**72**	–	–	–	–	49	*	*	*	**131***
I_{8765}	MSS	**100**	**78**	–	**46**	**97**	**105**	–	–	*	*	*	**138***
	IS	**100**	**78**	**65**	–	–	–	–	–	*	*	*	**138***
	LSS	**100**	**78**	**65**	–	–	–	–	50	*	*	*	**138***
Clock	MSS	**118**	87	71	**58**	**118**	108	37	–	–	–	–	105
	IS, LSS	87	87	71	–	–	–	37	–	–	–	–	105
Z	MSS	Z is an output											
	IS, LSS	**72**	**60**	**48**	–	–	–	–	–	–	–	–	**114**
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$\quad \overline{S} + C_n$ if $Z = 1$
$Y_3 = S_3 \oplus F_3$ (MSS)
$Z = S_3$ (MSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-6
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Two's Complement Multiply, Last Cycle
(I_{8765} = 6_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**120**	88	–	–	99	112	49	–	–	94	–	–
	IS, LSS	99	88	81	–	–	–	49	–	–	94	–	–
DA, DB Inputs	MSS	**85**	60	–	–	64	89	–	–	–	62	–	–
	IS, LSS	63	60	49	–	–	–	–	–	–	62	–	–
$\overline{EA}$	MSS	**93**	53	–	–	59	83	–	–	–	57	–	–
	IS, LSS	59	53	42	–	–	–	–	–	–	57	–	–
C_n	MSS	**64**	30	–	–	40	58	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**112**	**99**	–	–	**91**	**120**	–	–	*	**98***	*	–
	IS	**112**	**99**	**86**	–	–	–	–	–	*	**98***	*	–
	LSS	**112**	**99**	**86**	**42**	–	–	–	49	*	**98***	*	–
I_{4321}	MSS	**115**	**93**	–	–	**94**	**124**	–	–	*	**97***	*	–
	IS	**115**	**93**	**85**	–	–	–	–	–	*	**97***	*	–
	LSS	**115**	**93**	**85**	**43**	–	–	–	49	*	**97***	*	–
I_{8765}	MSS	**105**	**93**	–	–	**88**	**114**	–	–	*	**96***	*	–
	IS	**105**	**93**	**78**	–	–	–	–	–	*	**96***	*	–
	LSS	**105**	**93**	**78**	**50**	–	–	–	50	*	**96***	*	–
Clock	MSS	**110**	87	–	–	88	108	37	–	40	84	–	–
	IS, LSS	87	87	71	**53**	–	–	37	–	40	84	–	–
Z	MSS	**91**	**64**	–	–	**74**	**98**	–	–	–	**70**	–	–
	IS	**91**	**64**	**50**	–	–	–	–	–	–	**70**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
Y_3 = OVR ⊕ F_3 (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-8
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Single-Length Normalize Instruction
($I_{8765} = 8_H$, $I_{4321} = 0_H$, $I_0 = 0$)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	99	88	–	–	99	112	49	–	–	–	–	–
	IS, LSS	99	88	81	–	–	–	49	–	–	–	–	–
DA, DB Inputs	MSS	63	60	–	–	64	89	–	–	–	–	–	–
	IS, LSS	63	60	49	–	–	–	–	–	–	–	–	–
$\overline{EA}$	MSS	59	53	–	–	59	83	–	–	–	–	–	–
	IS, LSS	59	53	42	–	–	–	–	–	–	–	–	–
C_n	MSS	40	30	–	–	40	58	–	–	–	–	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	–	–
I_0	MSS	**67**	**52**	–	**33**	**45**	**42**	–	–	*	*	**72***	–
	IS	**67**	**52**	**58**	**33**	–	–	–	–	*	*	**72***	–
	LSS	**67**	**52**	**58**	**33**	–	–	–	49	*	*	**72***	–
I_{4321}	MSS	**68**	**58**	–	**34**	**45**	**47**	–	–	*	*	**72***	–
	IS	**68**	**58**	**58**	**36**	–	–	–	–	*	*	**72***	–
	LSS	**68**	**58**	**58**	**36**	–	–	–	49	*	*	**72***	–
I_{8765}	MSS	**66**	**70**	–	**44**	**50**	**47**	–	–	*	*	**72***	–
	IS	**66**	**70**	**41**	**44**	–	–	–	–	*	*	**72***	–
	LSS	**66**	**70**	**41**	**44**	–	–	–	50	*	*	**72***	–
Clock	MSS	87	**49**	–	**46**	**49**	**47**	37	–	40	–	92	–
	IS, LSS	87	87	71	**48**	–	–	37	–	40	–	92	–
Z	MSS	Z is an output											
	IS, LSS	Z is an output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$
$C_{n+4} = Q_3 \oplus Q_2$ (MSS)
$OVR = Q_2 \oplus Q_1$ (MSS)
$N = Q_3$ (MSS)
$Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-A
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
First Divide Operation (Double Length Normalize)
(I_{8765} = A_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	99	**113**	–	**94**	**94**	**102**	49	–	–	–	**120**	–
	IS, LSS	99	88	81	–	–	–	49	–	–	–	104	–
DA, DB Inputs	MSS	63	**75**	–	**54**	**54**	**62**	–	–	–	–	**80**	–
	IS, LSS	63	60	49	–	–	–	–	–	–	–	70	–
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	**76**	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	64	–
C_n	MSS	40	**54**	–	**45**	**45**	**50**	–	–	–	–	**68**	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**69**	**95**	–	**68**	**72**	**86**	–	–	*	*	**96** *	–
	IS	**69**	**95**	**56**	**68**	–	–	–	–	*	*	**96** *	–
	LSS	**69**	**95**	**56**	**68**	–	–	–	49	*	*	**96** *	–
I_{4321}	MSS	**69**	**94**	–	**68**	**72**	**86**	–	–	*	*	**96** *	–
	IS	**69**	**94**	**57**	**68**	–	–	–	–	*	*	**96** *	–
	LSS	**69**	**94**	**57**	**68**	–	–	–	49	*	*	**96** *	–
I_{8765}	MSS	**69**	**95**	–	**68**	**72**	**86**	–	–	*	*	**96** *	–
	IS	**69**	**95**	**57**	**68**	–	–	–	–	*	*	**96** *	–
	LSS	**69**	**95**	**57**	**68**	–	–	–	50	*	*	**96** *	–
Clock	MSS	87	**101**	–	**80**	**84**	**89**	37	–	40	–	**106**	–
	IS, LSS	87	87	71	**80**	–	–	37	–	40	–	92	–
Z	MSS	Z is an output											
	IS	Z is an output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$
$N = F_3$ (MSS)
$SIO_3 = F_3 \oplus R_3$ (MSS)
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = F_2 \oplus F_1$ (MSS)
$Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-C
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Two's Complement Divide Operation
(I_{8765} = C_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	99	88	–	–	99	112	49	–	–	–	**107**	–
	IS, LSS	99	88	81	–	–	–	49	–	–	–	104	–
DA, DB Inputs	MSS	63	60	–	–	64	89	–	–	–	–	**84**	–
	IS, LSS	63	60	49	–	–	–	–	–	–	–	70	–
$\overline{EA}$	MSS	59	53	–	–	59	83	–	–	–	–	**91**	–
	IS, LSS	59	53	42	–	–	–	–	–	–	–	64	–
C_n	MSS	40	30	–	–	40	58	–	–	–	–	**64**	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**94**	**93**	–	**39**	**94**	**120**	–	–	*	*	**108***	–
	IS	**94**	**93**	**74**	–	–	–	–	–	*	*	**108***	–
	LSS	**94**	**93**	**74**	–	–	–	–	49	*	*	**108***	–
I_{4321}	MSS	**94**	**84**	–	**42**	**93**	**120**	–	–	*	*	**108***	–
	IS	**94**	**84**	**74**	–	–	–	–	–	*	*	**108***	–
	LSS	**94**	**84**	**74**	–	–	–	–	49	*	*	**108***	–
I_{8765}	MSS	**93**	**89**	–	**43**	**93**	**120**	–		*	*	**108***	–
	IS	**93**	**89**	**64**	–	–	–	–	–	*	*	**108***	–
	LSS	**93**	**89**	**64**	–	–	–	–	50	*	*	**108***	–
Clock	MSS	87	87	–	**53**	88	108	37	–	40	–	**130**	–
	IS, LSS	87	87	71	–	–	–	37	–	40	–	92	–
Z	MSS	Z is an output											
	IS, LSS	**68**	**65**	**52**	–	–	–	–	–	–	–	**77**	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = R + S + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-E
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Two's Complement Divide, Correction
(I_{8765} = E_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	99	88	–	–	99	112	49	–	–	–	104	–
	IS, LSS	99	88	81	–	–	–	49	–	–	–	104	–
DA, DB Inputs	MSS	63	60	–	–	64	89	–	–	–	–	70	–
	IS, LSS	63	60	49	–	–	–	–	–	–	–	70	–
$\overline{EA}$	MSS	59	53	–	–	59	83	–	–	–	–	64	–
	IS, LSS	59	53	42	–	–	–	–	–	–	–	64	–
C_n	MSS	40	30	–	–	40	58	–	–	–	–	46	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**95**	**91**	–	**42**	**94**	**120**	–	–	*	*	**98***	–
	IS	**95**	**91**	**72**	–	–	–	–	–	*	*	**98***	–
	LSS	**95**	**91**	**72**	–	–	–	–	49	*	*	**98***	–
I_{4321}	MSS	**96**	**91**	–	**42**	**94**	**118**	–	–	*	*	**98***	–
	IS	**96**	**91**	**78**	–	–	–	–	–	*	*	**98***	–
	LSS	**96**	**91**	**78**	–	–	–	–	49	*	*	**98***	–
I_{8765}	MSS	**85**	**78**	–	**43**	**74**	**89**	–	–	*	*	**88***	–
	IS	**85**	**78**	**62**	–	–	–	–	–	*	*	**88***	–
	LSS	**85**	**78**	**62**	–	–	–	–	50	*	*	**88***	–
Clock	MSS	87	87	–	**53**	88	108	37	–	40	–	92	–
	IS, LSS	87	87	71	–	–	–	37	–	40	–	92	–
Z	MSS	Z is an output											
	IS, LSS	**73**	**66**	**54**	–	–	–	–	–	–	–	**79**	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = R + S + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

Table IV A
Guaranteed Combinational Delays
T_C = −55° to +125°C, V_{CC} = 4.5V to 5.5V
Standard Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	91	85	72	116	92	115	–	–	–	89	98	120
B Address	101	93	84	126	102	118	52	–	–	97	106	148
A Address (Logic Mode)	92	–	72	117	93	–	–	–	–	84	98	120
B Address	86	–	73	111	89	–	52	–	–	86	92	125
DA Inputs (Arith. Mode)	64	62	51	89	66	94	–	–	–	62	71	107
DB Inputs	63	60	48	88	63	89	–	–	–	64	68	100
DA Inputs (Logic Mode)	65	–	51	90	67	–	–	–	–	62	72	108
DB Inputs	56	–	32	81	57	–	–	–	–	52	63	100
$\overline{EA}$	60	56	43	85	60	87	–	–	–	58	64	103
C_n	40	30	–	65	40	59	–	–	–	38	46	69
I_0	52	50	36	77	52	66	–	53	*	51 *	58 *	96 *
I_{4321}	72	69	73	97	71	88	–	53	*	66 *	75 *	111 *
I_{8765}	44	–	–	69	–	–	–	50	65 *	42 *	45 *	42 *
$\overline{IEN}$	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	26	–	–	51	–	–	–	–	–	–	29	36
Clock	89	90	74	114	89	116	39	–	42	91	96	110
Y	–	–	–	25	–	–	–	–	–	–	–	–
$\overline{MSS}$	45	–	44	70	44	44	–	–	–	44	46	44

Note: A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

TABLE IV B
Guaranteed Set-up and Hold Times
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
All Functions
CAUTION: READ NOTES TO TABLE B. NA = Not Applicable; no timing constraint.

Input	With Respect to this Signal	HIGH-to-LOW		LOW-to-HIGH		Comment
		Set-up	Hold	Set-up	Hold	
Y	Clock	NA	NA	23	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	35	0	To Write into RAM
A, B as Sources	Clock	38	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	23	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	74	0	See Note 6

Notes:
1. For set-up times from all inputs not specified in Table IV B, the set-up time is computed by calculating the delay to stable Y outputs and then allowing the Y set-up time. Even if the RAM is not being loaded, the Y set-up time is necessary to set-up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

TABLE IV C
Guaranteed Enable/Disable Times
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	34	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	70	60	ns
$\overline{LSS}$	$\overline{WRITE}$	34	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE IV D
Guaranteed Clock and Write Pulse Characteristics
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
All Functions

Minimum Clock LOW Time	40	ns
Minimum Clock HIGH Time	40	ns
Minimum Time CP and WE both LOW to Write	40	ns

TABLE IV E-0
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Unsigned Multiply Instruction
(I_{8765} = 0_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**103**	93	–	–	102	118	52	–	–	97	–	–
	IS, LSS	101	93	84	–	–	–	52	–	–	97	–	–
DA, DB Inputs	MSS	**66**	62	–	–	66	94	–	–	–	64	–	–
	IS, LSS	64	62	51	–	–	–	–	–	–	64	–	–
$\overline{EA}$	MSS	**74**	56	–	–	60	87	–	–	–	58	–	–
	IS, LSS	60	56	43	–	–	–	–	–	–	58	–	–
C_n	MSS	**45**	30	–	–	40	59	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**97**	**97**	–	–	**87**	**106**	–	–	*	**71***	*	–
	IS	**97**	**97**	**85**	–	–	–	–	–	*	**71***	*	–
	LSS	**97**	**97**	**85**	**42**	–	–	–	53	*	**71***	*	–
I_{4321}	MSS	**103**	**100**	–	–	**94**	**111**	–	–	*	**73***	*	–
	IS	**103**	**100**	**86**	–	–	–	–	–	*	**73***	*	–
	LSS	**103**	**100**	**86**	**43**	–	–	–	53	*	**73***	*	–
I_{8765}	MSS	**102**	**93**	–	–	**76**	**89**	–	–	*	**75***	*	–
	IS	**102**	**93**	**92**	–	–	–	–	–	*	**75***	*	–
	LSS	**102**	**93**	**92**	**51**	–	–	–	50	*	**75**	*	–
Clock	MSS	**94**	90	–	–	89	116	39	–	42	91	–	–
	IS, LSS	89	90	74	**57**	–	–	39	–	42	91	–	–
Z	MSS	**76**	**65**	–	–	**70**	**81**	–	–	–	**72**	–	–
	IS	**76**	**65**	**49**	–	–	–	–	–	–	**72**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$S + R + C_n$ if $Z = 1$
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-2
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Two's Complement Multiply Instruction
(I_{8765} = 2_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**113**	93	–	–	102	118	52	–	–	97	–	–
	IS, LSS	101	93	84	–	–	–	52	–	–	97	–	–
DA, DB Inputs	MSS	**78**	62	–	–	66	94	–	–	–	64	–	–
	IS, LSS	64	62	51	–	–	–	–	–	–	64	–	–
$\overline{EA}$	MSS	**85**	56	–	–	60	87	–	–	–	58	–	–
	IS, LSS	60	56	43	–	–	–	–	–	–	58	–	–
C_n	MSS	**58**	30	–	–	40	59	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**105**	**97**	–	–	**89**	**102**	–	–	*	**71** *	*	–
	IS	**105**	**97**	**81**	–	–	–	–	–	*	**71** *	*	–
	LSS	**105**	**97**	**81**	**42**	–	–	–	53	*	**71** *	*	–
I_{4321}	MSS	**112**	**98**	–	–	**94**	**111**	–	–	*	**75** *	*	–
	IS	**112**	**98**	**85**	–	–	–	–	–	*	**75** *	*	–
	LSS	**112**	**98**	**85**	**43**	–	–	–	53	*	**75** *	*	–
I_{8765}	MSS	**99**	**86**	–	–	**78**	**100**	–	–	*	**74** *	*	–
	IS	**99**	**86**	**84**	–	–	–	–	–	*	**74** *	*	–
	LSS	**99**	**86**	**84**	**48**	–	–	–	50	*	**74** *	*	–
Clock	MSS	**107**	90	–	–	89	116	39	–	42	91	–	–
	IS, LSS	89	90	74	**57**	–	–	39	–	42	91	–	–
Z	MSS	**90**	**65**	–	–	**70**	**81**	–	–	–	**72**	–	–
	IS	**90**	**65**	**48**	–	–	–	–	–	–	**72**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$S + R + C_n$ is $Z = 1$
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-4
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Increment by One or Two Instruction
($I_{8765} = 4_H$, $I_{4321} = 0_H$, $I_0 = 0$)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	93	–	126	102	118	52	–	–	–	–	148
	IS, LSS	101	93	84	126	–	–	52	–	–	–	–	148
DA, DB Inputs	MSS	64	62	–	89	66	94	–	–	–	–	–	107
	IS, LSS	64	62	51	89	–	–	–	–	–	–	–	107
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	40	30	–	65	40	59	–	–	–	–	–	69
	IS, LSS	40	30	–	65	40	59	–	–	–	–	–	69
I_0	MSS	**73**	**61**	–	**98**	**72**	**87**	–	–	*	*	*	**110***
	IS	**73**	**61**	**62**	**98**	–	–	–	–	*	*	*	**110***
	LSS	**73**	**61**	**62**	**98**	–	–	–	53	*	*	*	**110***
I_{4321}	MSS	**72**	**61**	–	**97**	**74**	**87**	–	–	*	*	*	**110***
	IS	**72**	**61**	**62**	**97**	–	–	–	–	*	*	*	**110***
	LSS	**72**	**61**	**62**	**97**	–	–	–	53	*	*	*	**110***
I_{8765}	MSS	**72**	**61**	–	**97**	**74**	**87**	–	–	*	*	*	**110***
	IS	**72**	**61**	**62**	**97**	–	–	–	–	*	*	*	**110***
	LSS	**72**	**61**	**62**	**97**	–	–	–	50	*	*	*	**110***
Clock	MSS	89	90	74	114	89	116	39	–	42	–	–	110
	IS, LSS	89	90	74	114	89	116	39	–	42	–	–	110
Z	MSS	Z is an output											
	IS, LSS	Z is an output											
Y	Any	–	–	–	25	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + 1 + C_n$

Notes:
1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-5
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Sign Magnitude/Two's Complement Conversion
(I_{8765} = 5_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**143**	93	–	**78**	**143**	118	52	–	–	–	–	148
	IS, LSS	101	93	84	–	–	–	52	–	–	–	–	148
DA, DB Inputs	MSS	**103**	62	–	**40**	**103**	94	–	–	–	–	–	107
	IS, LSS	64	62	51	–	–	–	–	–	–	–	–	107
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	**83**	30	–	–	**83**	59	–	–	–	–	–	69
	IS, LSS	40	30	–	–	–	–	–	–	–	–	–	69
I_0	MSS	**102**	**80**	–	**50**	**100**	**115**	–	–	*	*	*	**132***
	IS	**102**	**80**	**70**	–	–	–	–	–	*	*	*	**132***
	LSS	**102**	**80**	**70**	–	–	–	–	53	*	*	*	**132***
I_{4321}	MSS	**102**	**80**	–	**50**	**102**	**110**	–	–	*	*	*	**132***
	IS	**102**	**80**	**75**	–	–	–	–	–	*	*	*	**132***
	LSS	**102**	**80**	**75**	–	–	–	–	53	*	*	*	**132***
I_{8765}	MSS	**103**	**80**	–	**50**	**100**	**112**	–	–	*	*	*	**142***
	IS	**103**	**80**	**65**	–	–	–	–	–	*	*	*	**142***
	LSS	**103**	**80**	**65**	–	–	–	–	50	*	*	*	**142***
Clock	MSS	**120**	90	–	**61**	**120**	116	39	–	–	–	–	110
	IS, LSS	89	90	74	–	–	–	39	–	–	–	–	110
Z	MSS	Z is an output											
	IS, LSS	**76**	**61**	**51**	–	–	–	–	–	–	–	–	**118**
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = \overline{S} + C_n$ if Z = 0
$\overline{S} + C_n$ if Z = 1
$Y_3 = S_3 \oplus F_3$ (MSS)
$Z = S_3$ (MSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-6
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Two's Complement Multiply, Last Cycle
(I_{8765} = 6_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**121**	93	–	–	102	118	52	–	–	97	–	–
	IS, LSS	101	93	84	–	–	–	52	–	–	97	–	–
DA, DB Inputs	MSS	**88**	62	–	–	66	94	–	–	–	64	–	–
	IS, LSS	64	62	51	–	–	–	–	–	–	64	–	–
$\overline{EA}$	MSS	**96**	56	–	–	60	87	–	–	–	58	–	–
	IS, LSS	60	56	43	–	–	–	–	–	–	58	–	–
C_n	MSS	**64**	30	–	–	40	59	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**118**	**102**	–	–	**97**	**126**	–	–	*	**102***	*	–
	IS	**118**	**102**	**87**	–	–	–	–	–	*	**102***	*	–
	LSS	**118**	**102**	**87**	**42**	–	–	–	53	*	**102***	*	–
I_{4321}	MSS	**120**	**101**	–	–	**97**	**127**	–	–	*	**101***	*	–
	IS	**120**	**101**	**86**	–	–	–	–	–	*	**101***	*	–
	LSS	**120**	**101**	**86**	**43**	–	–	–	53	*	**101***	*	–
I_{8765}	MSS	**105**	**98**	–	–	**88**	**115**	–	–	*	**102***	*	–
	IS	**105**	**98**	**86**	–	–	–	–	–	*	**102***	*	–
	LSS	**105**	**98**	**86**	**51**	–	–	–	50	*	**102***	*	–
Clock	MSS	**110**	90	–	–	89	116	39	–	42	91	–	–
	IS, LSS	89	90	74	**58**	–	–	39	–	42	91	–	–
Z	MSS	**92**	**67**	–	–	**80**	**103**	–	–	–	**72**	–	–
	IS	**92**	**67**	**53**	–	–	–	–	–	–	**72**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if Z = 0
$S - R - 1 + C_n$ is Z = 1
$Y_3 = (OVR \oplus F_3)$ MSS
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-8
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Single-Length Normalize Instruction
(I_{8765} = 8_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	93	–	–	102	118	52	–	–	–	–	–
	IS, LSS	101	93	84	–	–	–	52	–	–	–	–	–
DA, DB Inputs	MSS	63	60	–	–	66	94	–	–	–	–	–	–
	IS, LSS	63	60	51	–	–	–	–	–	–	–	–	–
$\overline{EA}$	MSS	60	56	–	–	60	87	–	–	–	–	–	–
	IS, LSS	60	56	43	–	–	–	–	–	–	–	–	–
C_n	MSS	40	30	–	–	40	59	–	–	–	–	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	–	–
I_0	MSS	**72**	**60**	–	**34**	**43**	**42**	–	–	*	*	**78***	–
	IS	**72**	**60**	**59**	**34**	–	–	–	–	*	*	**78***	–
	LSS	**72**	**60**	**59**	**34**	–	–	–	53	*	*	**78***	–
I_{4321}	MSS	**72**	**60**	–	**38**	**48**	**47**	–	–	*	*	**78***	–
	IS	**72**	**60**	**60**	**38**	–	–	–	–	*	*	**78***	–
	LSS	**72**	**60**	**60**	**38**	–	–	–	53	*	*	**78***	–
I_{8765}	MSS	**67**	**58**	–	**50**	**53**	**47**	–	–	*	*	**72***	–
	IS	**67**	**58**	**42**	**50**	–	–	–	–	*	*	**72***	–
	LSS	**67**	**58**	**42**	**50**	–	–	–	50	*	*	**72***	–
Clock	MSS	89	**53**	–	**53**	**49**	**49**	39	–	42	–	96	–
	IS, LSS	89	90	74	**53**	–	–	39	–	42	–	96	–
Z	MSS	Z is an output											
	IS, LSS	Z is an output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$
$C_{n+4} = Q_3 \oplus Q_2$ (MSS)
$OVR = Q_2 \oplus Q_1$ (MSS)
$N = Q_3$ (MSS)
$Z = \overline{Q_0 Q_1 Q_2 Q_3}$

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-A
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
First Divide Operation (Double Length Normalize)
(I_{8765} = A_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	**122**	–	**96**	**100**	**112**	52	–	–	–	**130**	–
	IS, LSS	101	93	84	96	–	–	52	–	–	–	106	–
DA, DB Inputs	MSS	64	**80**	–	**63**	**65**	**72**	–	–	–	–	**84**	–
	IS, LSS	64	62	51	63	–	–	–	–	–	–	71	–
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	**80**	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	46	–
C_n	MSS	40	**57**	–	**48**	**48**	**55**	–	–	–	–	**68**	–
	IS, LSS	40	30	–	48	–	–	–	–	–	–	46	–
I_0	MSS	**71**	**98**	–	**85**	**72**	**91**	–	–	*	*	**101***	–
	IS	**71**	**98**	**61**	**85**	–	–	–	–	*	*	**101***	–
	LSS	**71**	**98**	**61**	**85**	–	–	–	53	*	*	**101***	–
I_{4321}	MSS	**71**	**98**	–	**85**	**76**	**91**	–	–	*	*	**101***	–
	IS	**71**	**98**	**61**	**85**	–	–	–	–	*	*	**101***	–
	LSS	**71**	**98**	**61**	**85**	–	–	–	53	*	*	**101***	–
I_{8765}	MSS	**71**	**98**	–	**85**	**76**	**91**	–	–	*	*	**101***	–
	IS	**71**	**98**	**61**	**85**	–	–	–	–	*	*	**101***	–
	LSS	**71**	**98**	**61**	**85**	–	–	–	50	*	*	**101***	–
Clock	MSS	89	**113**	–	**90**	**87**	**98**	39	–	42	–	**114**	–
	IS, LSS	89	90	74	**90**	–	–	39	–	42	–	96	–
Z	MSS	Z is an output											
	IS	Z is an output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$
$N = F_3$ (MSS)
$SIO_3 = F_3 \oplus R_3$ (MSS)
$Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = F_2 \oplus F_1$ (MSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-C
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Two's Complement Divide Operation
(I_{8765} = C_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	93	–	–	102	118	52	–	–	–	**112**	–
	IS, LSS	101	93	84	–	–	–	52	–	–	–	106	–
DA, DB Inputs	MSS	64	62	–	–	66	94	–	–	–	–	**88**	–
	IS, LSS	64	62	51	–	–	–	–	–	–	–	71	–
$\overline{EA}$	MSS	60	56	–	–	60	87	–	–	–	–	**96**	–
	IS, LSS	60	56	43	–	–	–	–	–	–	–	64	–
C_n	MSS	40	30	–	–	40	59	–	–	–	–	**64**	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**95**	**96**	–	**42**	**98**	**127**	–	–	*	*	**113***	–
	IS	**95**	**96**	**77**	–	–	–	–	–	*	*	**113***	–
	LSS	**95**	**96**	**77**	–	–	–	–	53	*	*	**113***	–
I_{4321}	MSS	**96**	**96**	–	**42**	**97**	**124**	–	–	*	*	**114***	–
	IS	**96**	**97**	**82**	–	–	–	–	–	*	*	**114***	–
	LSS	**96**	**97**	**82**	–	–	–	–	53	*	*	**114***	–
I_{8765}	MSS	**98**	**97**	–	**44**	**102**	**112**	–	–	*	*	**119***	–
	IS	**98**	**97**	**64**	–	–	–	–	–	*	*	**119***	–
	LSS	**98**	**97**	**64**	–	–	–	–	50	*	*	**119***	–
Clock	MSS	89	90	–	**58**	89	116	39	–	42	–	**136**	–
	IS, LSS	89	90	74	–	–	–	39	–	42	–	96	–
Z	MSS	Z is an output											
	IS, LSS	**71**	**68**	**56**	–	–	–	–	–	–	–	**81**	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + R + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-E
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Two's Complement Divide, Correction
(I_{8765} = E_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	93	–	–	102	118	52	–	–	–	106	–
	IS, LSS	101	93	84	–	–	–	52	–	–	–	106	–
DA, DB Inputs	MSS	64	62	–	–	66	94	–	–	–	–	71	–
	IS, LSS	64	62	51	–	–	–	–	–	–	–	71	–
$\overline{EA}$	MSS	60	56	–	–	60	87	–	–	–	–	64	–
	IS, LSS	60	56	43	–	–	–	–	–	–	–	64	–
C_n	MSS	40	30	–	–	40	59	–	–	–	–	46	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**98**	**96**	–	**42**	**96**	**127**	–	–	*	*	**105***	–
	IS	**98**	**96**	**78**	–	–	–	–	–	*	*	**105***	–
	LSS	**98**	**96**	**78**	–	–	–	–	53	*	*	**105***	–
I_{4321}	MSS	**100**	**96**	–	**43**	**97**	**123**	–	–	*	*	**104***	–
	IS	**100**	**96**	**84**	–	–	–	–	–	*	*	**104***	–
	LSS	**100**	**96**	**84**	–	–	–	–	53	*	*	**104***	–
I_{8765}	MSS	**85**	**78**	–	**44**	**78**	**95**	–	–	*	*	**89***	–
	IS	**85**	**78**	**62**	–	–	–	–	–	*	*	**89***	–
	LSS	**85**	**78**	**62**	–	–	–	–	50	*	*	**89***	–
Clock	MSS	89	90	–	**58**	89	116	39	–	42	–	96	–
	IS, LSS	89	90	74	–	–	–	39	–	42	–	96	–
Z	MSS	Z is an output											
	IS, LSS	**76**	**70**	**54**	–	–	–	–	–	–	–	**79**	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = R + S + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

Am2903A

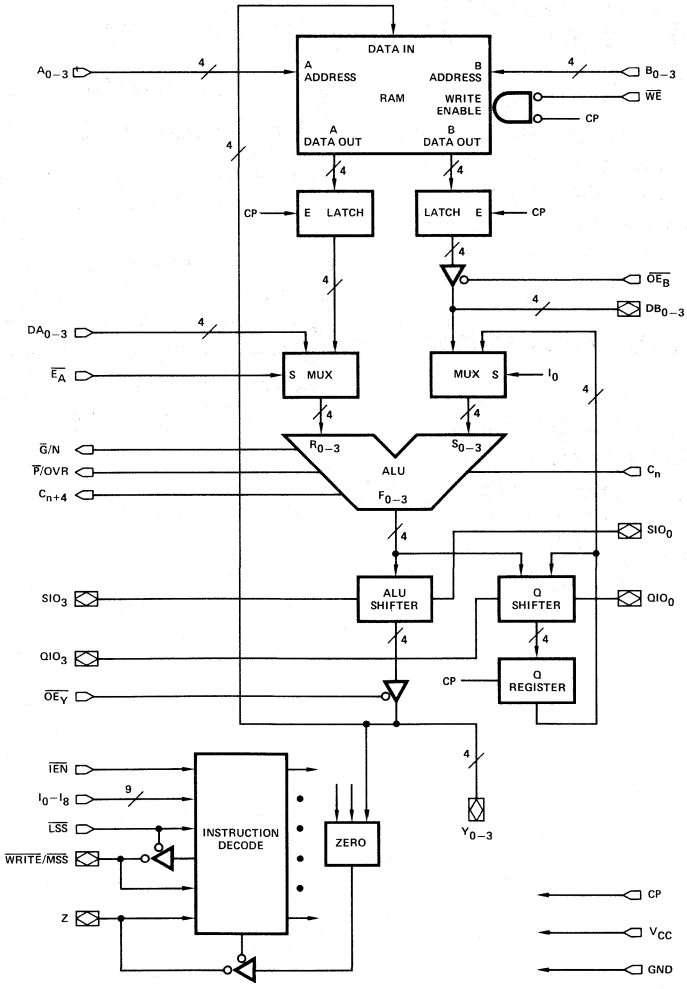
The Superslice®

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Second generation of Am2903 Superslice® –**
  Improved design/process results in fastest version of the Am2903.
- **Plug-in replacement for Am2903 –**
  The Am2903A is a pin-for-pin replacement for the original version of the Am2903. Only the switching speeds have changed.
- **At least 30% faster –**
  The design objective is for the Am2903A to be at least 30% faster than the original Am2903 on critical paths.

BLOCK DIAGRAM



Introducing the Am2904 — LSI Glue

We've provided LSI solutions to large portions of digital processors with our Am2901 and 2903 ALUs, 2909/10/11 sequencers, 2940 DMA chips and others. But the ALU has still been surrounded by a lot of MSI "glue" – multiplexers, registers, and SSI. *Now AMD offers the Am2904, a single LSI chip that replaces most of the MSI lying around the ALU.*

Eliminates Shift Multiplexers

Every CPU needs the ability to shift data words left or right. In the Am2901 and 2903, two shifters are built in, one for the ALU data, and the other for the auxiliary "Q" register. At the ends of an array of ALUs, some multiplexers are used to select the source of the new bit to be shifted into the data word. It may be a 0 or a 1, a sign or carry bit, or the bit shifted out of the other end of the array. These multiplexers are contained inside the Am2904. Thirty-two different shift linkages are available – 16 left and 16 right.

Eliminates Carry-In Control Mux

For each arithmetic operation of an ALU, the carry-in must be selected from a 0 (for add), a 1 (for subtract), the carry flip-flop (for double length operations), or some other source. This multiplexer is included in the 2904, with seven different sources for the carry-in available.

Eliminates the Status Register

Following each ALU operation, most machines capture the four status bits carry, overflow, zero, and negative. A four-bit register inside the 2904 performs this function. A second four-bit register can be swapped with the first one to provide a one-level stack on the status register for foreground/background or interrupt levels.

The second register may be loaded directly from the ALU, if desired, on a bit-by-bit basis. Any individual status bit(s) may be updated without disturbing the others. In this application, the second register can represent machine instruction level status.

Eliminates SSI and Condition Code Mux

Logic inside the Am2904 develops logical combinations of the status bits to detect conditions such as $A > B$, $A < B$ on both signed and unsigned numbers. These conditions as well as the individual status bits can be tested by the on-chip condition code multiplexer. The output of the CC mux can be fed directly to the Am2910 sequencer, or can be three-stated with other condition code sources, or can be fed to an external wider CC multiplexer.

Am2904

Status and Shift Control Unit

DISTINCTIVE CHARACTERISTICS

- **Replaces most MSI used around any ALU** including the Am2901, Am2903 and MSI ALUs.
- **Generates Carry-In to the ALU**
  Carry signal is selectable from 7 different sources.
- **Contains shift linkage multiplexers**
  Connects to shift lines at the ends of an Am2901 or Am2903 array to implement single and double length arithmetic and logical shifts and rotates – 32 different modes in all.
- **Contains two edge-triggered status registers**
  Use for foreground/background registers in controllers or as microlevel and machine level status registers. Bit manipulating instructions are provided.
- **Condition Code Multiplexer on chip**
  Single cycle tests for any of 16 different conditions. Tests can be performed on either of the two status registers or directly on the ALU output.

DESCRIPTION

The Am2904 is designed to perform all the miscellaneous functions which are usually performed in MSI around an ALU. These include the generation of the carry-in signal to the ALU and carry lookahead unit; the interconnection of the data path, auxiliary register, and carry flip-flop during shift operations; and the storage and testing of ALU status flags. These tasks are accomplished in the Am2904 by three nearly independent blocks of logic. The carry-in is generated by a multiplexer. The shift linkages are established by four three-state multiplexers. There are two registers for storing the carry, overflow, zero, and negative status flags. The condition code multiplexer on the Am2904 can look at true or complement of any of the four status bits and certain combinations of status bits from either of the storage registers or directly from the ALU.

For additional applications refer to Chapter 4 of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

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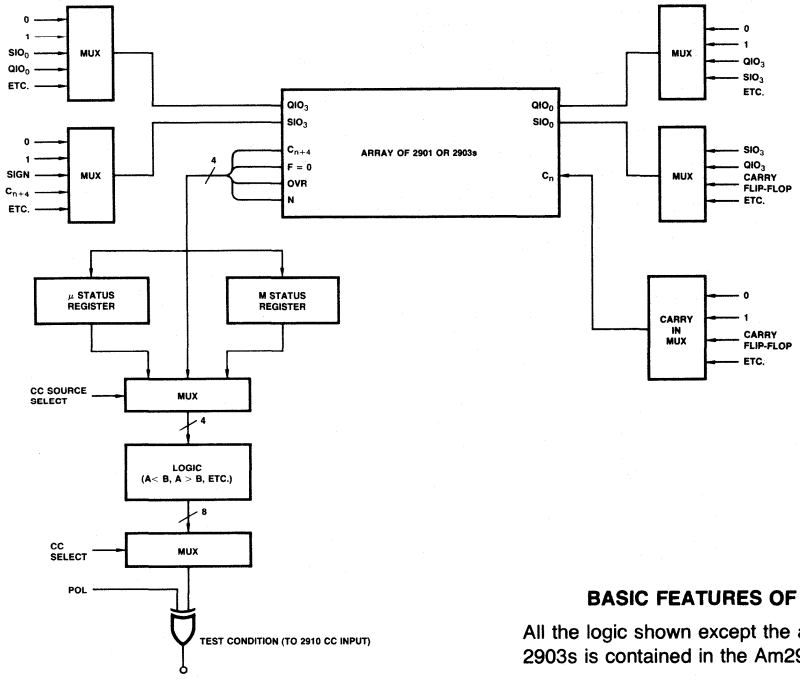
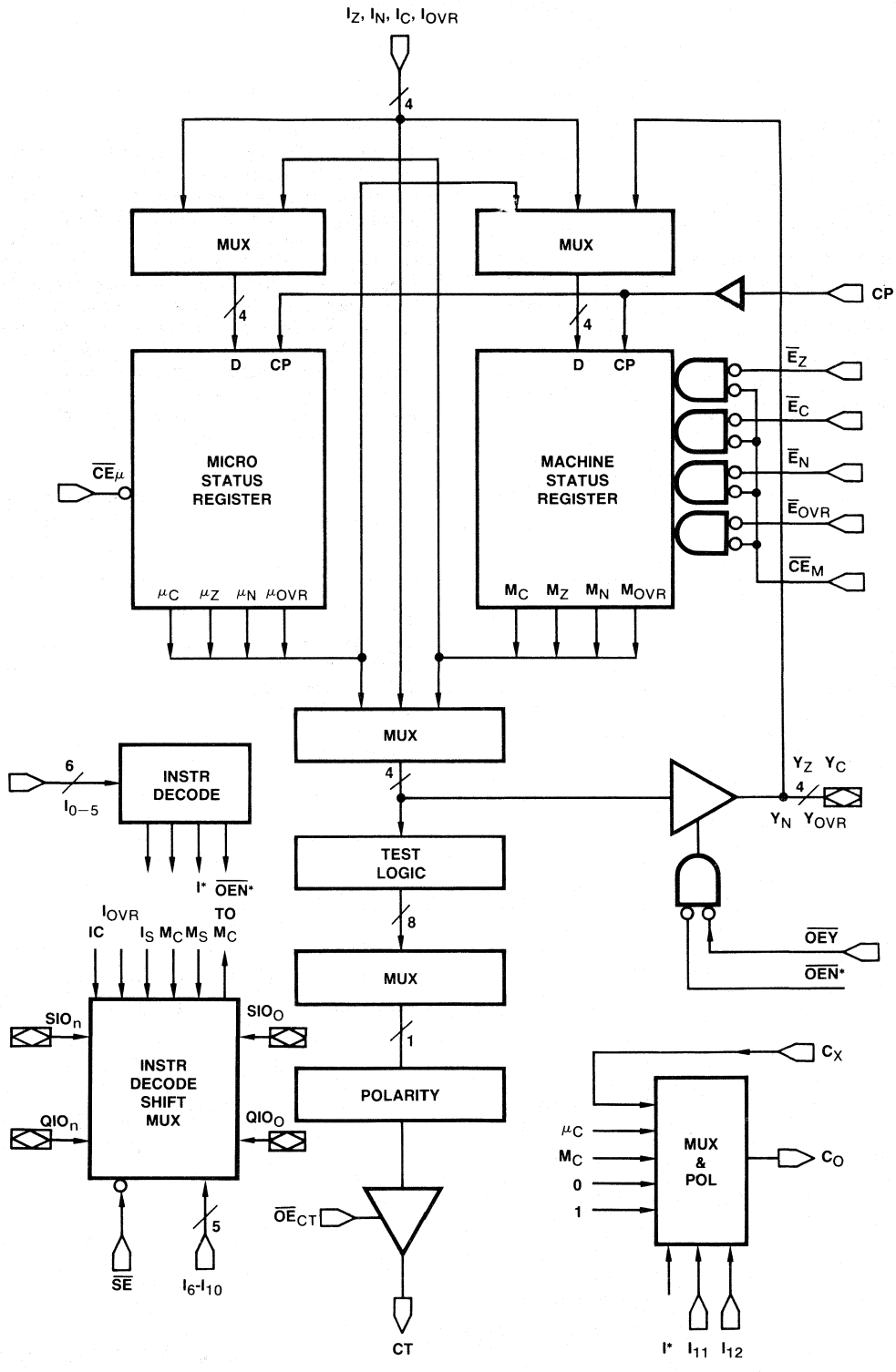


MPR-722

BASIC FEATURES OF Am2904

All the logic shown except the array of 2901s or 2903s is contained in the Am2904.

BLOCK DIAGRAM



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Am2904 ARCHITECTURE

The Am2904 Status and Shift Control Unit provides four functions which are included in all processors. These are: a) Status Register, b) Condition Code Multiplexer, c) Shift Linkages and d) Carry-in Control. The architecture and instruction codes have been designed to complement the flexibility of the 2900 Family.

Status Register

The Am2904 contains two four-bit registers which can store the status outputs of an ALU: Carry (C), Negative (N), Zero (Z), and Overflow (OVR). They are designated Micro Status Register (μSR) and Machine Status Register (MSR). Each register can be independently controlled. The registers use edge-triggered D-type flip-flops which change state on the LOW to HIGH transition of the Clock Input.

The μSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}) or from the MSR under instruction control (I_{0-5}). The bits in the μSR can also be individually set or reset under instruction control (I_{0-5}). When the $\overline{CE\mu}$ input is HIGH, the μSR is inhibited from changing, independent of the I_{0-5} inputs.

The MSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}), from the μSR, and from the four parallel input/output pins (Y_C, Y_N, Y_Z, Y_{OVR}) under instruction control (I_{0-5}) .The MSR can also be set, reset or complemented under instruction control (I_{0-5}). The bits in the MSR can be selectively updated by controlling the four bit-enable inputs ($\overline{E_Z}$, $\overline{E_N}$, $\overline{E_C}$, $\overline{E_{OVR}}$) and the $\overline{CE_M}$ input. A LOW on both the $\overline{CE_M}$ input and the bit enable input for a specific bit enables updating that bit. A HIGH on a given bit enable input prevents the corresponding bit changing in the MSR. A HIGH on $\overline{CE_M}$ prevents any bits changing in the MSR.

The four parallel bidirectional input/output pins (Y_Z, Y_N, Y_C, Y_{OVR}) allow the contents of both the μSR and the MSR to be transferred to the system data bus and also allows the MSR to be loaded from the system data bus. This capability is used to save and restore the status registers during certain subroutines and when servicing interrupts.

Condition Code Multiplexer

The Condition Code Multiplexer output, CT, can be selected from 16 different functions. These include the true and complemented state of each of the status bits and combinations of these bits to detect such conditions as "greater than", "greater than or equal to", "less than" or "less than or equal to" for unsigned or two's complement numbers.

The Am2904 can perform these tests on the contents of the μSR, the MSR or the direct status inputs, (I_Z, I_N, I_C, I_{OVR}). The CT output is used as the test ($\overline{CC}$) input of the Am2910 and is provided with an output enable, $\overline{OE_{CT}}$ to make the addition of other condition inputs to this point easy.

Shift Linkage Multiplexer

The Shift Linkage Multiplexer generates the necessary linkages to allow the ALU to perform 32 different shift and rotate functions. Both single length and double length shifts and rotates, with and without carry (M_C), are provided. When the $\overline{SE}$ input is HIGH, the four input/output pins (SIO_0, SIO_n, QIO_0, QIO_n) are disabled. The SIO_0, SIO_n, QIO_0, QIO_n pins of the Am2904 are intended to be directly connected to the RAM_0, RAM_3, Q_0 and Q_3 pins of the Am2901 or the SIO_0, SIO_3, QIO_0, QIO_3 pins of the Am2903.

Carry-In Control Multiplexer

The Carry-In Control Multiplexer generates the C_0 output which can be selected from 7 functions (0, 1, C_X, μ_C, M_C, $\overline{\mu_C}$, $\overline{M_C}$). These functions allow easy implementation of both single length and double length addition and subtraction. The C_X input is intended to be connected to the Z output of the Am2903 to facilitate execution of some of the Am2903 special instructions. The C_0 pin is to be connected to the C_n pin of the least significant Am2901 or Am2903 and the C_n pin of the Am2902A.

Am2904 INSTRUCTION SET

The Am2904 is controlled by manipulating the 13 instruction lines, I_{0-12}, together with the nine enable lines, $\overline{CE_M}$, $\overline{CE\mu}$, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, $\overline{SE}$. Most systems will save on microword bits by tying some of these lines to a fixed level or by connecting certain lines together, or by decoding microinstructions to generate appropriate Am2904 controls.

Status Registers

Instruction lines I_5, I_4, I_3, I_2, I_1, I_0 control the Status Registers. Below, these lines are referred to as two octal digits.

Micro Status Register (μSR)

The instruction codes for the Micro Status Register fall into three groups: Bit Operations, Register Operations and Load Operations (See Table 1 and Map 1). All operations require

TABLE 1. MICRO STATUS REGISTER INSTRUCTION CODES.

Bit Operations

I_{543210} Octal	μSR Operation	Comments
10	$0 \rightarrow \mu_Z$	RESET ZERO BIT
11	$1 \rightarrow \mu_Z$	SET ZERO BIT
12	$0 \rightarrow \mu_C$	RESET CARRY BIT
13	$1 \rightarrow \mu_C$	SET CARRY BIT
14	$0 \rightarrow \mu_N$	RESET SIGN BIT
15	$1 \rightarrow \mu_N$	SET SIGN BIT
16	$0 \rightarrow \mu_{OVR}$	RESET OVERFLOW BIT
17	$1 \rightarrow \mu_{OVR}$	SET OVERFLOW BIT

Register Operations

I_{543210} Octal	μSR Operation	Comments
00	$M_X \rightarrow \mu_X$	LOAD MSR TO μSR
01	$1 \rightarrow \mu_X$	SET μSR
02	$M_X \rightarrow \mu_X$	REGISTER SWAP
03	$0 \rightarrow \mu_X$	RESET μSR

Load Operations

I_{543210} Octal	μSR Operation	Comments
06, 07	$I_Z \rightarrow \mu_Z$ $I_C \rightarrow \mu_C$ $I_N \rightarrow \mu_N$ $I_{OVR} + \mu_{OVR} \rightarrow \mu_{OVR}$	LOAD WITH OVERFLOW RETAIN
30, 31 50, 51 70, 71	$I_Z \rightarrow \mu_Z$ $\overline{I_C} \rightarrow \mu_C$ $I_N \rightarrow \mu_N$ $I_{OVR} \rightarrow \mu_{OVR}$	LOAD WITH CARRY INVERT
04, 05 20-27 32-47 52-67 72-77	$I_Z \rightarrow \mu_Z$ $I_C \rightarrow \mu_C$ $I_N \rightarrow \mu_N$ $I_{OVR} \rightarrow \mu_{OVR}$	LOAD DIRECTLY FROM I_Z, I_C, I_N, I_{OVR}

Note: The above tables assume $\overline{CE}\ \mu$ is LOW.

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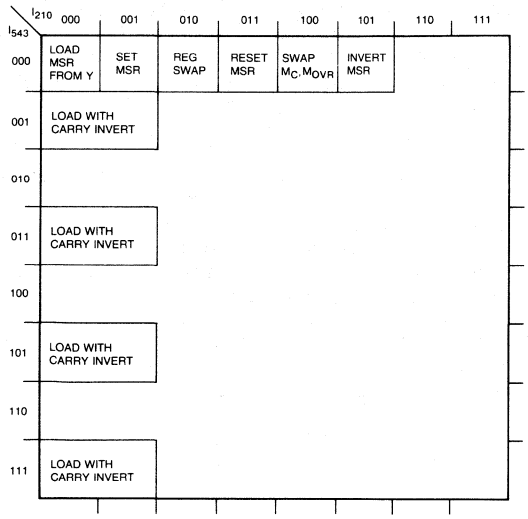
MAP 2. MACHINE STATUS REGISTER INSTRUCTION CODES.



Note 1. All unmarked locations are a load direct from I_Z, I_C, I_{OVR}, I_N.

06_8, 07_8 These instructions load the MSR directly from the 12_8-27_8 I_Z, I_C, I_N, I_{OVR} inputs.
32_8-47_8
52_8-67_8
72_8-77_8

10_8, 11_8 These instructions cause a load from the I inputs
30_8, 31_8 but invert the CARRY bit. The reason for this is
50_8, 51_8 explained more fully under the "BORROW SAVE"
70_8, 71_8 section

Condition Code Multiplexer

The four instruction lines I_3, I_2, I_1, I_0 will select one of 16 possible operations to be carried out on the input bits, the result being routed to the Conditional Test Output (CT). Eight of the operations supply an individual status bit or its complement to the CT output. Another four do more complex operations while the remaining four are the complemented results of these (See Table 4).

TABLE 3. Y OUTPUT INSTRUCTION CODES.

$\overline{OE_Y}$	I_5	I_4	Y Output	Comment
1	X	X	Z	Output Off High Impedance
O	O	X	$\mu_i \rightarrow Y_i$	See Note 1
O	1	O	$M_i \rightarrow Y_i$	
O	1	1	$I_i \rightarrow Y_i$	

Notes: 1. For the conditions:
I_5, I_4, I_3, I_2, I_1, I_0 are LOW, Y is an input.
$\overline{OE_Y}$ is "Don't Care" for this condition.
2. X is "Don't Care" condition.

TABLE 4. CONDITION CODE OUTPUT (CT) INSTRUCTION CODES.

$I_3 - 0$ HEX	I_3	I_2	I_1	I_0	$I_5 = I_4 = 0$	$I_5 = 0, I_4 = 1$	$I_5 = 1, I_4 = 0$	$I_5 = I_4 = 1$
0	0	0	0	0	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(M_N \oplus M_{OVR}) + M_Z$	$(I_N \oplus I_{OVR}) + I_Z$
1	0	0	0	1	$(\mu_N \odot \mu_{OVR}) \cdot \overline{\mu}_Z$	$(\mu_N \odot \mu_{OVR}) \cdot \overline{\mu}_Z$	$(M_N \odot M_{OVR}) \cdot \overline{M}_Z$	$(I_N \odot I_{OVR}) \cdot \overline{I}_Z$
2	0	0	1	0	$\mu_N \oplus \mu_{OVR}$	$\mu_N \oplus \mu_{OVR}$	$M_N \oplus M_{OVR}$	$I_N \oplus I_{OVR}$
3	0	0	1	1	$\mu_N \odot \mu_{OVR}$	$\mu_N \odot \mu_{OVR}$	$M_N \odot M_{OVR}$	$I_N \odot I_{OVR}$
4	0	1	0	0	μ_Z	μ_Z	M_Z	I_Z
5	0	1	0	1	$\overline{\mu}_Z$	$\overline{\mu}_Z$	$\overline{M}_Z$	$\overline{I}_Z$
6	0	1	1	0	μ_{OVR}	μ_{OVR}	M_{OVR}	I_{OVR}
7	0	1	1	1	$\overline{\mu}_{OVR}$	$\overline{\mu}_{OVR}$	$\overline{M}_{OVR}$	$\overline{I}_{OVR}$
8	1	0	0	0	$\mu_C + \mu_Z$	$\mu_C + \mu_Z$	$M_C + M_Z$	$\overline{I}_C - I_Z$ (2)
9	1	0	0	1	$\overline{\mu}_C \cdot \overline{\mu}_Z$	$\overline{\mu}_C \cdot \overline{\mu}_Z$	$\overline{M}_C \cdot \overline{M}_Z$	$I_C \cdot I_Z$ (2)
A	1	0	1	0	μ_C	μ_C	M_C	I_C
B	1	0	1	1	$\overline{\mu}_C$	$\overline{\mu}_C$	$\overline{M}_C$	$\overline{I}_C$
C	1	1	0	0	$\overline{\mu}_C + \mu_Z$	$\overline{\mu}_C + \mu_Z$	$\overline{M}_C + M_Z$	$\overline{I}_C + I_Z$
D	1	1	0	1	$\mu_C \cdot \overline{\mu}_Z$	$\mu_C \cdot \overline{\mu}_Z$	$M_C \cdot \overline{M}_Z$	$I_C \cdot \overline{I}_Z$
E	1	1	1	0	$I_N \oplus M_N$	μ_N	M_N	I_N
F	1	1	1	1	$I_N \odot M_N$	$\overline{\mu}_N$	$\overline{M}_N$	$\overline{I}_N$

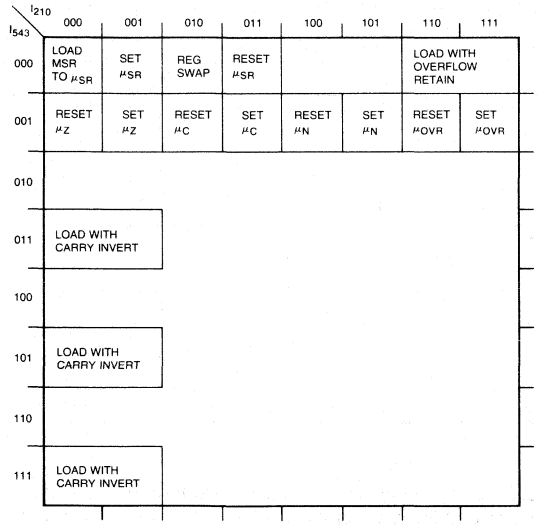
Notes: 1. $\oplus$ Represents EXCLUSIVE-OR
$\odot$ Represents EXCLUSIVE-NOR or coincidence.
2. Correct code as stated.

TABLE 5. CRITERIA FOR COMPARING TWO NUMBERS FOLLOWING "A MINUS B" OPERATION.

	For Unsigned Numbers			For 2's Complement Numbers		
		I_{3-0}			I_{3-0}	
Relation	Status	CT = H	CT = L	Status	CT = H	CT = L
A = B	Z = 1	4	5	Z = 1	4	5
A ≠ B	Z = 0	5	4	Z = 0	5	4
A ≥ B	C = 1	A	B	N ⊙ OVR = 1	3	2
A < B	C = 0	B	A	N ⊕ OVR = 1	2	3
A > B	$C \cdot \overline{Z} = 1$	D	C	$(N \odot OVR) \cdot \overline{Z} = 1$	1	0
A ≤ B	$\overline{C} + Z = 1$	C	D	$(N \oplus OVR) + Z = 1$	0	1

⊕ = Exclusive OR H = HIGH
⊙ = Exclusive NOR L = LOW
Note: For Am2910, the CC input is active LOW, so use I_{3-0} code to produce CT = L for the desired test.

MAP 1. MICRO STATUS REGISTER INSTRUCTION CODES.



Notes: 1. All unmarked locations are a load direct from I_Z, I_C, I_N, I_{OVR}.

that $\overline{CE}_\mu$ be LOW to operate.

Instruction Codes 10_8 to 17_8 are BIT operations. These operations set or reset the individual bits in the μSR.

Instruction Codes 00_8 to 03_8 are REGISTER operations. These operations affect all bits in the μSR.

00_8 This instruction loads the μSR with the contents of the MSR while loading the MSR from the Y inputs and is further explained under "INTERRUPTS".

01_8 This instruction SETS all μSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all μSR bits.

All instruction codes except those mentioned in the above two sections cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

06_8, 07_8 When a series of arithmetic operations are being executed sometimes it is not necessary to test for an overflow condition after *each* operation, but rather it is sufficient simply to know that an overflow occured during any one of the operations. Use of these instructions captures the overflow condition by loading the μSR overflow bit with the LOGICAL OR of its present state and I_{OVR}. Thus, once an overflow occurs, μOVR will remain set throughout the remaining operations.

30_8, 31_8, 50_8, 51_8, 70_8, 71_8 These instructions cause a load from the I inputs, but invert the carry bit. The reason for this is explained more fully under the "BORROW SAVE" section.

All others The remaining instructions load the μSR directly from the I_Z, I_C, I_N, I_{OVR} inputs.

Machine Status Register (MSR)

The instruction codes for the MSR fall into two groups; REGISTER Operations and LOAD Operations. All operations require that $\overline{CE}_M$ be LOW to operate (See Table 2 and Map 2).

BIT operations are accomplished by the use of Register or Load Operations with the $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ inputs selectively set LOW.

Instruction codes 00_8-03_8 and 05_8 are REGISTER operations. They affect only those bits enabled by $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$.

00_8 This instruction loads the MSR from the Y inputs while transferring the present contents to the μSR. The use of this instruction is further explained under "INTERRUPTS".

01_8 This instruction SETS all enabled MSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all enabled MSR bits.

05_8 This instruction COMPLEMENTS all enabled MSR bits.

All instruction codes except those mentioned in the above section cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

04_8 The Am2904 Shift Linkage Multiplexer allows for shifts and rotates through the MSR CARRY bit. Some machines require a shift or rotate through the OVERFLOW bit. By using this code, which swaps the contents of the MSR CARRY bit (M_C) and OVERFLOW bit (M_{OVR}), the shift or rotate can be made to appear to take place through the OVERFLOW bit. The procedure is to swap the bits, shift or rotate (any number or positions) then swap the bits again.

TABLE 2. MACHINE STATUS REGISTER INSTRUCTION CODES.

Register Operations

I_{543210} Octal	MSR Operation	Comments
00	$Y_X \rightarrow M_X$	LOAD Y_Z, Y_C, Y_N, Y_{OVR} TO MSR
01	$1 \rightarrow M_X$	SET MSR
02	$\mu_X \rightarrow M_X$	REGISTER SWAP
03	$0 \rightarrow M_X$	RESET MSR
05	$\overline{M_X} \rightarrow M_X$	INVERT MSR

Load Operations

I_{543210} Octal	MSR Operation	Comments
04	$I_Z \rightarrow M_Z$ $M_{OVR} \rightarrow M_C$ $I_N \rightarrow M_N$ $M_C \rightarrow M_{OVR}$	LOAD FOR SHIFT THROUGH OVERFLOW OPERATION
10, 11 30, 31 50, 51 70, 71	$I_Z \rightarrow M_Z$ $\overline{I_C} \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD WITH CARRY INVERT
06, 07 12-17 20-27 32-37 40-47 52-67 72-77	$I_Z \rightarrow M_Z$ $I_C \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD DIRECTLY FROM I_Z, I_C I_N, I_{OVR}

Notes: 1. The above tables assume $\overline{CE_M}$, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ are LOW.
2. A shift-through-carry instruction loads M_C irrespective of I_5-I_0.

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The more complex operations are intended to follow the calculation A-B to give an indication of which is the larger (A, B unsigned) or more positive (A, B in 2's complement form). See Table 5.

The two instruction lines I_4, I_5 select whether the μSR, the MSR or the direct inputs I_Z, I_C, I_N, I_{OVR} are used as the inputs to the Y output buffer and the CT output (see Tables 3 and 4).

Instruction codes 16_8 and 17_8 form the EXCLUSIVE – OR and the EXCLUSIVE – NOR functions of M_N and I_N. The use of these instructions is explained under "NORMALIZING".

Shift Linkage Multiplexer

The five instruction lines I_{10}, I_9, I_8, I_7, I_6 control the SHIFT LINKAGE multiplexer. All instructions set up the linkages for both the ALU shifter (RAM shifter on the Am2901A) and the Q register.

UP and DOWN shifts are decided by I_{10} which should be connected to I_8 of the Am2903's instruction lines or I_7 of the Am2901's instruction lines. A wide range of input and output connections are provided, allowing for single or double length shifting or rotating with or without the use of the MSR CARRY or SIGN bits (See Table 7).

In the following discussion of some of the shifts the instruction codes are given as two octal digits AB; A represents I_{10}, I_9, B represents I_8, I_7, I_6.

When adding and down shifting on the same microcycle, (i.e. when doing multiplication or averaging) the shifter input must be the present CARRY, I_C, rather than the carry resulting from the last cycle (M_C). Instruction Code 13_8 accomplishes this for unsigned arithmetic. For 2's complement arithmetic, the required shifter input is: $I_N \oplus I_{OVR}$. This is provided by Instruction Code 16_8.

Instruction Codes 14_8, 15_8, 17_8 provide the RIGHT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

Instruction Codes 34_8, 35_8, 37_8 provide the LEFT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

The shift outputs are in the high impedance state unless $\overline{SE}$ is LOW.

Loading of the M_C bit by a shift operation overrides any loading or holding of the M_C bit by MSR Instructions (I_{0-5}, $\overline{CE_M}$ and $\overline{E_C}$).

"CARRY-IN" Control Multiplexer

The two instruction lines I_{12}, I_{11} control the source of the CARRY output (C_0).

When $I_{12} = 0$ $\quad C_0 = I_{11}$

When $I_{12} = 1$ and $I_{11} = 0$, the external carry input C_X is presented to the carry output.

When $I_{12} = I_{11} = 1$ the carry output is selected from μ_C, $\overline{\mu_C}$, M_C or $\overline{M_C}$ as defined by I_5, I_3, I_2, I_1 (See Table 6).

TABLE 6. CARRY-IN CONTROL MULTIPLEXER INSTRUCTION CODES.

I_{12}	I_{11}	I_5	I_3	I_2	I_1	C_0
0	0	X	X	X	X	0
0	1	X	X	X	X	1
1	0	X	X	X	X	C_X
1	1	0	0	X	X	μ_C
1	1	0	X	1	X	μ_C
1	1	0	X	X	1	μ_C
1	1	0	1	0	0	$\overline{\mu}_C$
1	1	1	0	X	X	M_C
1	1	1	X	1	X	M_C
1	1	1	X	X	1	M_C
1	1	1	1	0	0	$\overline{M}_C$

APPLICATIONS INFORMATION

Borrow – Save

One of the capabilities of the Am2900 Family is the complete emulation of other processing machines. One requirement of an emulator is that, when a calculation is being performed, not only must the answer obtained from the Am2900 chips be the same as that from the machine being emulated, but after each machine level instruction, the status bits must be indentical.

There are alternative methods for subtracting in a digital machine and the state of the CARRY after the calculation depends on the method. For instance, the subtraction of 0100 from 1010 by the 2's complement add method generates a result of 0110 with a CARRY. Direct subtraction however, yields an answer of 0110 with no BORROW.

Many machines store the state of the CARRY for subtract operations, and this is the recommended method for maximum effective use of the Am2904, but, to allow those machines which store the BORROW to be efficiently emulated, the Am2904 has allocated special instructions. Using these codes causes the CARRY bit to be inverted before storage in the status registers and also re-inverts these status bits before using them as carry inputs. These codes are 10_8, 11_8, 30_8, 31_8, 50_8, 51_8, 70_8, 71_8 (I_{5-0}).

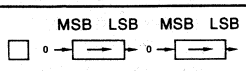
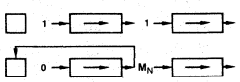
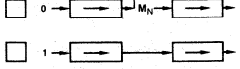
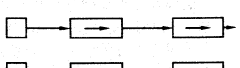
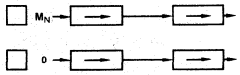
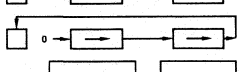
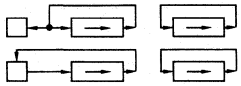
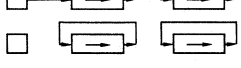
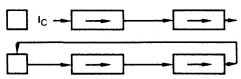
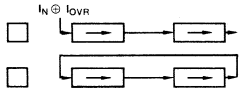
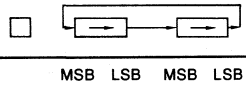
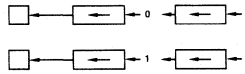
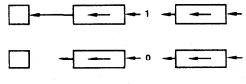
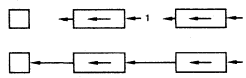
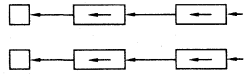
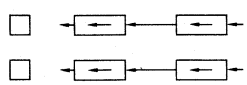
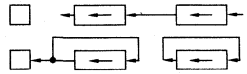
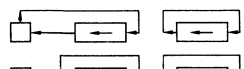
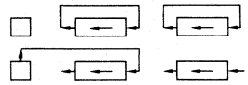
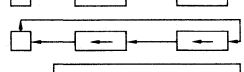
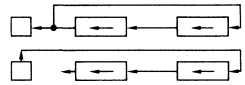
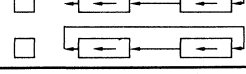
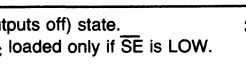
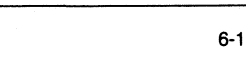
Notice that when these codes are used to load the inverted CARRY to either of the status registers, the CT output selected by the Condition Code Multiplexer assumes the CARRY is inverted and still defines whether $A > B$ or $A \leq B$ (See Table 4).

Similarly, when doing a compare on a machine which saves the borrow, testing for $A > B$, $A \leq B$ forces the complement of the CARRY to be stored in the status registers (See Tables 1 and 2).

Normalizing

Normalizing is the process of stripping off all leading sign bits until the two most significant bits are complementary. The Am2904 facilitates both single and double length normalization in the Am2901 and the Am2903. When using the NORMALIZE special instructions with the Am2903, the EXCLUSIVE – OR of the most significant two bits is generated at the C_{n+4} pin of the most significant Am2903. The EXCLUSIVE – OR of the two bits next to the most significant bit is also generated at the OVR pin. The procedure for normalizing then is to loop on the normalize instruction with a branch condition on the C_{n+4} state or the OVR state, depending on the architecture employed. The C_{n+4} or OVR output is routed to the Am2910 CC input through the Am2904 Condition Code multiplexer. As the contents of the status registers always refers to the last cycle, not the present one, the last operation in Normalizing is to downshift, bringing the sign bit (M_N) back into the most significant bit position. This is achieved using the shift operations 05_8 (I_{10-6}) for double length normalizing,

TABLE 7. SHIFT LINKAGE MULTIPLEXER INSTRUCTION CODES.

I_{10}	I_9	I_8	I_7	I_6	M_C RAM Q	SIO_0	SIO_n	QIO_0	QIO_n	Loaded into M_C
0	0	0	0	0		Z	0	Z	0	
0	0	0	0	1		Z	1	Z	1	
0	0	0	1	0		Z	0	Z	M_N	SIO_0
0	0	0	1	1		Z	1	Z	SIO_0	
0	0	1	0	0		Z	M_C	Z	SIO_0	
0	0	1	0	1		Z	M_N	Z	SIO_0	
0	0	1	1	0		Z	0	Z	SIO_0	
0	0	1	1	1		Z	0	Z	SIO_0	QIO_0
0	1	0	0	0		Z	SIO_0	Z	QIO_0	SIO_0
0	1	0	0	1		Z	M_C	Z	QIO_0	SIO_0
0	1	0	1	0		Z	SIO_0	Z	QIO_0	
0	1	0	1	1		Z	I_C	Z	SIO_0	
0	1	1	0	0		Z	M_C	Z	SIO_0	QIO_0
0	1	1	0	1		Z	QIO_0	Z	SIO_0	QIO_0
0	1	1	1	0		Z	$I_N \oplus I_{OVR}$	Z	SIO_0	
0	1	1	1	1		Z	QIO_0	Z	SIO_0	
1	0	0	0	0		0	Z	0	Z	SIO_n
1	0	0	0	1		1	Z	1	Z	SIO_n
1	0	0	1	0		0	Z	0	Z	
1	0	0	1	1		1	Z	1	Z	
1	0	1	0	0		QIO_n	Z	0	Z	SIO_n
1	0	1	0	1		QIO_n	Z	1	Z	SIO_n
1	0	1	1	0		QIO_n	Z	0	Z	
1	0	1	1	1		QIO_n	Z	1	Z	
1	1	0	0	0		SIO_n	Z	QIO_n	Z	SIO_n
1	1	0	0	1		M_C	Z	QIO_n	Z	SIO_n
1	1	0	1	0		SIO_n	Z	QIO_n	Z	
1	1	0	1	1		M_C	Z	0	Z	
1	1	1	0	0		QIO_n	Z	M_C	Z	SIO_n
1	1	1	0	1		QIO_n	Z	SIO_n	Z	SIO_n
1	1	1	1	0		QIO_n	Z	M_C	Z	
1	1	1	1	1		QIO_n	Z	SIO_n	Z	

Notes: 1. Z = High impedance (outputs off) state.
2. Outputs enabled and M_C loaded only if $\overline{SE}$ is LOW.
3. Loading of M_C from I_{10-6} overrides control from I_{5-0}, $\overline{CE}_M$, $\overline{E}_C$.

and 02_8 for single length normalizing. For more details regarding normalizing with the Am2903 see the Am2903 data sheet.

The Am2901 does not have the EXCLUSIVE – OR gates to help with normalizing, so the Am2904 includes in the Condition Code multiplexer the EXCLUSIVE – OR and EXCLUSIVE – NOR functions of M_N (the sign bit resulting from the last operation) and I_N (the sign bit resulting from the present operation).

Interrupts

Some machines allow interrupts only at the machine instruction level while others allow them at the microinstruction level. The Am2904 is designed to handle both cases.

When the machine is interrupted, it is necessary to store the contents of either the MSR (machine instruction level interrupts) or both the status registers (micro instruction level interrupts) into an external store. This transfer is intended to take place over the Y input/output pins (See Table 3).

After the interrupt has been serviced the registers must be restored to their pre-interrupt state. This is accomplished by two operations of instruction 00_8 (I_{5-0}) which loads the MSR from the Y inputs while loading the μSR from the MSR. Thus, the pre-interrupt contents of the μSR are first loaded to the MSR (first instruction 00_8), then this data is transferred to the μSR while the MSR is restored to its pre-interrupt state (second instruction 00_8).

In controllers and some other microprogrammed machines the applications program itself is often in the microprogram memory; that is, there is no macroinstruction set. These machines require only a microstatus register since there is no separate machine status. The MSR in the Am2904 can be used as a one-level stack on the microstatus register. When an interrupt occurs, the μSR and the MSR are simply swapped ($I_{5-0} = 02_8$).

PIN DEFINITIONS

I_Z Zero status input pin, intended for connection to the Z outputs of the Am2903 or the F = 0 ouputs of the Am2901.

I_C Carry status input pin, intended for connection to the C_{n+4} output of the most significant ALU slice.

I_N Sign status input pin, intended for connection to the most significant ALU slice. The connection is to the N pin on the Am2903, and the F_3 pin on the Am2901.

I_{OVR} Overflow status input pin, intended for connection to the OVR pin on the most significant ALU slice.

I_{0-12} The thirteen instruction pins which select the operation the Am2904 is to perform.

$\overline{CE_M}$ This pin, used in conjunction with $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ acts as the overall enable for the machine status register. When the pin is LOW, MSR bits may be modified, according to the states of $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$. When HIGH, the MSR will retain the present state, regardless of the state of $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$.

$\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ These pins, when LOW, enable the corresponding bits in the Machine Status Register. When HIGH, they will prevent the corresponding bits from changing state. By using these pins together with the $\overline{CE_M}$ pin, MSR bits can be selectively modified.

$\overline{CE_\mu}$ This pin, when LOW, enables all four bits of the Micro Status Register. When this pin is HIGH, the μSR will not change state.

Y_Z, Y_C, Y_N, Y_{OVR} These pins form a three-state bidirectional bus over which MSR and μSR status can be read out or the MSR can be loaded in parallel.

$\overline{OE_Y}$ When LOW, this pin enables the Y pins as outputs. When HIGH, the Y outputs are in the high impedance state.

CT The conditional test output. The output of the Condition Code multiplexer appears here.

$\overline{OE_{CT}}$ When this pin is LOW, the CT pin is active. When HIGH the CT pin is in the high impedance state.

SIO_0, SIO_n QIO_0 QIO_n These pins complete the linking for the various shift and rotate conditions. SIO_0 is intended for connection to the SIO_0 pin of the least significant Am2903 slice (RAM_0 for Am2901). SIO_n connects to the SIO_3 pin of the most significant Am2903 slice, (RAM_3 for Am2901). QIO_0 connects to the QIO_0 pin of the least significant Am2903 slice (QIO_0 for Am2901) and QIO_n connects to the QIO_3 pin of the most significant Am2903 slice (Q_3 for Am2901).

$\overline{SE}$ This pin controls the state of the shift outputs. When LOW, the shift outputs are enabled. When HIGH, the shift outputs are in the high impedance state.

C_0 This pin is the output of the Carry In control multiplexer. It connects to the C_n input of the least significant ALU slice, and the C_n input of the Am2902A.

C_X This pin is used as an input to the Carry In Control multiplexer which can route it to the C_0 pin. The C_X pin is intended for connection to the Z output of the Am2903 to facilitate some of the Am2903 special instructions.

CP The clock input to the device. The μSR and MSR are modified on the LOW to HIGH transition of the clock input. All other portions of the Am2904 are combinational and are unaffected by CP.

ORDERING INFORMATION

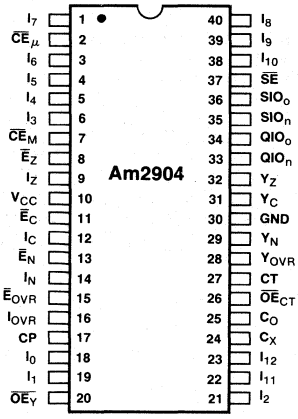
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2904PC	P-40	C	C-1
AM2904DC	D-40	C	C-1
AM2904DC-B	D-40	C	B-2 (Note 4)
AM2904DM	D-40	M	C-3
AM2904DM-B	D-40	M	B-3
AM2904FM	F-42	M	C-3
AM2904FM-B	F-42	M	B-3
AM2904XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2904XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

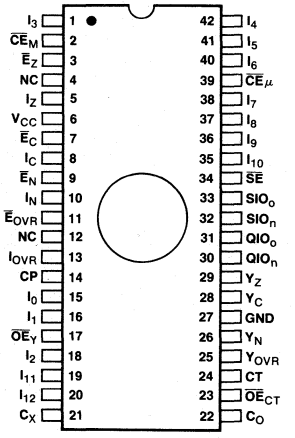
CONNECTION DIAGRAMS
Top Views

DIP



MPR-723

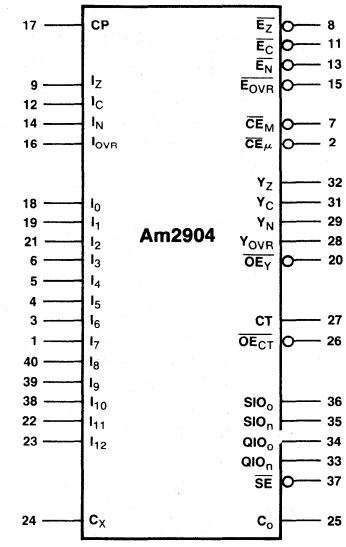
Flat Package



MPR-724

Note: Pin 1 is marked for orientation.
NC = No Connection.

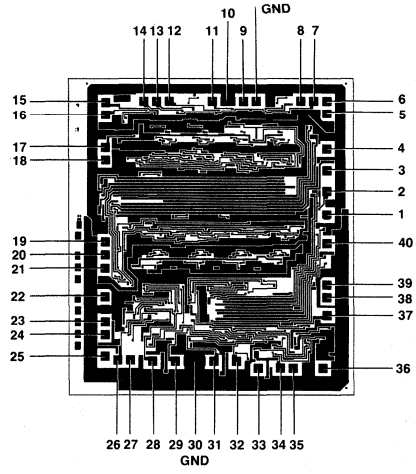
LOGIC SYMBOL
(DIP)



MPR-725

V_{CC} = Pin 10
GND = Pin 30

Am2904 Metallization and Pad Layout



DIE SIZE 0.140" X 0.161"
Pad Numbers correspond to DIP pinout

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Case) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2904PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V, MAX. = 5.25V)
Am2904DM, FM	MIL	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V, MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_Z, Y_C, Y_N, Y_{OVR}		2.4			Volts
			I_{OH} = −0.8mA SIO_o, SIO_n, QIO_o QIO_n, CT, CO		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_Z, Y_C Y_N, Y_{OVR}	I_{OL} = 24mA (Com'l)			0.5	
				I_{OL} = 16mA (MIL)			0.5	Volts
			SIO_o, QIO_o, CT, SIO_n, QIO_n, CO	I_{OL} = 8mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	CP				−0.7	mA
			$\overline{CE_m}$, $\overline{CE_\mu}$				−1.8	
			I_Z, I_C, I_N, I_{OVR}				−1.2	
			I_0-I_{12}, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$ $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, C_X, Y_Z, Y_C, Y_N, Y_{OVR}				−0.45	
			$\overline{SE}$, SIO_o, SIO_n, QIO_o, QIO_n				−1.35	
I_{IH}	Input HIGH Current	V_{CC} = MAX. V_{IN} = 2.7V	CP, I_0-I_{12}, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, C_X				20	μA
			$\overline{CE_m}$, $\overline{CE_\mu}$				80	
			I_Z, I_C, I_N, I_{OVR}, $\overline{SE}$				60	
			SIO_o, SIO_n, QIO_o, QIO_n				110	
			Y_Z, Y_C, Y_N, Y_{OVR}				70	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	CT	V_O = 2.4			50	μA
				V_O = 0.5			−50	
			SIO_o, SIO_n, QIO_o, QIO_n (Note 4)	V_O = 2.4			110	
				V_O = 0.5			−1350	
			Y_Z, Y_C, Y_N, Y_{OVR} (Note 4)	V_O = 2.4			70	
				V_O = 0.5			−450	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75V, V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX.		T_A = 25°C		180	296	mA
			Am2904PC, DC	T_A = 0°C to +70°C			318	
				T_A = +70°C			262	
			Am2904DM, FM	T_C = −55°C to +125°C			342	
				T_C = +125°C			222	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
5. "MIL" = Am2904 XM, DM, FM. "COM'L" = Am2904 XC, PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

SWITCHING CHARACTERISTICS

The tables below define the Am2904 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns. All outputs have maximum DC loading.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to +5.25V, C_L = 50pF)

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	14	5
I_C (I_1 I_2 I_3 = 001)	27	5
I_C (I_1 I_2 I_3 = 001)	14	5
$\overline{CE}_\mu$	18	3
$\overline{CE}_M$	23	3
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$ $\overline{E}_{OVR}$	22	3(b)
I_0-I_5	41	1
I_6-I_{10}	40	1
$\overline{SE}$	36	0
Y_Z, Y_C, Y_N, Y_{OVR} ($I_{0\text{-}5}$ = LOW)	15	5
SIO_o, SIO_n, QIO_o, QIO_n	20	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z I_C I_N I_{OVR}	Y_Z Y_C Y_N Y_{OVR}	38
CP	Y_Z, Y_C, Y_N, Y_{OVR}	41
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	35
I_Z, I_C, I_N, I_{OVR}	CT	33
CP	CT	36
I_0-I_5	CT	33
C_X	C_O	20
CP	C_O	27
$I_{1, 2, 3, 5, 11, 12}$	C_O	39
SIO_n, QIO_n	SIO_o	19
SIO_o, QIO_o	SIO_n	19
I_C, I_N, I_{OVR}	SIO_n	26
SIO_n, QIO_n	QIO_o	19
SIO_o, QIO_o	QIO_n	19
CP	SIO_o, SIO_n QIO_o, QIO_n	30
I_6-I_{10}	SIO_o, SIO_n QIO_o, QIO_n	26

C. Clock Requirements (ns)

Minimum Clock LOW Time	20
Minimum Clock HIGH Time	20

D. Enable/Disable Times (ns)

C_L = 5.0pF for output disable tests

From (Input)	To (Output)	Enable	Disable
OE_{CT}	CT	23	18
SE	SIO_o, SIO_n QIO_o, QIO_n	30	12
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	39	29
OE_Y	Y_Z, Y_C, Y_N, Y_{OVR}	26	21
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	28	40

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to +5.5V, C_L = 50pF)

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	15	5
I_C (I_1 I_2 I_3 = 001)	28	5
I_C (I_1 I_2 I_3 = 001)	15	5
$\overline{CE}_\mu$	20	3
$\overline{CE}_M$	23	4
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$ $\overline{E}_{OVR}$	23	4
I_0-I_5	48	2
I_6-I_{10}	44	2
$\overline{SE}$	40	0
Y_Z, Y_C, Y_N, Y_{OVR} ($I_{0\text{-}5}$ = LOW)	16	6
SIO_o, SIO_n, QIO_o, QIO_n	20	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z I_C I_N I_{OVR}	Y_Z Y_C Y_N Y_{OVR}	40
CP	Y_Z, Y_C, Y_N, Y_{OVR}	45
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	38
I_Z, I_C, I_N, I_{OVR}	CT	44
CP	CT	40
I_0-I_5	CT	41
C_X	C_O	22
CP	C_O	28
$I_{1, 2, 3, 5, 11, 12}$	C_O	42
SIO_n, QIO_n	SIO_o	20
SIO_o, QIO_o	SIO_n	20
I_C, I_N, I_{OVR}	SIO_n	29
SIO_n, QIO_n	QIO_o	20
SIO_o, QIO_o	QIO_n	20
CP	SIO_o, SIO_n QIO_o, QIO_n	32
I_6-I_{10}	SIO_o, SIO_n QIO_o, QIO_n	31

C. Clock Requirements (ns)

Minimum Clock LOW Time	25
Minimum Clock HIGH Time	25

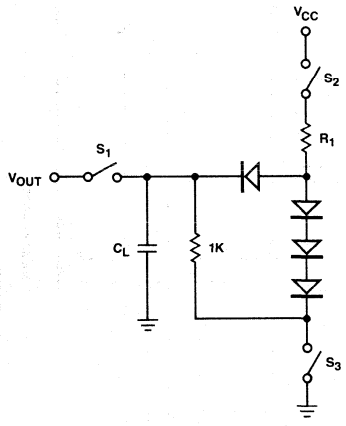
D. Enable/Disable Times (ns)

C_L = 5.0pF for output disable tests

From (Input)	To (Output)	Enable	Disable
OE_{CT}	CT	25	18
SE	SIO_o, SIO_n QIO_o, QIO_n	35	16
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	43	32
OE_Y	Y_Z, Y_C, Y_N, Y_{OVR}	28	23
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	30	41

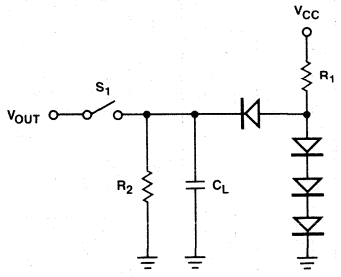
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2904

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2904

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
25	C_0	B	470	3K
27	CT	A	430	1K
28	Y_{OVR}	A	220	1K
29	Y_N	A	220	1K
31	Y_C	A	220	1K
32	Y_Z	A	220	1K
33	QIO_N	A	430	1K
34	QIO_0	A	430	1K
35	SIO_N	A	430	1K
36	SIO_0	A	430	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

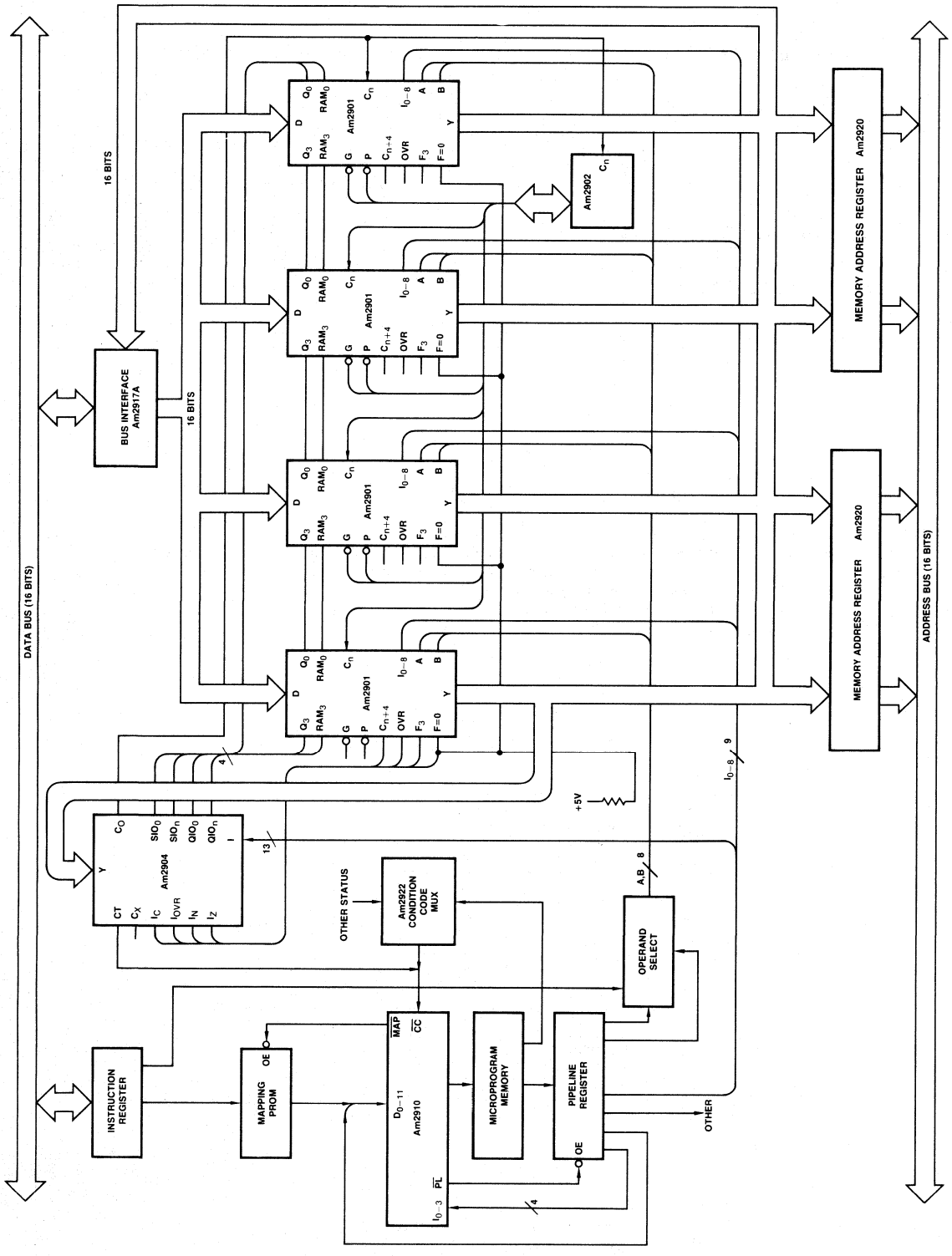


Figure 1. Typical Application of Am2904 with Am2901.

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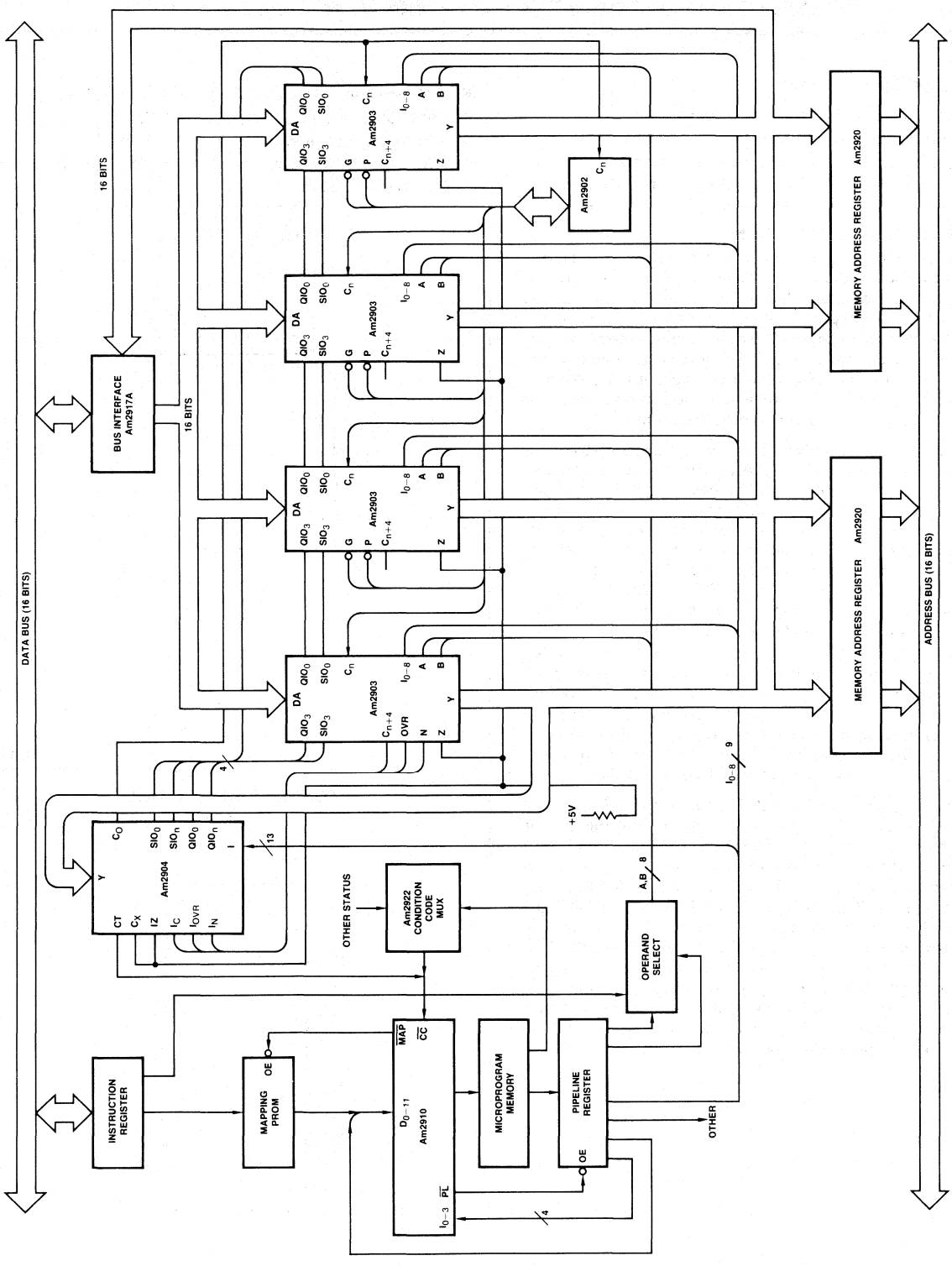

Figure 2. Typical Application of Am2904 with Am2903.

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Am2905

Quad Two-Input OC Bus Transceiver With Three-State Receiver

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

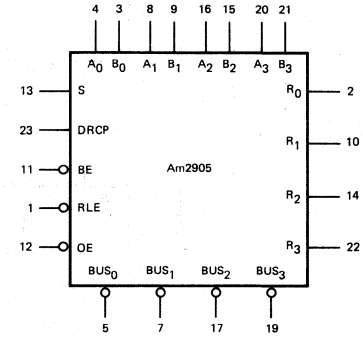
The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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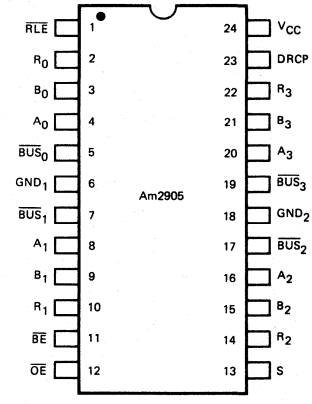
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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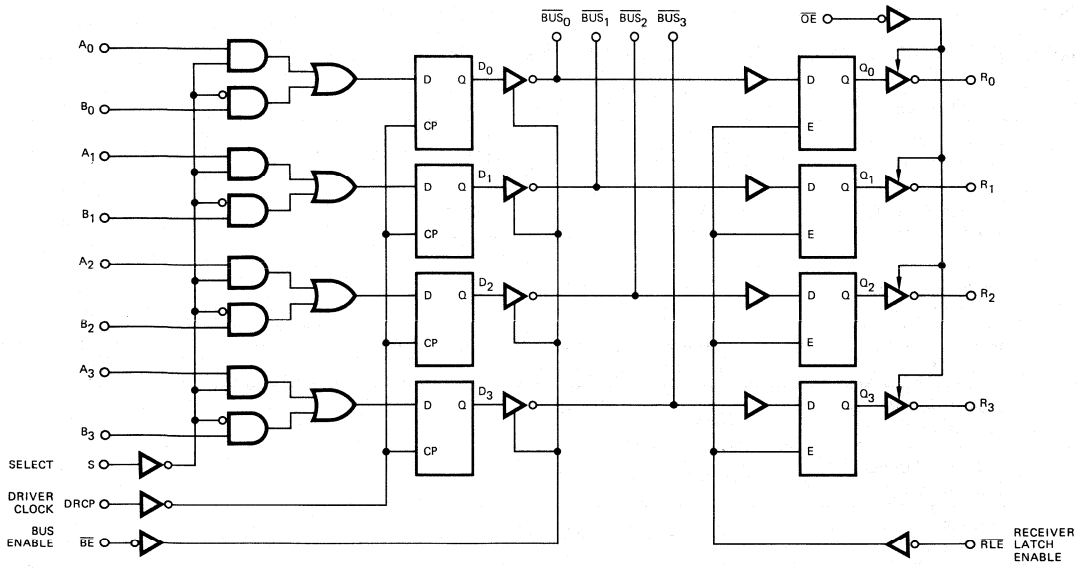
LOGIC DIAGRAM



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6

MAXIMUM RATINGS (Above which the useful life may be impaired)

torage Temperature	−65°C to +150°C
emperature (Ambient) Under Bias	−55°C to +125°C
upply Voltage to Ground Potential	−0.5V to +7V
C Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
C Input Voltage	−0.5V to +7V
C Output Current, Into Outputs (Except Bus)	30mA
C Output Current, Into Bus	200mA
C Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

he following conditions apply unless otherwise noted:

m2905XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
m2905XM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

arameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2905XM MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

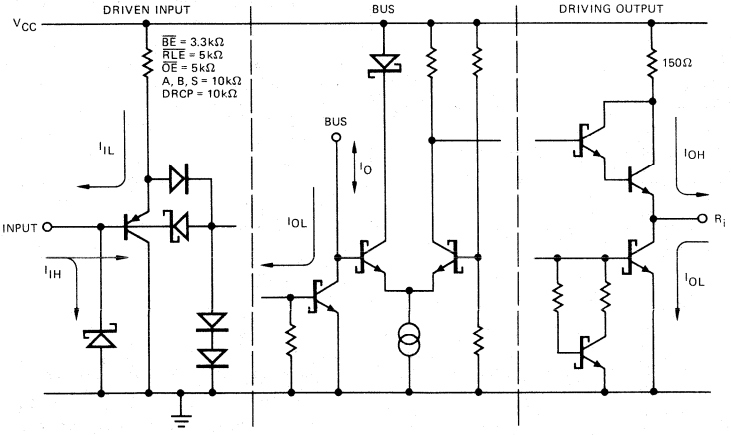
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	$V_{CC} = V_{IN}$, $V_{IN} = V_{IL}$ or V_{IH}	MIL, $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6$mA	2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA		0.27	0.4	Volts
			I_{OL} = 8mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$V				100	μA
I_O	Receiver Off-State Output Current	V_{CC} = MAX.	$V_O = 2.4$V			20	μA
			$V_O = 0.4$V			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX.		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND			69	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2905XM Min.	Am2905XM Typ. (Note 2)	Am2905XM Max.	Am2905XC Min.	Am2905XC Typ. (Note 2)	Am2905XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Input (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{ZH}	Output Control to Receiver Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Receiver Output			14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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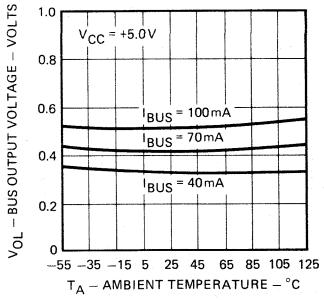
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



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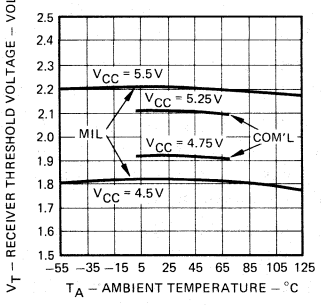
Receiver Threshold Variation Versus Ambient Temperature



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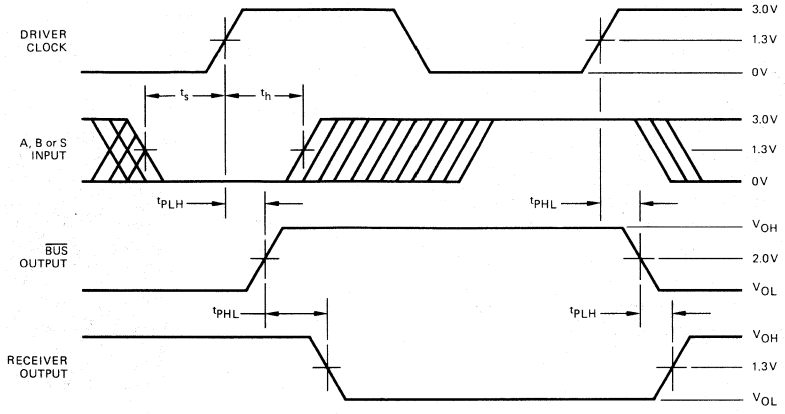
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

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FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2905PC	P-24	C	C-1
AM2905DC	D-24	C	C-1
AM2905DC-B	D-24	C	B-1
AM2905DM	D-24	M	C-3
AM2905DM-B	D-24	M	B-3
AM2905FM	F-24-1	M	C-3
AM2905FM-B	F-24-1	M	B-3
AM2905XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2905XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

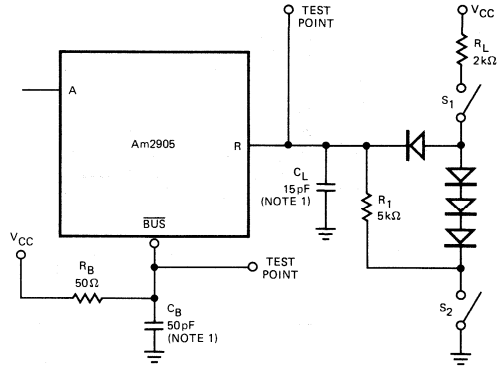
$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

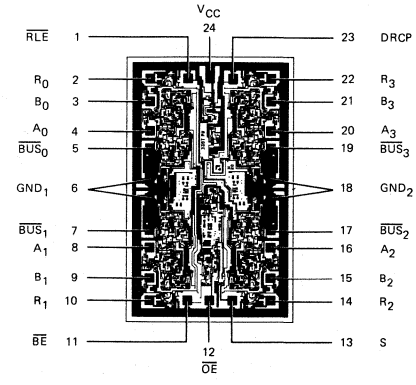
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



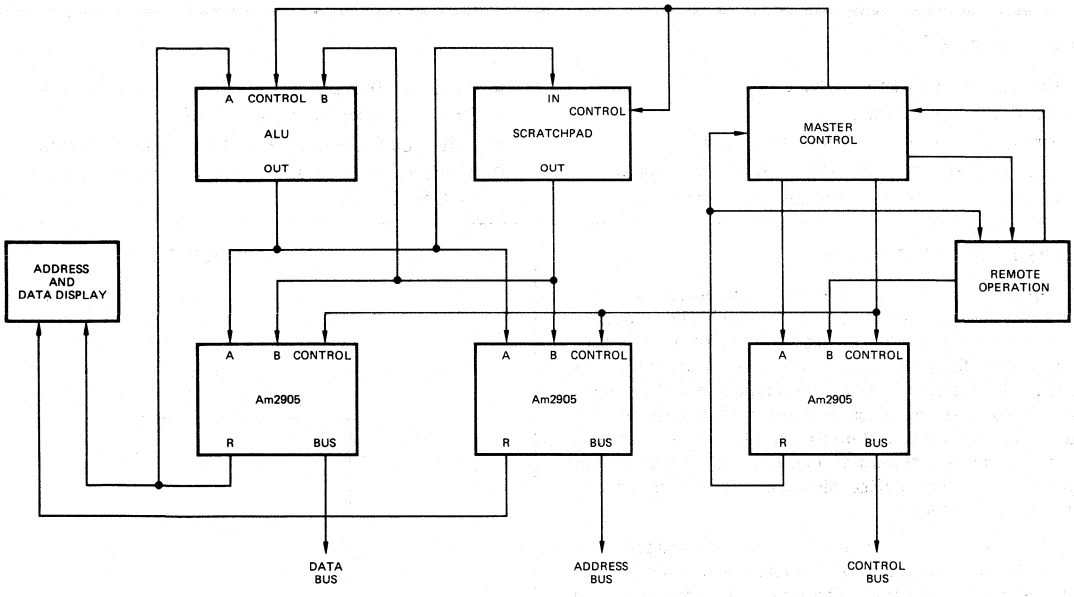
MPR-070

Metallization and Pad Layout



DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

MPR-071

6

Am2906

Quad Two-Input OC Bus Transceiver With Parity

Distinctive Characteristics

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance witl MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

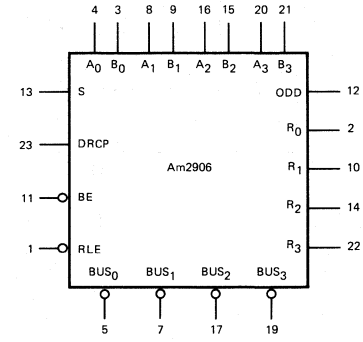
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

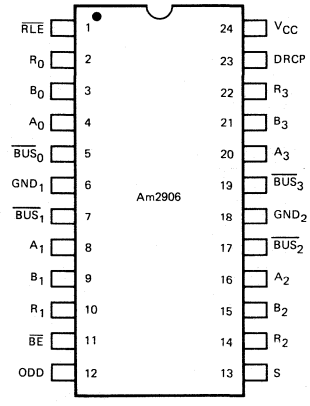
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-073

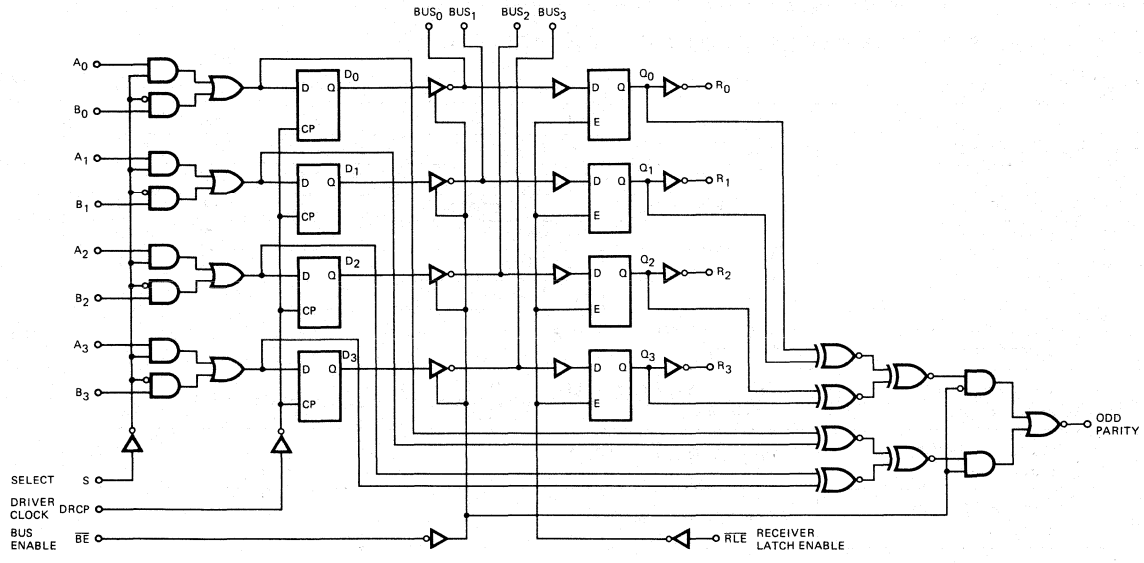
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-074

LOGIC DIAGRAM



MPR-075

6

MAXIMUM RATINGS (Above which the useful life may be impaired)

torage Temperature	−65°C to +150°C
emperature (Ambient) Under Bias	−55°C to +125°C
upply Voltage to Ground Potential	−0.5V to +7V
C Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
C Input Voltage	−0.5V to +5.5V
C Output Current, Into Outputs (Except Bus)	30mA
C Output Current, Into Bus	200mA
C Input Current	−30mA to +5.0mA

ECTRICAL CHARACTERISTICS

e following conditions apply unless otherwise noted:

12906XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
12906XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

JS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

rameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2906XM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. 4.5V V_{CC} MAX. = 5.5V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

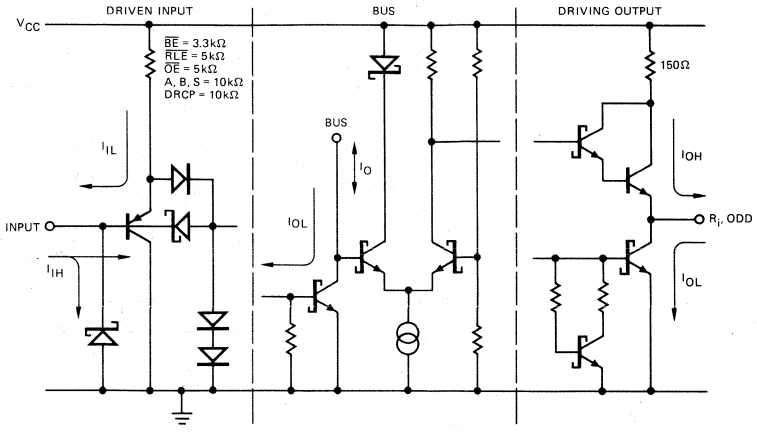
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	MIL	$I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L	$I_{OH} = -2.6mA$	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$ $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				72	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2906XM Min.	Am2906XM Typ. (Note 2)	Am2906XM Max.	Am2906XC Min.	Am2906XC Typ. (Note 2)	Am2906XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs-(A or B)	C_L = 15pF R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Inputs (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

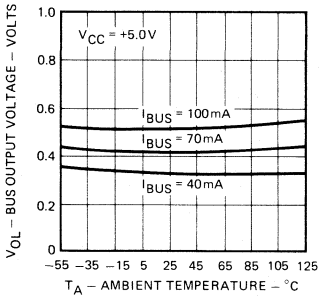


Note: Actual current flow direction shown.

MPR-076

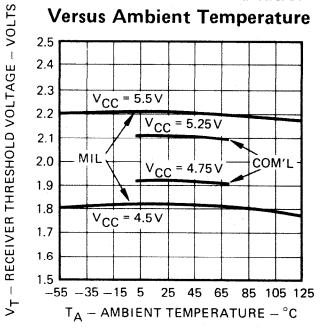
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



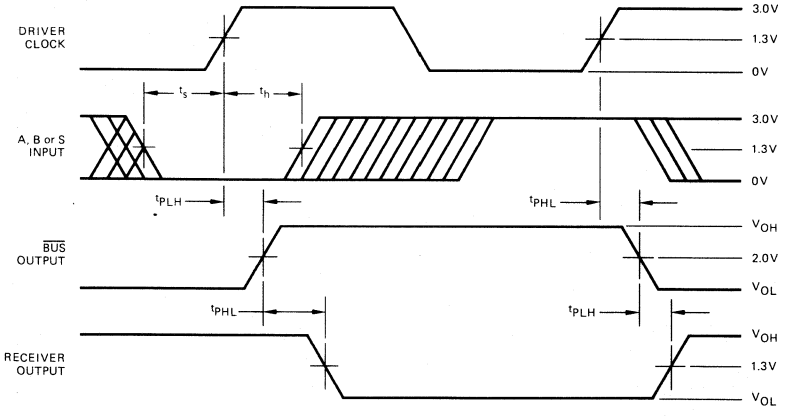
MPR-077

Receiver Threshold Variation Versus Ambient Temperature



MPR-078

SWITCHING WAVEFORMS

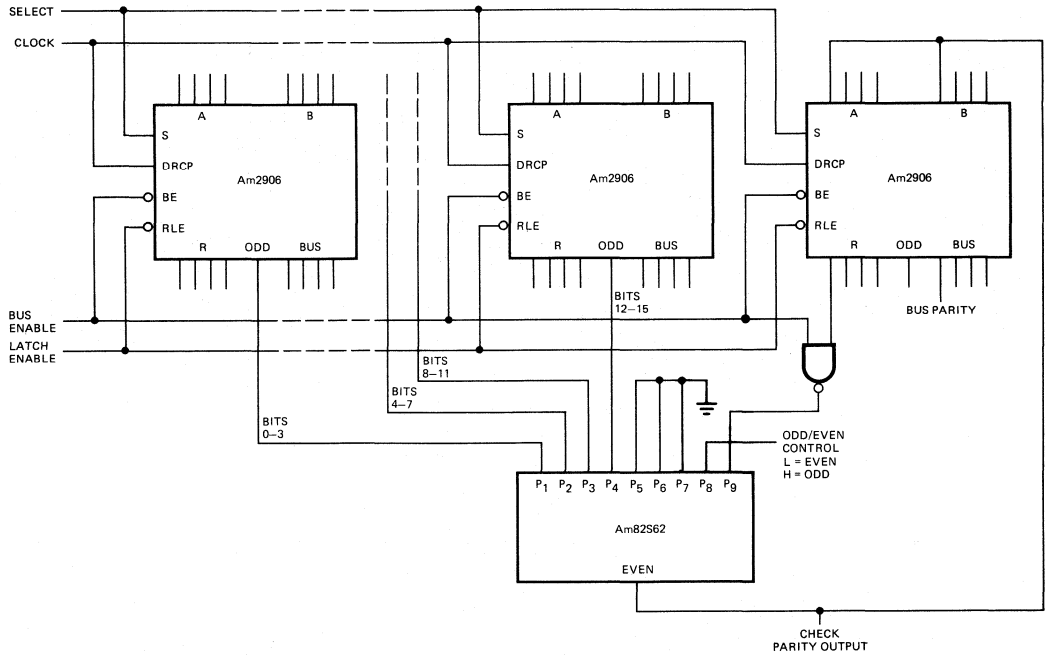


Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-079

6

APPLICATIONS



Generating or checking parity for 16 data bits.

MPR-08

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS_i}$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2906PC	P-24	C	C-1
AM2906DC	D-24	C	C-1
AM2906DC-B	D-24	C	B-1
AM2906DM	D-24	M	C-3
AM2906DM-B	D-24	M	B-3
AM2906FM	F-24-1	M	C-3
AM2906FM-B	F-24-1	M	B-3
AM2906XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2906XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

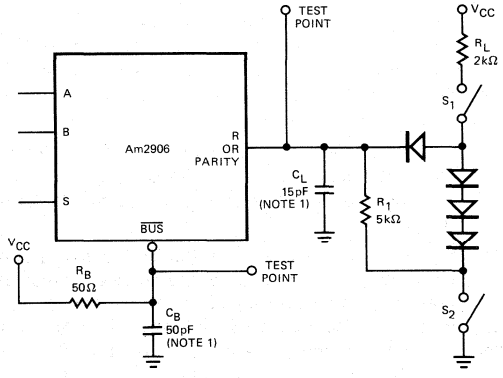
$\overline{BUS_0}$, $\overline{BUS_1}$ $\overline{BUS_2}$, $\overline{BUS_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

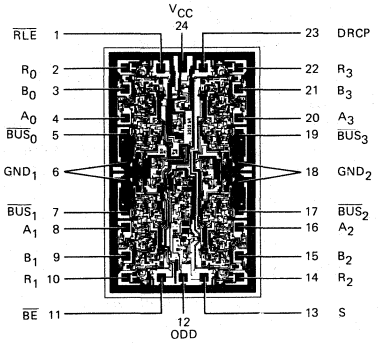
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



MPR-080

Metallization and Pad Layout



DIE SIZE 0.080" X 0.130"

Am2907 • Am2908

Quad Bus Transceivers with Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100mA at 0.8V max.
- Internal odd 4-bit parity checker/generator
- Am2907 has 2.0V input receiver threshold; Am2908 is "DEC Q or LSI-II bus compatible" with 1.5V receiver threshold
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced Low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2907 and Am2908 are high-performance bus transceivers intended for bipolar or MOS microprocessor system applications. The Am2908 is Digital Equipment Corporation "Q or LSI-II bus compatible" while the Am2907 features a 2.0V receiver threshold. These devices consist of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The devices also contain a four-bit odd parity checker/generator.

These LSI bus transceivers are fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

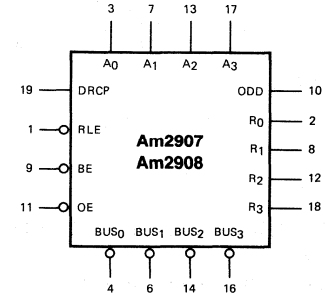
The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted form driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 and Am2908 feature a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

The Am2907 has receiver threshold typically of 2.0V while the Am2908 threshold is typically 1.5V.

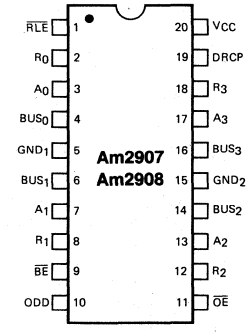
LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

MPR-083

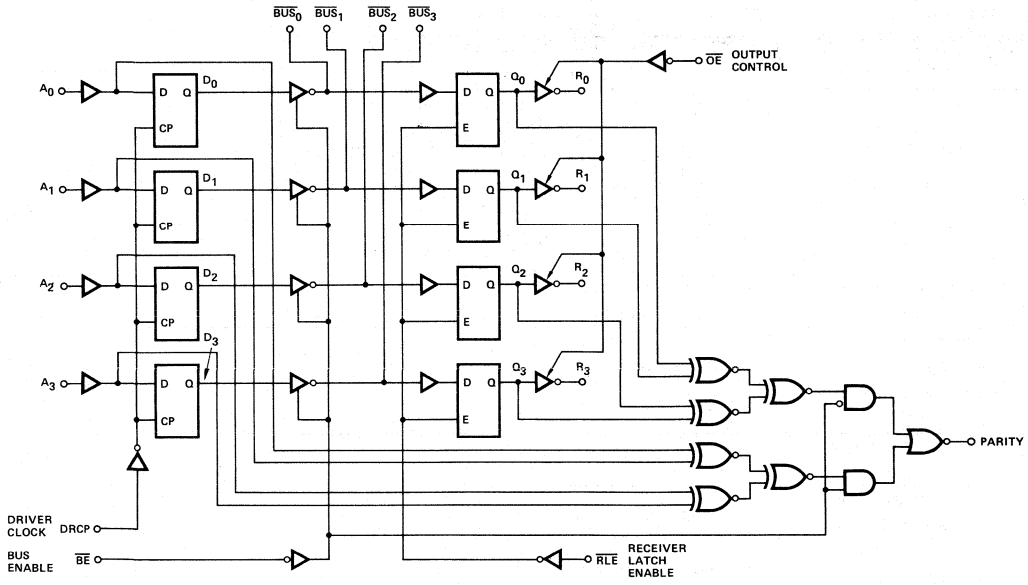
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-084

LOGIC DIAGRAM



MPR-085

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC, Am2908XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2907XM, Am2908XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V	Am2907	MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
			Am2908	MIL	1.9	1.5		
				COM'L	1.7	1.5		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V	Am2907	MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	
			Am2908	MIL		1.5	1.1	
				COM'L		1.5	1.3	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC, Am2908XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V

Am2907XM, Am2908XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1mA		2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA		2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −660μA, V_{IN} = V_{IH} or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5 V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND		Am2907		75	110	mA
				Am2908		80	120	
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V				20	μA
			V_O = 0.4 V				−20	

Am2907 SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2907XM Min.	Am2907XM Typ. (Note 2)	Am2907XM Max.	Am2907XC Min.	Am2907XC Typ. (Note 2)	Am2907XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs	C_L = 15pF, R_L = 2.0kΩ	18			15			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF, R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2908 SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2908XM Min.	Am2908XM Typ. (Note 2)	Am2908XM Max.	Am2908XC Min.	Am2908XC Typ. (Note 2)	Am2908XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF, R_L(BUS): 91Ω to V_{CC}, 200Ω to GND		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_r	Bus Output Rise Time		5	10		7	10		ns
t_f	Bus Output Fall Time		3	6		4	6		
t_s	Data Inputs		18			15			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)	C_L = 50pF, R_L = 2.0kΩ		18	38		18	35	ns
t_{PHL}				18	38		18	35	
t_{PLH}	Latch Enable to Receiver Output			21	38		21	35	ns
t_{PHL}				21	38		21	35	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)	C_L = 15pF, R_L = 2.0kΩ		21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF, R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics fo the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

6

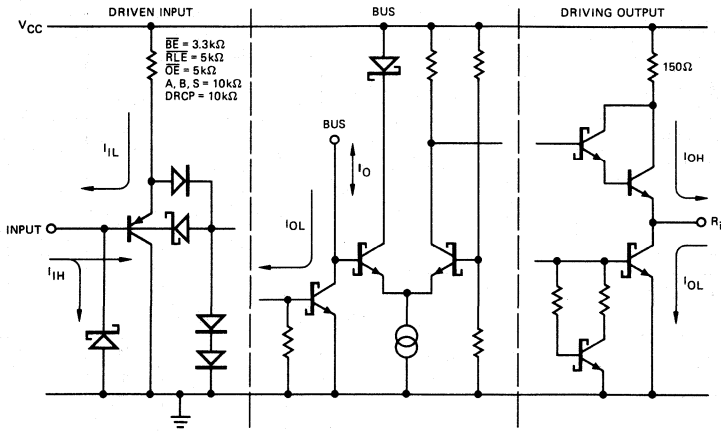
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2907 Order Number	Am2908 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2907PC	AM2908PC	P-20	C	C-1
AM2907DC	AM2908DC	D-20	C	C-1
AM2907DC-B	AM2908DC-B	D-20	C	B-1
AM2907DM	AM2908DM	D-20	M	C-3
AM2907DM-B	AM2908DM-B	D-20	M	B-3
AM2907FM	AM2908FM	F-20	M	C-3
AM2907FM-B	AM2908FM-B	F-20	M	B-3
AM2907XC	AM2908XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2907XM	AM2908XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C, Level B-3 conforms to MIL-STD-883, Class B.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

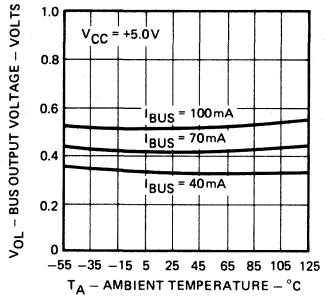


Note: Actual current flow direction shown.

MPR-086

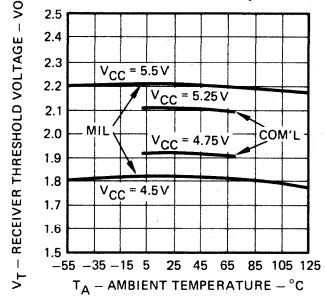
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



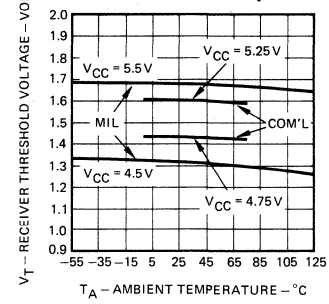
MPR-087

Am2907 Receiver Threshold Variation Versus Ambient Temperature



MPR-088

Am2908 Receiver Threshold Variation Versus Ambient Temperature



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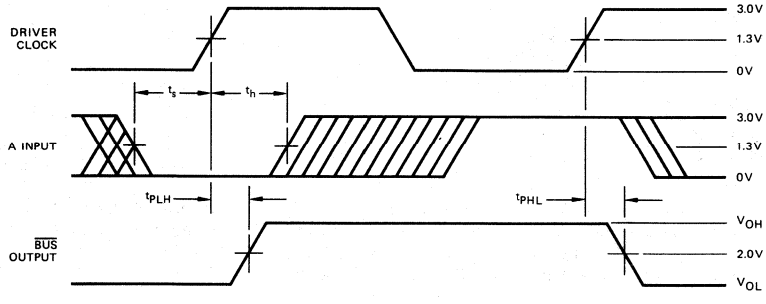
Am2907/08 SWITCHING WAVEFORMS



1. INPUT SET-UP AND HOLD TIMES.

MPR-089

TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

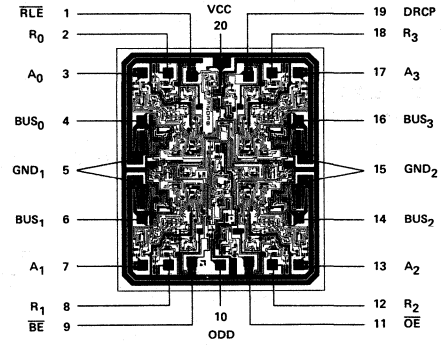
R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

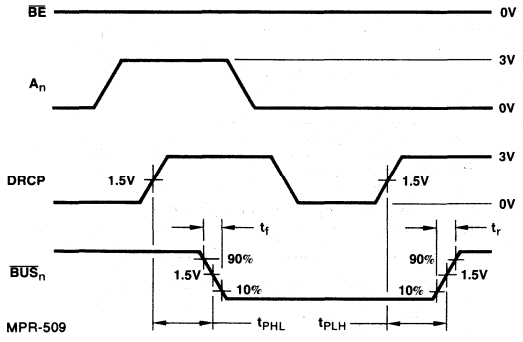
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

Metallization and Pad Layout

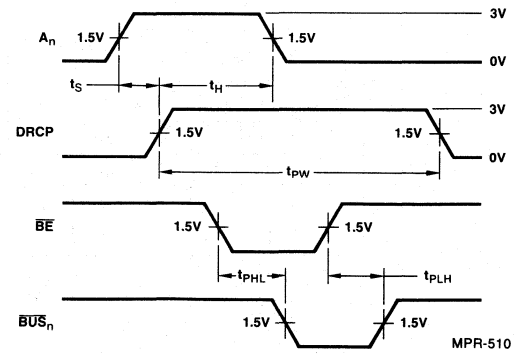


DIE SIZE 0.088" X 0.103"

Am2907/08 SWITCHING WAVEFORMS AND LOAD TEST CIRCUITS

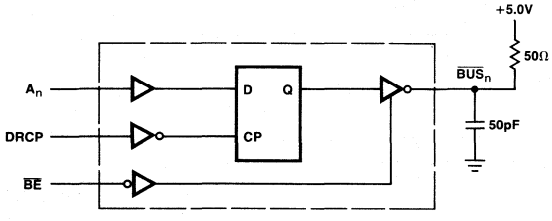


2. DRIVER CLOCK (DRCP) TO BUS

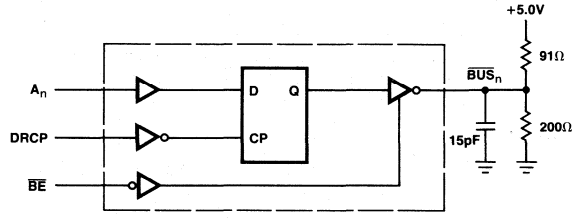


3. BUS ENABLE ($\overline{BE}$) TO BUS

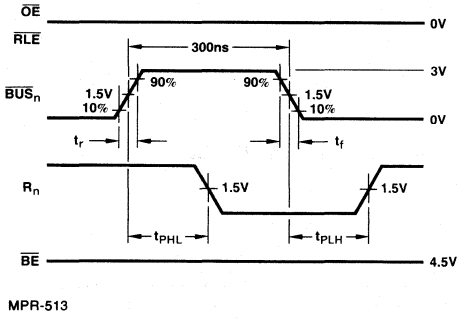
DRIVER SWITCHING WAVEFORMS



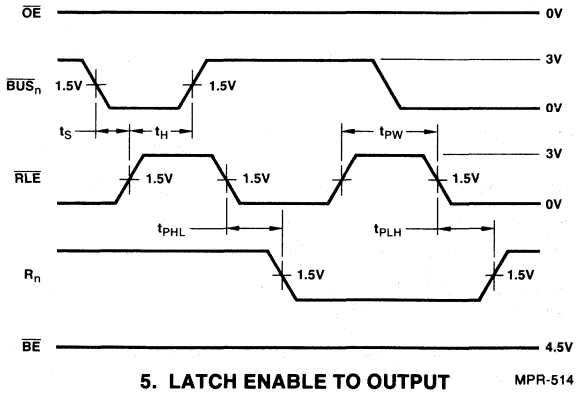
Am2907
DRIVER LOAD TEST CIRCUIT



Am2908
DRIVER LOAD TEST CIRCUIT

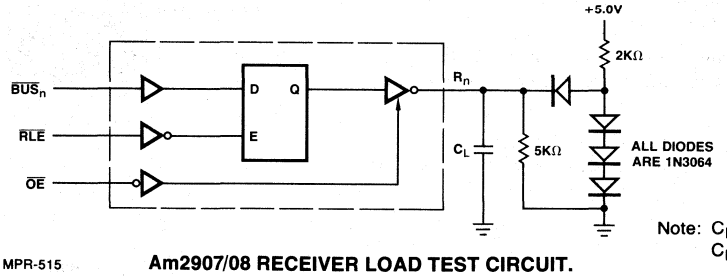


4. BUS TO RECEIVER OUTPUT (LATCH ENABLED)



5. LATCH ENABLE TO OUTPUT

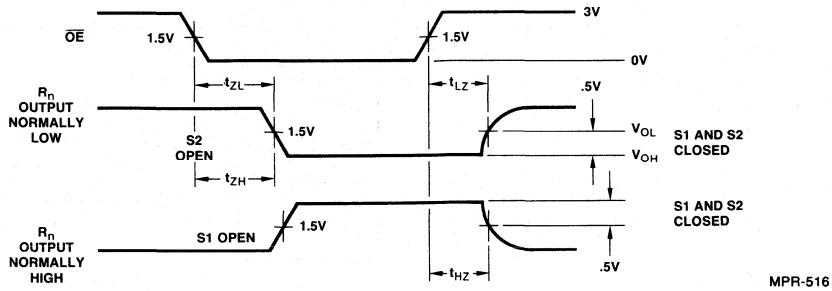
RECEIVER SWITCHING WAVEFORMS



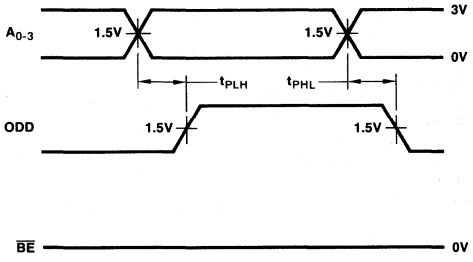
Note: C_L = 15pF for Am2907
C_L = 50pF for Am2908

Am2907/08 RECEIVER LOAD TEST CIRCUIT.

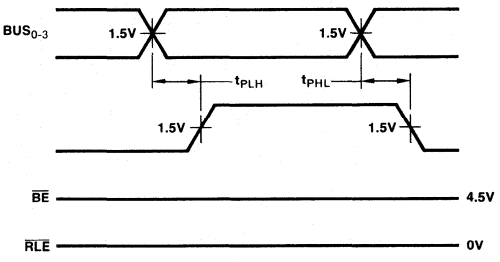
Am2907/08 SWITCHING WAVEFORMS AND LOAD TEST CIRCUITS (Cont.)



6. RECEIVER TRI-STATE WAVEFORMS

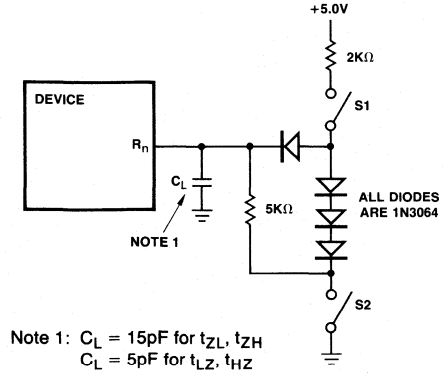


7. A INPUT TO PARITY OUTPUT

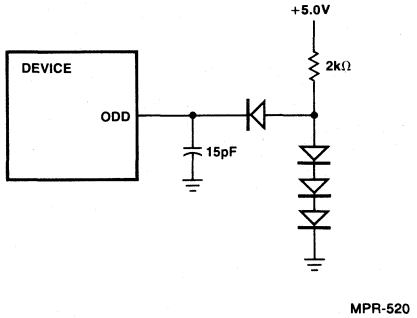


8. BUS TO PARITY OUTPUT

ODD PARITY OUTPUT WAVEFORMS

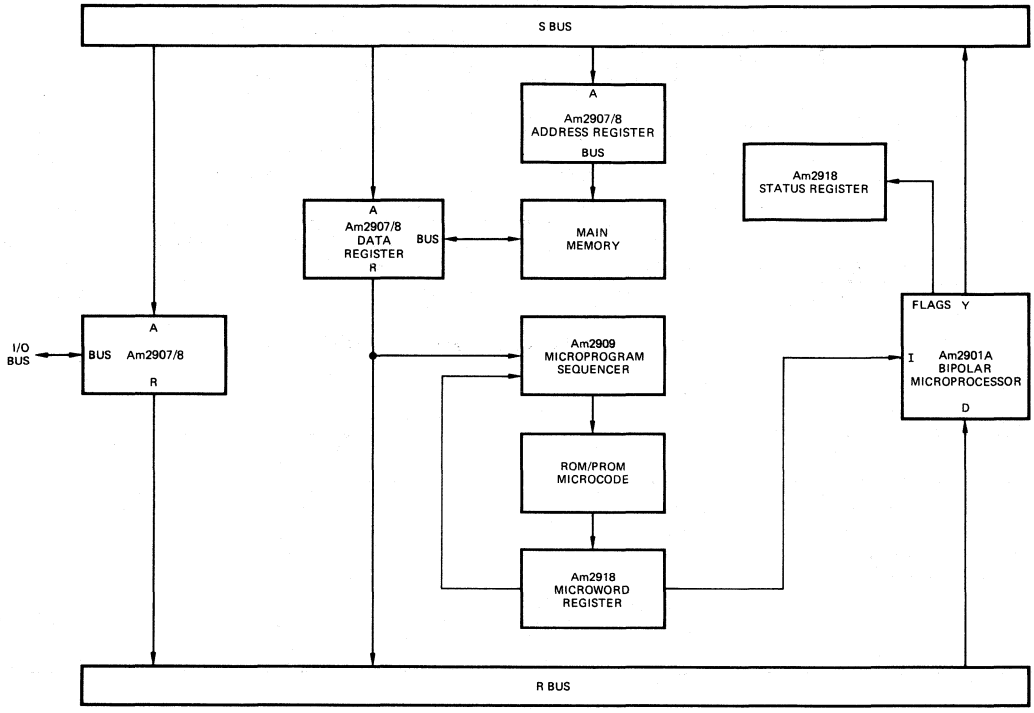


LOAD FOR RECEIVER TRI-STATE TEST



LOAD FOR PARITY OUTPUT

APPLICATIONS



The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

MPR-091

Am2909 • Am2911
Am2909A • Am2911A
Microprogram Sequencers

DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909 only)
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- Am2909 in 28-pin package
- Am2911 in 20-pin package
- New high-speed versions (Am2909A and Am2911A) are plug-in replacements for original Am2909 and Am2911
- Critical path speeds will be improved by about 25%

GENERAL DESCRIPTION

The Am2909 is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two Am2909's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

The Am2909 can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The Am2911 is an identical circuit to the Am2909, except the four OR inputs are removed and the D and R inputs are tied together. The Am2911 is in a 20-pin, 0.3" centers package. The Am2909A and Am2911A are direct plug-in replacements for the Am2909 and Am2911, but are about 25% faster.

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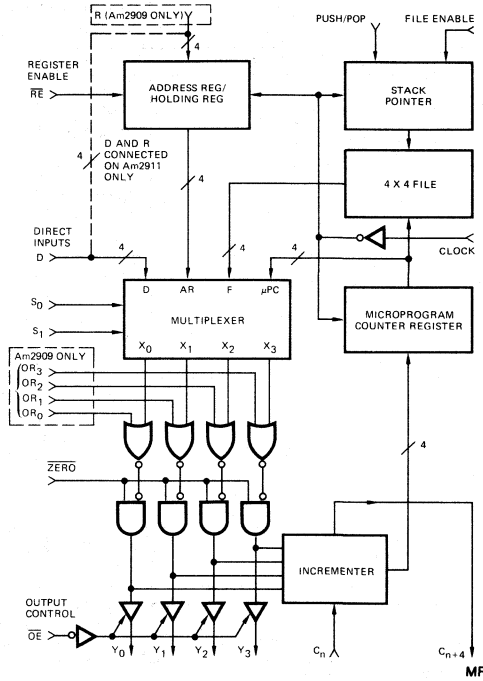
For applications information, see Chapter II of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

Operating Range	Part Number Suffix	Power Supply	Temperature Range
Commercial	PC, DC	5.0V ±5%	T_A = 0°C to +70°C
Military	DM, FM	5.0V ±10%	T_C = −55°C to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Notes)

(For Am2909, Am2911, Am2909A, Am2911A)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA, 2909/11				0.4	Volts
			I_{OL} = 8.0mA, 2909/11				0.45	
			I_{OL} = 12mA, 2909/11 (Note 5)				0.5	
			I_{OL} = 16mA, 2909A/11A				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL, 2909/11				0.7	Volts
			All others				0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{OE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n				40	μA
			Push/Pop				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 6V, V_{OUT} = .5V	$Y_0 - Y_3$		−30		−100	mA
			C_{n+4}		−30		−85	
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)	COM'L and MIL	T_A = +25°C			130	mA
			COM'L Only	T_A = 0 to +70°C			130	
			MIL Only	T_C = −55 to +125°C			140	
				T_C = +125°C			110	
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.7 V	Y_{0-3}	V_{OUT} = 0.4 V			−20	μA
I_{OZH}				V_{OUT} = 2.7 V			20	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs high. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 12mA guarantee applies only to Y_0, Y_1, Y_2 and Y_3.
6. For the Am2911 and Am2911A, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

Am2909A/Am2911A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II and III below define the timing characteristics of the Am2909A/Am2911A over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading. The data on this page applies to the following part numbers:

Operating Range	Part Numbers	Power Supply	Temperature Range
Com'l	Am2909APC, DC Am2911APC, DC	5.0V ±5%	T_A = 0°C to +70°C
Mil	Am2909ADM, FM Am2911ADM	5.0V ±10%	T_C = −55°C to +125°C

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

Time	COMMERCIAL	MILITARY
Minimum Clock LOW Time	20	20
Minimum Clock HIGH Time	20	20

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 50pF (except output disable tests))

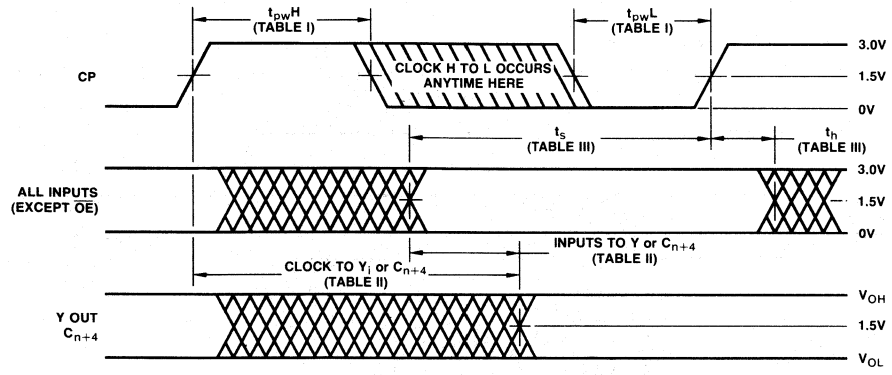
	COMMERCIAL		MILITARY	
From Input	Y	C_{n+4}	Y	C_{n+4}
D_i	17	22	20	25
S_0, S_1	29	34	29	34
OR_i	17	22	20	25
C_n	–	14	–	16
$\overline{ZERO}$	29	34	30	35
OE LOW (enable)	25	–	25	–
OE HIGH (disable)*	25	–	25	–
Clock ↑ S_1S_0 = LH	39	44	45	50
Clock ↑ S_1S_0 = LL	39	44	45	50
Clock ↑ S_1S_0 = HL	44	49	53	58

*C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL		MILITARY	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		19	4	19	5
R_i	2	10	4	12	5
PUSH/POP		25	4	27	5
FE		25	4	27	5
C_n		18	4	18	5
D_i		25	0	25	0
OR_i		25	0	25	0
S_0, S_1		25	0	29	0
$\overline{ZERO}$		25	0	29	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On Am2911A, R_i and D_i are internally connected and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



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Am2909 and Am2911 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II, and III below define the timing characteristics of the Am2909 and Am2911 over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e. clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading. The data on this page applies to the following part numbers:

Operating Range	Part Numbers	Power Supply	Temperature Range
Com'l	Am2909PC, DC Am2911PC, DC	5.0V ±5%	T_A = 0°C to +70°C
Mil	Am2909DM, FM Am2911DM	5.0V ±10%	T_C = −55°C to +125°C

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	30	35
Minimum Clock HIGH Time	30	35

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 50pF (except output disable tests))

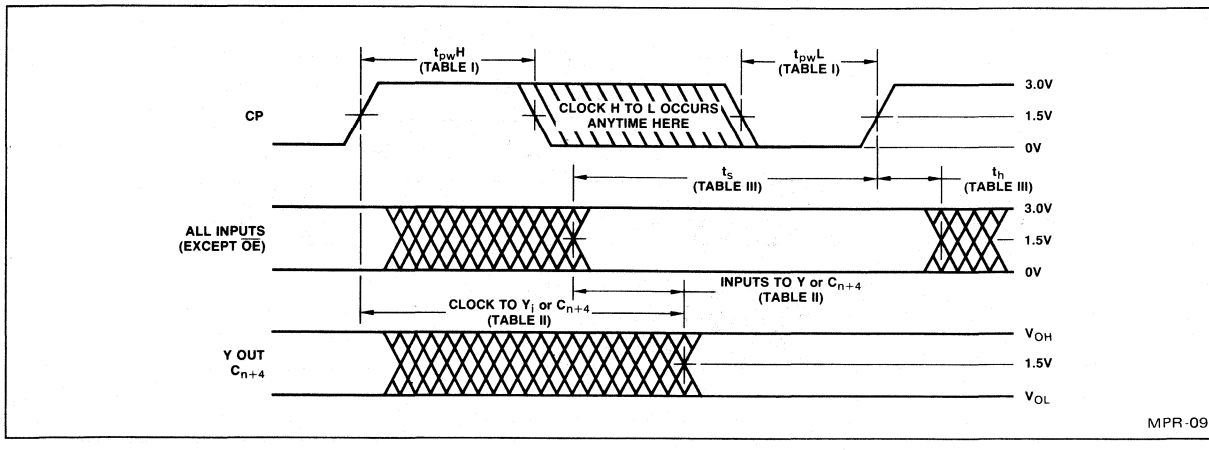
From Input	COMMERCIAL		MILITARY	
	Y	C_{n+4}	Y	C_{n+4}
D_i	17	30	20	32
S_0, S_1	30	48	40	50
OR_i	17	30	20	32
C_n	–	14	–	16
$\overline{ZERO}$	30	48	40	50
$\overline{OE}$ LOW (enable)	25	–	25	–
$\overline{OE}$ HIGH (disable)*	25	–	25	–
Clock ↑ S_1S_0 = LH	43	55	50	62
Clock ↑ S_1S_0 = LL	43	55	50	62
Clock ↑ S_1S_0 = HL	80	95	90	102

*C_L = 5.0pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL		MILITARY	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		22	5	22	5
R_i	2	10	5	12	5
PUSH/POP		26	6	30	7
$\overline{FE}$		26	5	30	5
C_n		28	5	30	5
D_i		30	0	35	3
OR_i		30	0	35	3
S_0, S_1		45	0	50	0
$\overline{ZERO}$		45	0	50	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On Am2911, R_i and D_i are internally connected together and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



DEFINITION OF TERMS

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the Am2909. Since its principle application is as a controller for a microprogram store, it is necessary to define some signals associated with the microcode itself. Figure 3 illustrates the basic interconnection of Am2909, memory, and microinstruction register. The definitions here apply to this architecture.

Inputs to Am2909/Am2911

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs from the Am2909/Am2911

Y_i	Address outputs from Am2909. (Address inputs to control memory.)
C_{n+4}	Carry out from the incrementer

Internal Signals

μPC	Contents of the microprogram counter
AR	Contents of the address/holding register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External to the Am2909/Am2911

A	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

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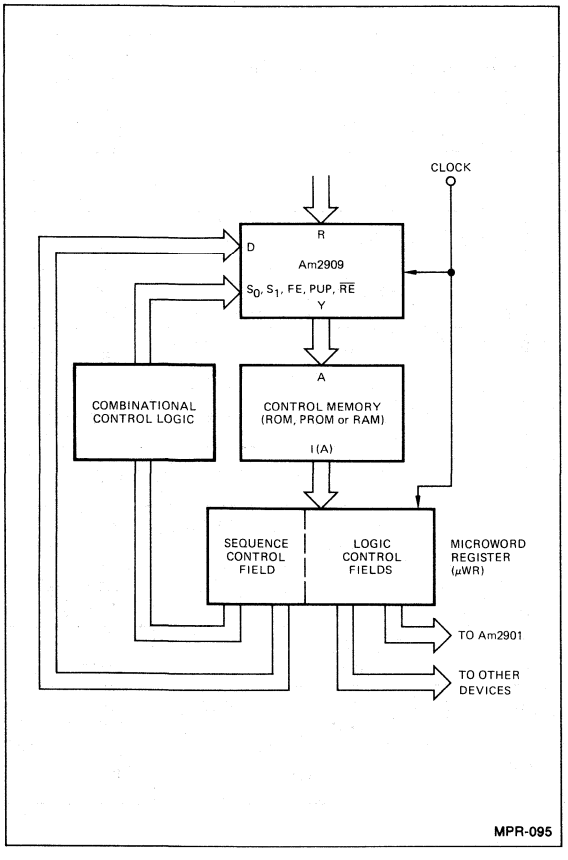


Figure 3. Microprogram Sequencer Control.

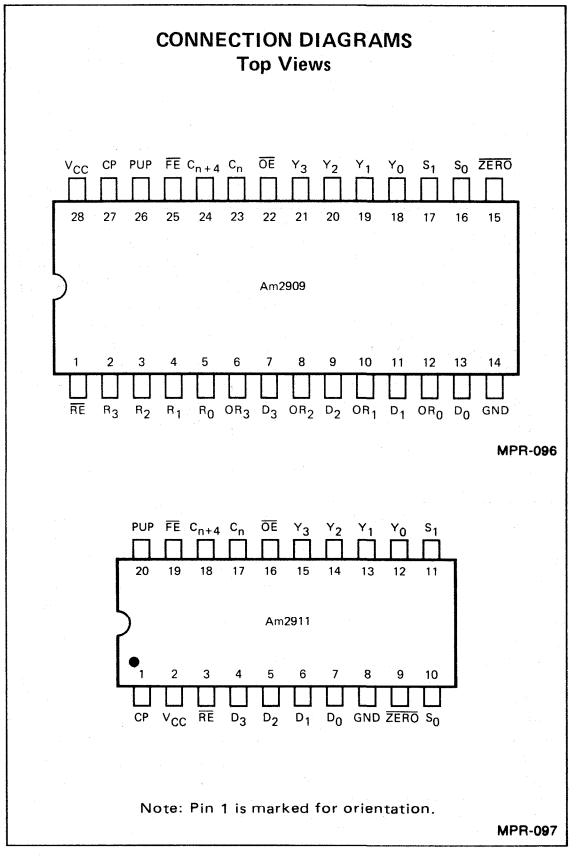


Figure 4.

OPERATION OF THE Am2909/Am2911

Figure 5 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 5 also shows the truth table for the output control and for the control of the push/pop stack. Figure 6 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the Am2909. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Address/Holding Register	AR
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 5.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N	0 0 0 0	J	K	Ra	Rb	Rc	Rd	J	Pop Stack	End Loop
N+1	–	J+1	K	Rb	Rc	Rd	Ra	–		
N	0 0 0 1	J	K	Ra	Rb	Rc	Rd	J	Push μPC	Set-up Loop
N+1	–	J+1	K	J	Ra	Rb	Rc	–		
N	0 0 1 X	J	K	Ra	Rb	Rc	Rd	J	Continue	Continue
N+1	–	J+1	K	Ra	Rb	Rc	Rd	–		
N	0 1 0 0	J	K	Ra	Rb	Rc	Rd	K	Pop Stack; Use AR for Address	End Loop
N+1	–	K+1	K	Rb	Rc	Rd	Ra	–		
N	0 1 0 1	J	K	Ra	Rb	Rc	Rd	K	Push μPC; Jump to Address in AR	JSR AR
N+1	–	K+1	K	J	Ra	Rb	Rc	–		
N	0 1 1 X	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR	JMP AR
N+1	–	K+1	K	Ra	Rb	Rc	Rd	–		
N	1 0 0 0	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0; Pop Stack	RTS
N+1	–	Ra+1	K	Rb	Rc	Rd	Ra	–		
N	1 0 0 1	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0; Push μPC	
N+1	–	Ra+1	K	J	Ra	Rb	Rc	–		
N	1 0 1 X	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0	Stack Ref (Loop)
N+1	–	Ra+1	K	Ra	Rb	Rc	Rd	–		
N	1 1 0 0	J	K	Ra	Rb	Rc	Rd	D	Pop Stack; Jump to Address on D	End Loop
N+1	–	D+1	K	Rb	Rc	Rd	Ra	–		
N	1 1 0 1	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D; Push μPC	JSR D
N+1	–	D+1	K	J	Ra	Rb	Rc	–		
N	1 1 1 X	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D	JMP D
N+1	–	D+1	K	Ra	Rb	Rc	Rd	–		

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer.

Figure 6. Output and Internal Next-Cycle Register States for Am2909/Am2911.

Figure 7 illustrates the execution of a subroutine using the Am2909. The configuration of Figure 3 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the Am2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the comand "Jump to subroutine at A". At the time T_2, this instruction is in the μWR, and the Am2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T_5. Figure 8 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	—
T_0	J	—
T_1	J+1	—
T_2	J+2	JSR A
T_6	J+3	—
T_7	J+4	—
	—	—
	—	—
	—	—
	—	—
	—	—
T_3	A	I(A)
T_4	A+1	—
T_5	A+2	RTS
	—	—
	—	—
	—	—
	—	—
	—	—
	—	—
	—	—

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	—	—	—	J+3	J+3	J+3	—	—		
	STK1	—	—	—	—	—	—	—	—		
	STK2	—	—	—	—	—	—	—	—		
	STK3	—	—	—	—	—	—	—	—		
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)		

Figure 7. Subroutine Execution.

C_n = HIGH

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	—
T_0	J	—
T_1	J+1	—
T_2	J+2	JSR A
T_9	J+3	—
	—	—
	—	—
	—	—
	—	—
T_3	A	—
T_4	A+1	—
T_5	A+2	JSR B
T_7	A+3	—
T_8	A+4	RTS
	—	—
	—	—
	—	—
	—	—
T_6	B	RTS
	—	—
	—	—

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	—	—	—	J+3	J+3	J+3	A+3	J+3	J+3	—
	STK1	—	—	—	—	—	—	J+3	—	—	—
	STK2	—	—	—	—	—	—	—	—	—	—
	STK3	—	—	—	—	—	—	—	—	—	—
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)

Figure 8. Two Nested Subroutines. Routine B is Only One Instruction.

C_n = HIGH

USING THE Am2909 AND Am2911

The Am2909 and Am2911 are four-bit slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the Am2909 and Am2911 apart from the Am2910, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The Am2909 or Am2911 should be selected instead of the Am2910 under the following conditions:

- Address less than 8 bits and not likely to be expanded
- Address longer than 12 bits
- More complex instruction set needed than is available on Am2910

Architecture of the Control Unit

The recommended architecture using the Am2909 or Am2911 is shown in Figure 1. Note that the path from the pipeline register output through the next address logic, multiplexer, and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return-from-subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the Am2909 or Am2911. The block labeled "next address logic" may consist of simple gates, a PROM or a PLA, but it should be all combinational.

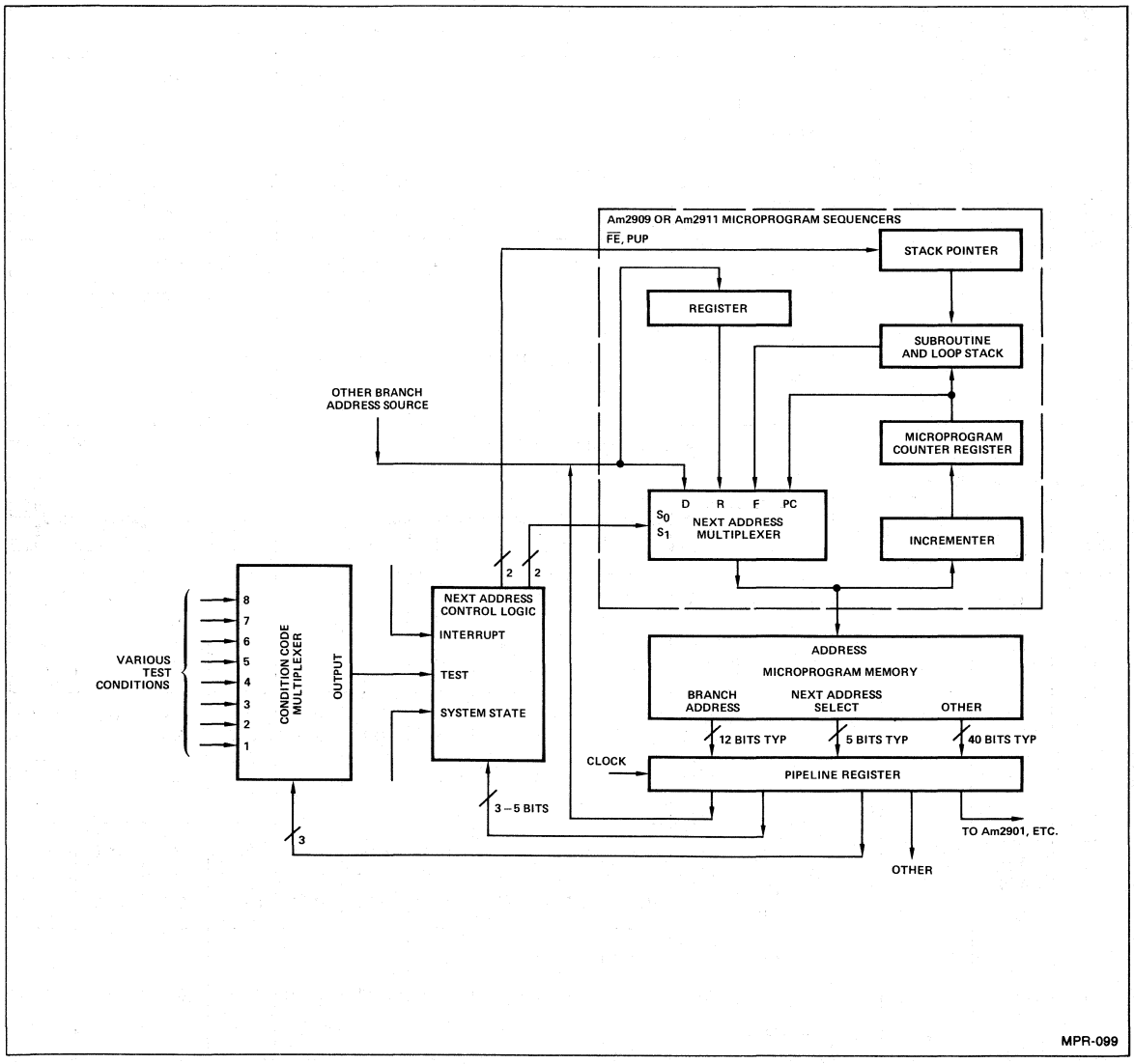


Figure 1. Recommended Computer Control Unit Architecture Using the Am2911 or Am2909.

The Am29811A is a combinational circuit which implements 16 sequence control instructions; it may be used with either an Am2909 or an Am2911. The set of instructions is nearly identical to that implemented internally in the Am2910.

Figure 2 shows the CCU of Figure 1 with the Am29811A in place. The Am29811A, in addition to controlling the Am2911, also controls a loop counter and several branch address sources. The instructions which are implemented by the Am29811A are shown in Figure 3, along with the Am29811A outputs for each instruction. Generating any instruction set consists simply of writing a truth table and designing combinational logic to implement it. For more detailed information refer to "The Microprogramming Handbook".

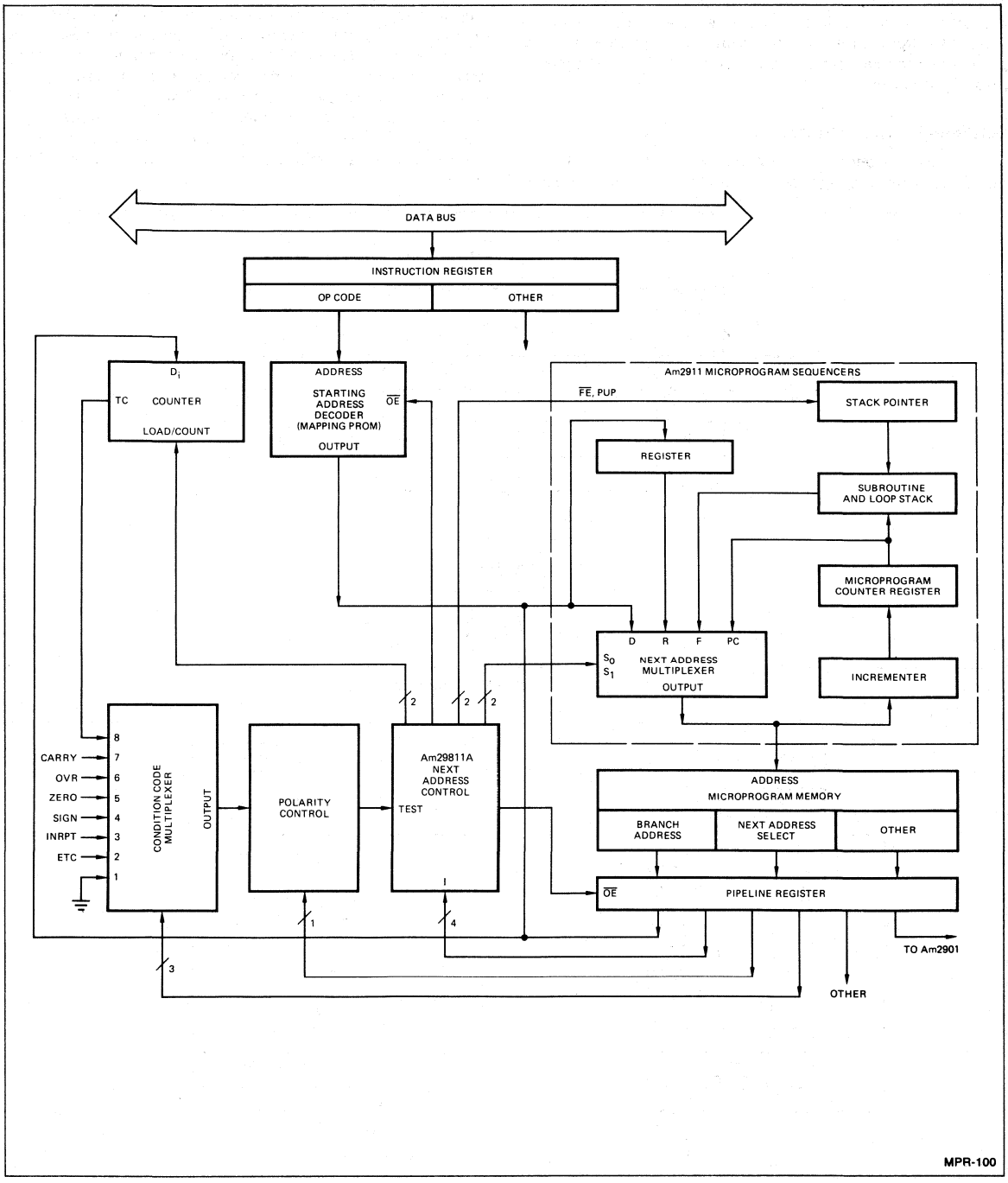


Figure 2. A Typical Computer Control Unit Using the Am2911 and Am29811A.

Expansion of the Am2909 or Am2911

Figure 4 shows the interconnection of three Am2911's to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between μPC incrementors. This carry path is not in the critical speed path if the Am2911 Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a micro-address register is placed at the Am2911 output, then the carry may lie in the critical speed path, since the last carry-in must be stable for a set-up time prior to the clock.

Selecting Between the Am2909 and Am2911

The difference between the Am2909 and the Am2911 involves two signals: the data inputs to the holding register and the "OR" inputs. In the Am2909, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the Am2911, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 5. Using the Am2909, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the Am2911, it is more common to connect the Am2911's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 5 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

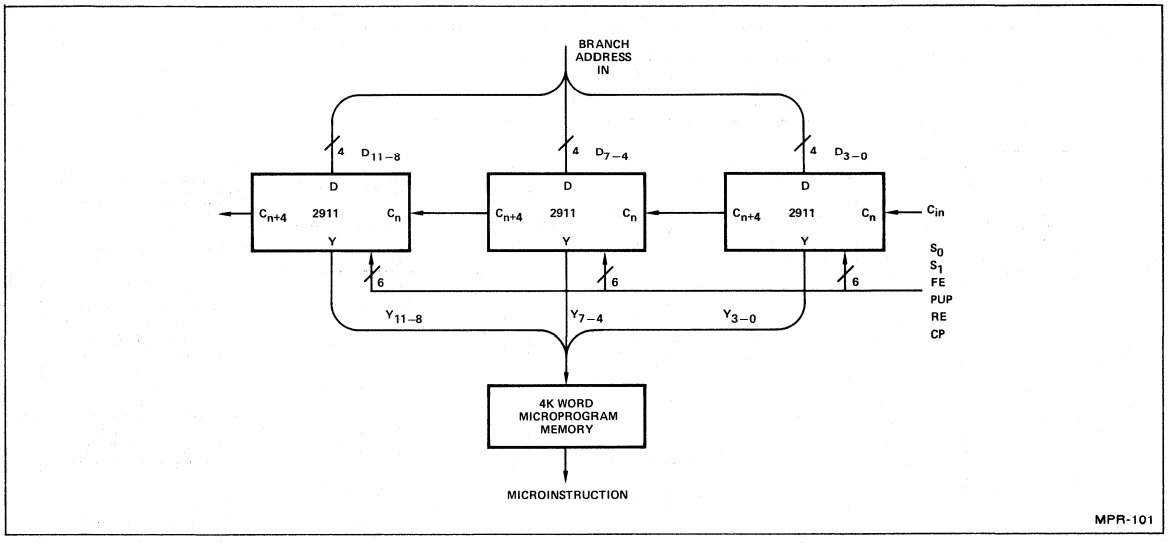


Figure 4. Twelve Bit Sequencer.

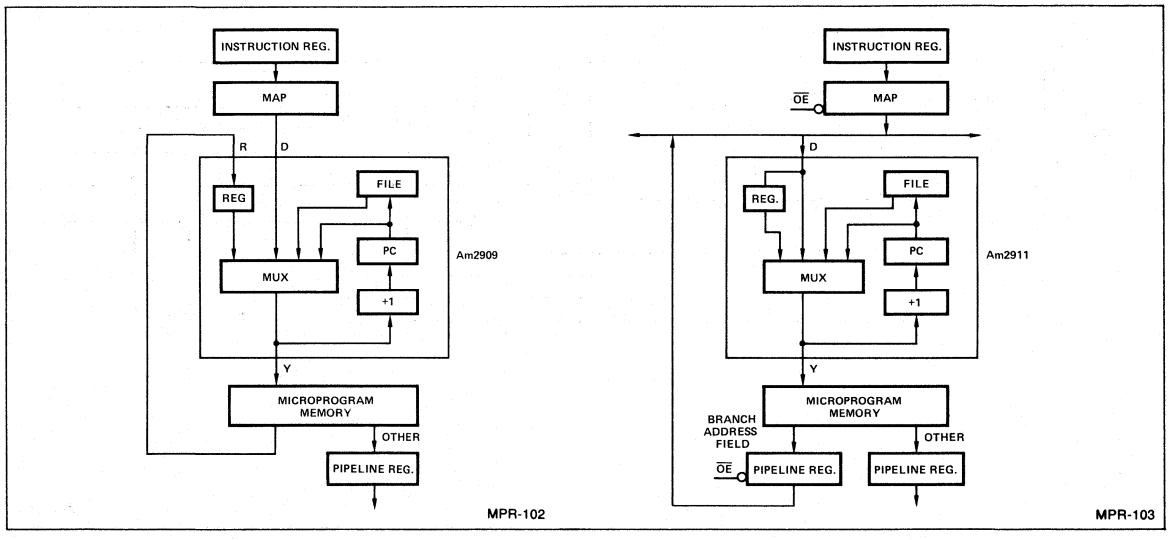


Figure 5. Branch Address Structures.

The second difference between the Am2909 and Am2911 is that the Am2909 has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply tying several test conditions into the OR lines. See Figure 6. Typically, a branch is taken to an address with zeroes in the least significant bits. These bits are replaced with 1's or 0's by test conditions applied to the OR lines. In Figure 6, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110, or 1111.

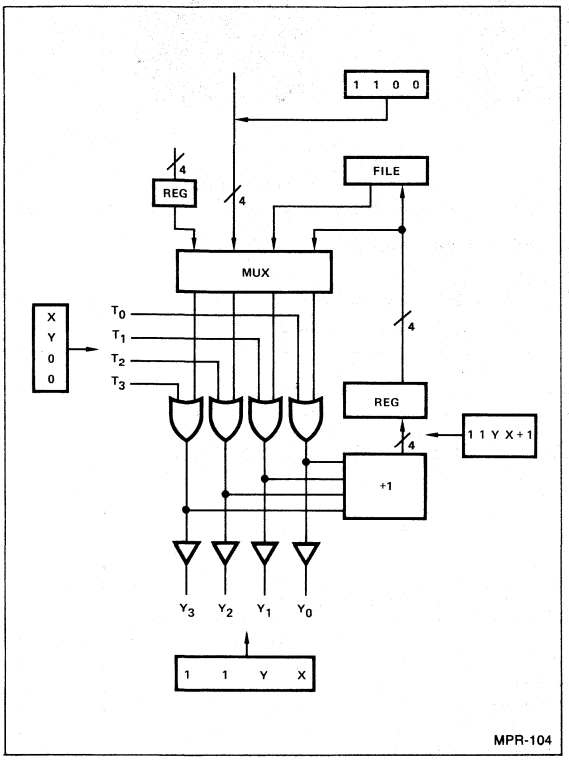


Figure 6. Use of OR Inputs to Obtain 4 - Way Branch.

The Am29803A has been designed to selectively apply any or all of four different test conditions to an Am2909. Figure 7 shows the truth table for this device. A nice trade off between flexibility and board space is achieved by using a single 28-pin Am2909 for the least significant four bits of a sequencer, and using the space-saving 20-pin Am2911's for the remainder of the bits. A detailed logic design for such a system is contained in The Microprogramming Handbook.

How to Perform Some Common Functions with the Am2909 or Am2911

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	1	0	0	1	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	1	1	1	1	X

Feed data on D inputs straight through to memory address lines. Increment address and place in PC.

3. JUMP-TO-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	1	1	1	0	1

Sub-routine address fed from D inputs to memory address. Current PC is pushed onto stack, where it is saved for the return.

4. RETURN-FROM-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	1	1	0	0	0

The address at the top of the stack is applied to the microprogram memory, and is incremented for PC on the next cycle. The stack is popped to remove the return address.

Am29803A FUNCTION TABLE

	BRANCH ON	I_3	I_2	I_1	I_0	OR_3	OR_2	OR_1	OR_0
NONE	NONE	L	L	L	L	L	L	L	L
Two-Way Branches	T_0	L	L	L	H	L	L	L	T_0
	T_1	L	L	H	L	L	L	L	T_1
	T_2	L	H	L	L	L	L	L	T_2
	T_3	H	L	L	L	L	L	L	T_3
Four-Way Branches	T_1 & T_0	L	L	H	H	L	L	T_1	T_0
	T_2 & T_0	L	H	L	H	L	L	T_2	T_0
	T_3 & T_0	H	L	L	H	L	L	T_3	T_0
	T_2 & T_1	L	H	H	L	L	L	T_2	T_1
	T_3 & T_1	H	L	H	L	L	L	T_3	T_1
	T_3 & T_2	H	H	L	L	L	L	T_3	T_2
Eight-Way Branches	T_2, T_1, T_0	L	H	H	H	L	T_2	T_1	T_0
	T_3, T_1, T_0	H	L	H	H	L	T_3	T_1	T_0
	T_3, T_2, T_0	H	H	L	H	L	T_3	T_2	T_0
	T_3, T_2, T_1,	H	H	H	L	L	T_3	T_2	T_1
Sixteen-Way Branch	T_3, T_2, T_1, T_0	H	H	H	H	T_3	T_2	T_1	T_0

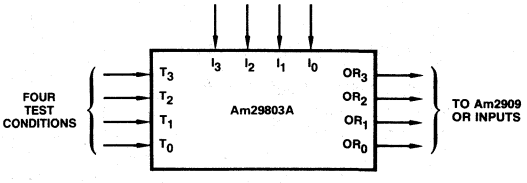
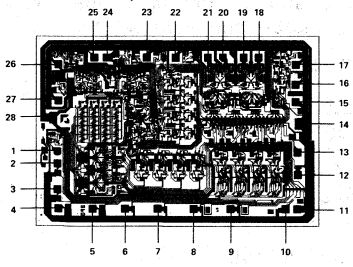


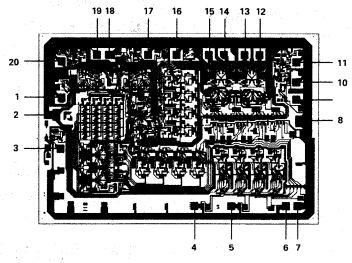
Figure 7.

Metallization and Pad Layouts

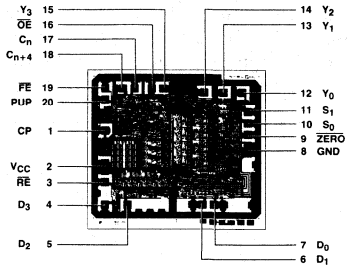
Am2909



Am2911



Am2911A



Numbers correspond to DIP pin-out
DIE SIZE 0.110" X 0.160"

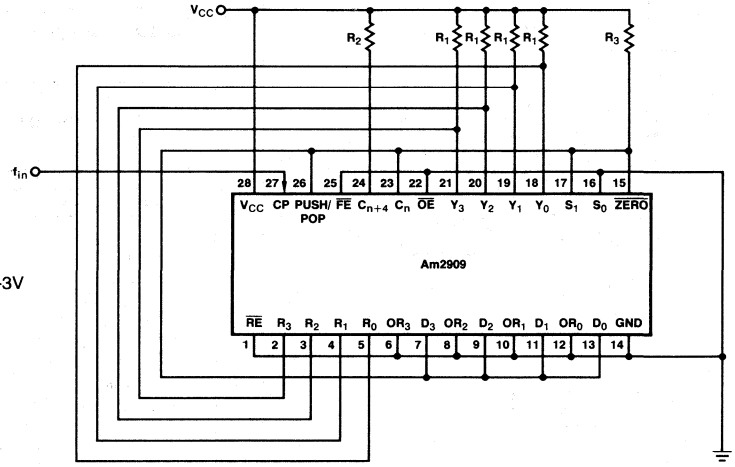
DIE SIZE 86 X 98 Mils

Burn-in Circuit for Am2909 (Flatpack and Hermetic DIP)

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

V_{CC} min. = 5.0V
V_{CC} max. = 5.1V



This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

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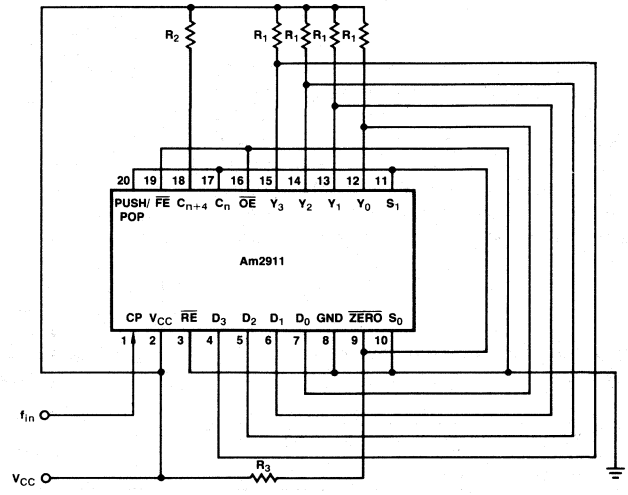
Burn-in Circuit for Am2911

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

From clock buffer on each board:
V_{CC} min. = 5.0V
V_{CC} max. = 5.1V



This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

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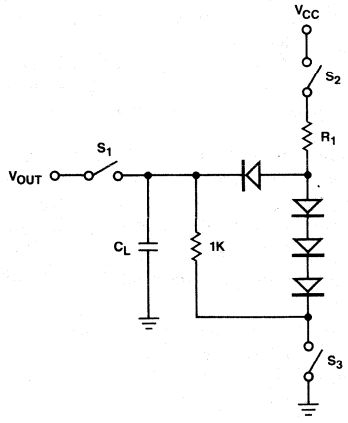
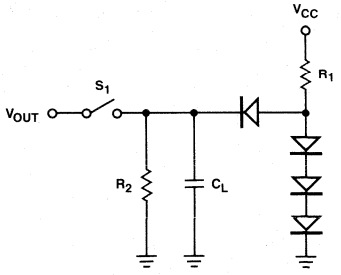
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2909/2911 AND Am2909A/2911A

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC test except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS

Pin # (DIP)	Pin Label	Test Circuit	Am2909		Am2909A	
			R_1	R_2	R_1	R_2
18-21	Y_{0-3}	A	300	1K	220	1K
24	C_{n+4}	B	470	2.4K	220	2.4K

TEST OUTPUT LOADS

Pin # (DIP)	Pin Label	Test Circuit	Am2911		Am2911A	
			R_1	R_2	R_1	R_2
12-15	Y_{0-3}	A	300	1K	220	1K
18	C_{n+4}	B	470	2.4K	220	2.4K

For additional information in testing, see section "Guidelines on Testing Am2900 Family Devices."

ARCHITECTURE OF THE Am2909/Am2911

The Am2909/Am2911 are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 2.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909/Am2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y+1→μPC.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y→μPC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage — the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The Am2909/Am2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2911 Order Number	Am2911A Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2911PC	AM2911APC	P-20	C	C-1
AM2911DC	AM2911ADC	D-20	C	C-1
AM2911DC-B	AM2911ADC-B	D-20	C	B-2 (Note 4)
AM2911DM	AM2911ADM	D-20	M	C-3
AM2911DM-B	AM2911ADM-B	D-20	M	B-3
AM2911XC	AM2911AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2911XM	AM2911AXM	Dice	M	

Am2909 Order Number	Am2909A Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2909PC	AM2909APC	P-28	C	C-1
AM2909DC	AM2909ADC	D-28	C	C-1
AM2909DC-B	AM2909ADC-B	D-28	C	B-2 (Note 4)
AM2909DM	AM2909ADM	D-28	M	C-3
AM2909DM-B	AM2909ADM-B	D-28	M	B-3
AM2909FM	AM2909AFM	F-28-1	M	C-3
AM2909FM-B	AM2909AFM-B	F-28-1	M	B-3
AM2909XC	AM2909AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2909XM	AM2909AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hours of burn-in.

Figure 1.

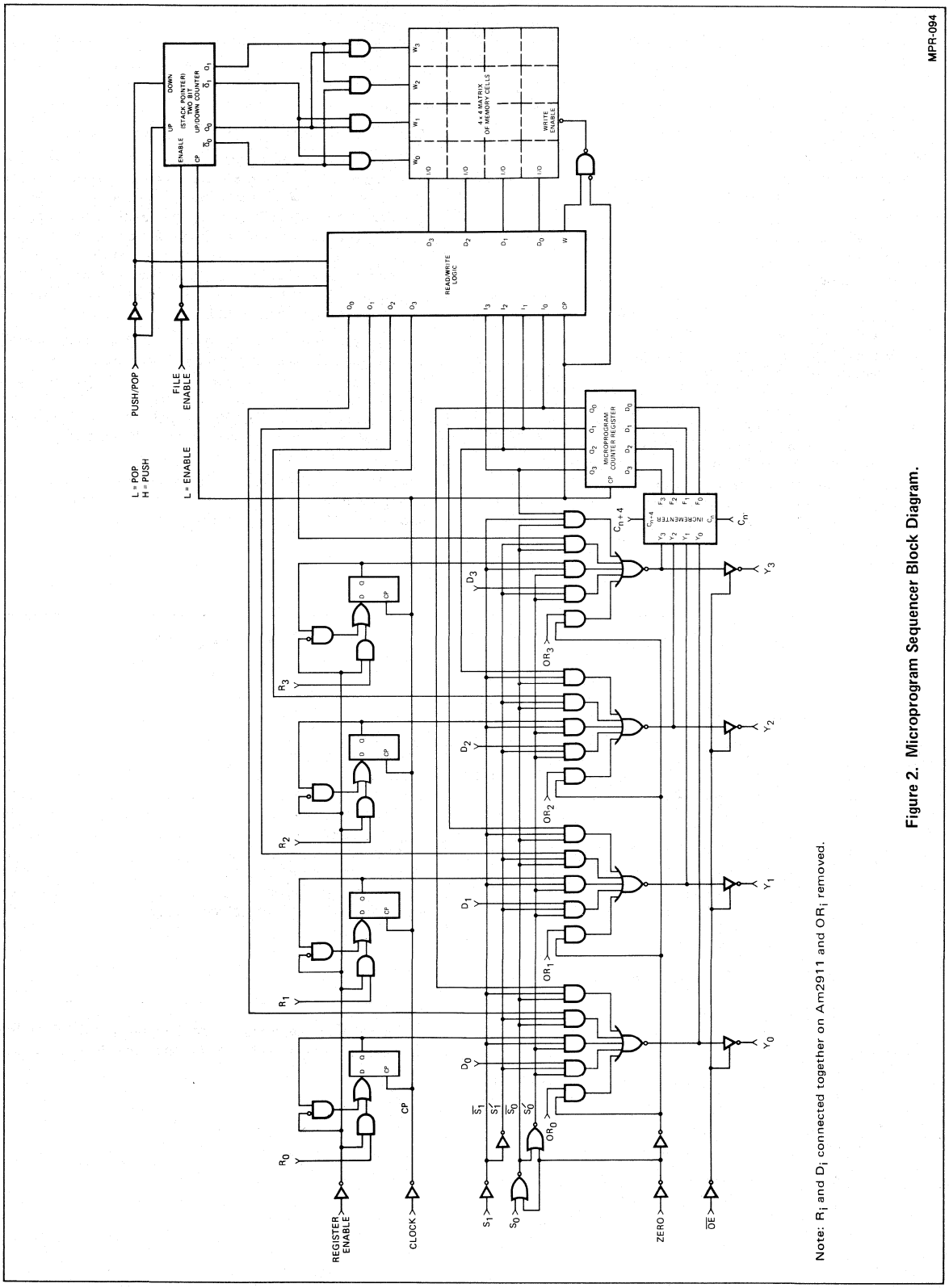


Figure 2. Microprogram Sequencer Block Diagram.

Note: R_i and D_i connected together on Am2911 and OR_i removed.

6

Am2910
Microprogram Controller

DISTINCTIVE CHARACTERISTICS

- Twelve Bits Wide
  Address up to 4096 words of microcode with one chip. All internal elements are a full 12 bits wide.
- Internal Loop Counter
  Pre-settable 12-bit down-counter for repeating instructions and counting loop iterations.
- Four Address Sources
  Microprogram Address may be selected from microprogram counter, branch address bus, 5-level push/pop stack, or internal holding register.
- Sixteen Powerful Microinstructions
  Executes 16 sequence control instructions, most of which are conditional on external condition input, state of internal loop counter, or both.
- Output Enable Controls for Three Branch Address Sources
  Built-in decoder function to enable external devices onto branch address bus. Eliminates external decoder.
- All Registers Positive Edge-triggered
  Simplifies timing problems. Eliminates long set-up times.
- Fast Control from Condition Input
  Delay from condition code input to address output only 21ns typical.

GENERAL DESCRIPTION

The Am2910 Microprogram controller is an address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range. A last-in, first-out stack provides microsubroutine return linkage and looping capability; there are five levels of nesting of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

During each microinstruction, the Microprogram controller provides a 12-bit address from one of four sources: 1) the microprogram address register (μPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a five-deep last-in, first-out stack (F).

For a detailed discussion of this architectural approach to microprogram control units, refer to "The Microprogramming Handbook", an AMD applications publication.

Am2910 BLOCK DIAGRAM

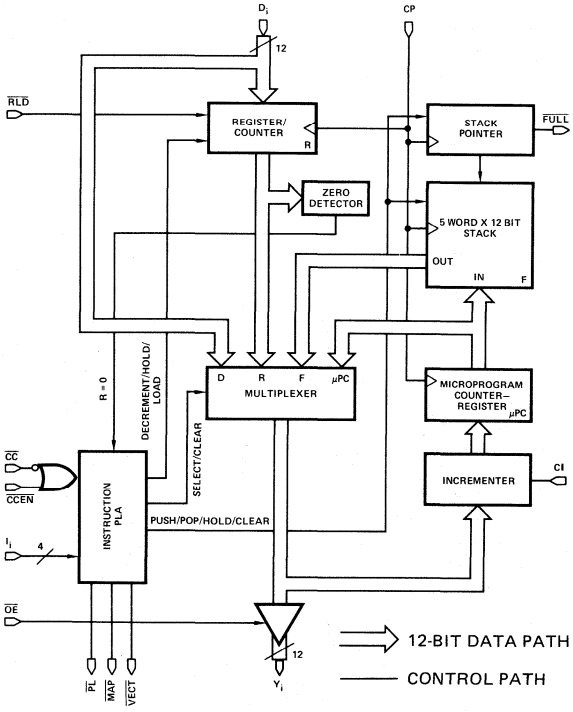


Figure 1.

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TABLE OF CONTENTS

For applications information, see Chapter II of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

ARCHITECTURE OF THE Am2910

The Am2910 is a bipolar microprogram controller intended for use in high-speed microprocessor applications. It allows addressing of up to 4K words of microprogram. A block diagram is shown in Figure 1.

The controller contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

The register/counter consists of 12 D-type, edge-triggered flip-flops, with a common clock enable. When its load control, $\overline{RLD}$, is LOW, new data is loaded on a positive clock transition. A few instructions include load; in most systems, these instructions will be sufficient, simplifying the microcode. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

The Am2910 contains a microprogram counter (μPC) that is composed of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways: When the carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). Sequential microinstructions are thus executed. When the carry-in is LOW, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). The same microinstruction is thus executed any number of times.

The third source for the multiplexer is the direct (D) input. This source is used for branching.

The fourth source available at the multiplexer input is a 5-word by 12-bit stack (file). The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a pop.

The stack pointer operates as an up/down counter. During microinstructions 1, 4, and 5, the PUSH operation may occur. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (Instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one. The depth can grow to five. After a depth of five is reached, $\overline{FULL}$ goes LOW. Any further PUSHes onto a full stack overwrite information at the top of the stack, but leave the stack pointer unchanged. This operation will usually destroy useful information and is normally avoided. A POP from an empty stack may place non-meaningful data on the Y outputs, but is otherwise safe. The stack pointer remains at zero whenever a POP is attempted from a stack already empty.

The register/counter is operated during three microinstructions (8, 9, 15) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions. The register/counter is arranged such that if it is preloaded with a number N and then used as a loop termination counter, the sequence will be executed exactly N+1 times. During instruction 15, a three-way branch under combined control of the loop counter and the condition code is available.

The device provides three-state Y outputs. These can be particularly useful in designs requiring automatic checkout of the processor. The microprogram controller outputs can be forced into the high-impedance state, and pre-programmed sequences of microinstructions can be executed via external access to the address lines.

OPERATION

Table I shows the result of each instruction in controlling the multiplexer which determines the Y outputs, and in controlling the three enable signals $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. The effect on the register/counter and the stack after the next positive-going clock edge is also shown. The multiplexer determines which internal source drives the Y outputs. The value loaded into μPC is either identical to the Y output, or else one greater, as determined by CI. For each instruction, one and only one of the three outputs $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$ is LOW. If these outputs control three-state enables for the primary source of microprogram jumps (usually part of a pipeline register), a PROM which maps the instruction to a microinstruction starting location, and an optional third source (often a vector from a DMA or interrupt source), respectively, the three-state sources can drive the D inputs without further logic.

Several inputs, as shown in Table II, can modify instruction execution. The combination $\overline{CC}$ HIGH and $\overline{CCEN}$ LOW is used as a test in 9 of the 16 instructions. $\overline{RLD}$, when LOW, causes the D input to be loaded into the register/counter, overriding any HOLD or DEC operation specified in the instruction. $\overline{OE}$, normally LOW, may be forced HIGH to remove the Am2910 Y outputs from a three-state bus.

The stack, a five-word last-in, first-out 12-bit memory, has a pointer which addresses the value presently on the top of the stack. Explicit control of the stack pointer occurs during instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever else the stack is empty, the contents of the top of stack is undefined until a PUSH occurs. Any POPs performed while the stack is empty put undefined data on the F outputs and leave the stack pointer at zero.

Any time the stack is full (five more PUSHes than POPs have occurred since the stack was last empty), the $\overline{FULL}$ warning output occurs. This signal first appears on the microcycle after a fifth PUSH. No additional PUSH should be attempted onto a full stack; if tried, information within the stack will be overwritten and lost.

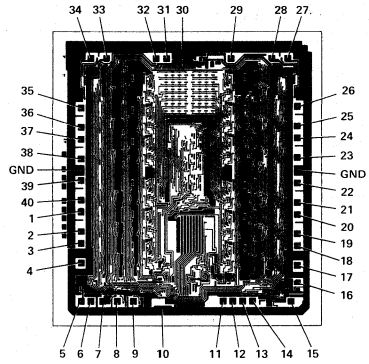
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2910PC	P-40	C	C-1
AM2910DC	D-40	C	C-1
AM2910DC-B	D-40	C	B-2 (Note 4)
AM2910DM	D-40	M	C-3
AM2910DM-B	D-40	M	B-3
AM2910FM	F-42	M	C-3
AM2910FM-B	F-42	M	B-3
AM2910XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2910XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

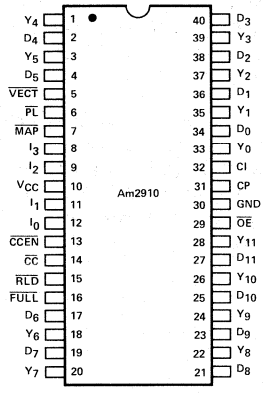
Metallization and Pad Layout



Die Size 0.170" x 0.194"
(Note: Numbers refer to DIP connections)

CONNECTION DIAGRAMS — Top Views

DIP



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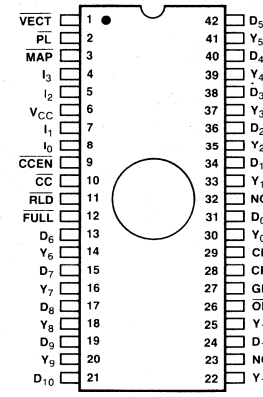
Flat Package



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Pin 1 is marked for orientation.

TABLE I. INSTRUCTIONS

I_3-I_0	MNEMONIC	NAME	REG/ CNTR CON-TENTS	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠ 0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

Note 1: If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care

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TABLE II. PIN FUNCTIONS

Abbreviation	Name	Function
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer. D_0 is LSB
I_i	Instruction Bit i	Selects one-of-sixteen instructions for the Am2910
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	Carry-In	Low order carry input to incrementer for microprogram counter
$\overline{RLD}$	Register Load	When LOW forces loading of register/counter regardless of instruction or condition
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs
CP	Clock Pulse	Triggers all internal state changes at LOW-to-HIGH edge
V_{CC}	+5 Volts	
GND	Ground	
Y_i	Microprogram Address Bit i	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB
$\overline{FULL}$	Full	Indicates that five items are on the stack
$\overline{PL}$	Pipeline Address Enable	Can select #1 source (usually Pipeline Register) as direct input source
$\overline{MAP}$	Map Address Enable	Can select #2 source (usually Mapping PROM or PLA) as direct input source
$\overline{VECT}$	Vector Address Enable	Can select #3 source (for example, Interrupt Starting Address) as direct input source

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150
Temperature (Ambient) Under Bias	−55°C to +125
Supply Voltage to Ground Potential	−0.5V to +7.(
DC Voltage Applied to Outputs for High Output State	−0.5 V to V_{CC} ma
DC Input Voltage	−0.5V to +5.!
DC Output Current, Into Outputs	30 n
DC Input Current	−30 mA to +5.0 n

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

MIL T_C = −55°C to +125°C V_{CC} = 5.0V ±10% MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.6mA, V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_{0-11}, I_{OL} = 12mA			0.5	Volts
			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$, $\overline{FULL}$, I_{OL} = 8mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-11}			−0.87	mA
			CI, $\overline{CCEN}$			−0.54	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$			−0.72	
			$\overline{CC}$			−1.31	
			CP			−2.14	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-11}			80	µA
			CI, $\overline{CCEN}$			30	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$			40	
			$\overline{CC}$			50	
			CP			100	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V			−50	µA
I_{OZH}			V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current	V_{CC} = MAX.	T_A = 25°C		195	320	mA
		Am2910PC, DC	T_A = 0°C to +70°C			344	
			T_A = +70°C			280	
		Am2910DM, FM	T_C = −55°C to +125°C			340	
			T_C = +125°C			227	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.

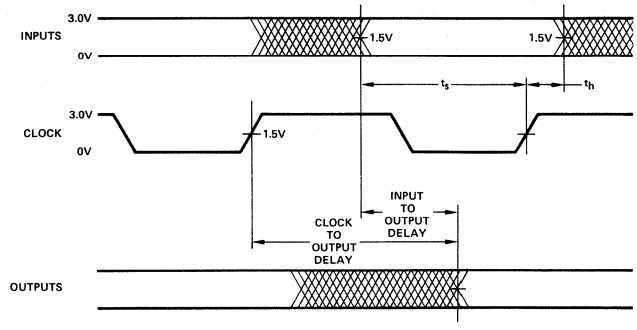

Figure 2. Switching Waveforms.

See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs. See Figure 5 for timing of a typical CCU cycle.

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Am2910 SWITCHING CHARACTERISTICS

The tables below define the Am2910 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns. All outputs have maximum DC loading.

I. TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_S	t_h
$D_i \rightarrow R$	9	4
$D_i \rightarrow PC$	34	3
I_0-I_3	64	0
$\overline{CC}$	46	0
$\overline{CCEN}$	49	0
CI	26	2
$\overline{RLD}$	18	2

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	14	–	–
I_0-I_3	40	27	–
$\overline{CC}$	21	–	–
$\overline{CCEN}$	23	–	–
CP (Note 2) I = 8, 9, 15	54	–	29
	79	–	29
CP All other I	46	–	29
$\overline{OE}$ (Note 3)	25/24	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	74	ns
	99	
Minimum Clock Period, I=14	60	ns

II. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2910PC,DC (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25, C_L = 50pF)

A. Set-up and Hold Times

Input	t_S	t_h
$D_i \rightarrow R$	24	6
$D_i \rightarrow PC$	58	4
I_0-I_3	104	0
$\overline{CC}$	80	0
$\overline{CCEN}$	80	0
CI	46	5
$\overline{RLD}$	36	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	20	–	–
I_0-I_3	70	51	–
$\overline{CC}$	43	–	–
$\overline{CCEN}$	45	–	–
CP (Note 2) I = 8, 9, 15	100	–	60
	125	–	60
CP All other I	55	–	60
$\overline{OE}$ (Note 3)	35/30	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	50	ns
Minimum Clock HIGH Time	35	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	138	ns
	163	
Minimum Clock Period, I=14	93	ns

III. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2910DM,FM (T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_S	t_h
$D_i \rightarrow R$	28	6
$D_i \rightarrow PC$	62	4
I_0-I_3	110	0
$\overline{CC}$	86	0
$\overline{CCEN}$	86	0
CI	58	5
$\overline{RLD}$	42	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	25	–	–
I_0-I_3	75	58	–
$\overline{CC}$	48	–	–
$\overline{CCEN}$	50	–	–
CP (Note 2) I = 8, 9, 15	106	–	67
	130	–	67
CP All other I	61	–	67
$\overline{OE}$ (Note 3)	40/30	–	–

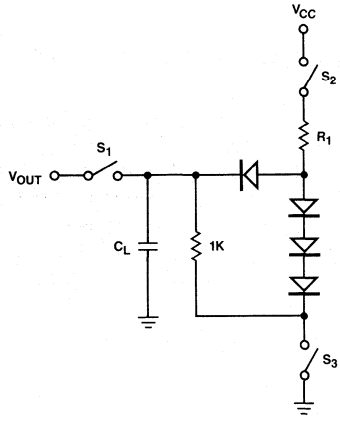
C. Clock Requirements (Note 1)

Minimum Clock LOW Time	58	ns
Minimum Clock HIGH Time	42	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	143	ns
	167	
Minimum Clock Period, I=14	100	ns

NOTES:
1. Clock periods for instructions not specified are determined by external conditions.
2. These instructions are conditional on the counter. Use the shorter specified delay times if the previous instruction could produce no change in the counter or could only decrement the counter. Use the longer delays from CP to outputs if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.
3. Enable/Disable. Disable times measured to 0.5V change on output voltage level with C_L = 5.0pF.

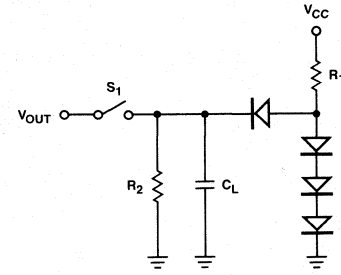
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2910

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTUPT LOADS FOR Am2910

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	$Y_{0\text{-}11}$	A	300	1K
5	$\overline{VECT}$	B	470	1.5K
6	$\overline{PL}$	B	470	1.5K
7	$\overline{MAP}$	B	470	1.5K
16	$\overline{FULL}$	B	470	1.5K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

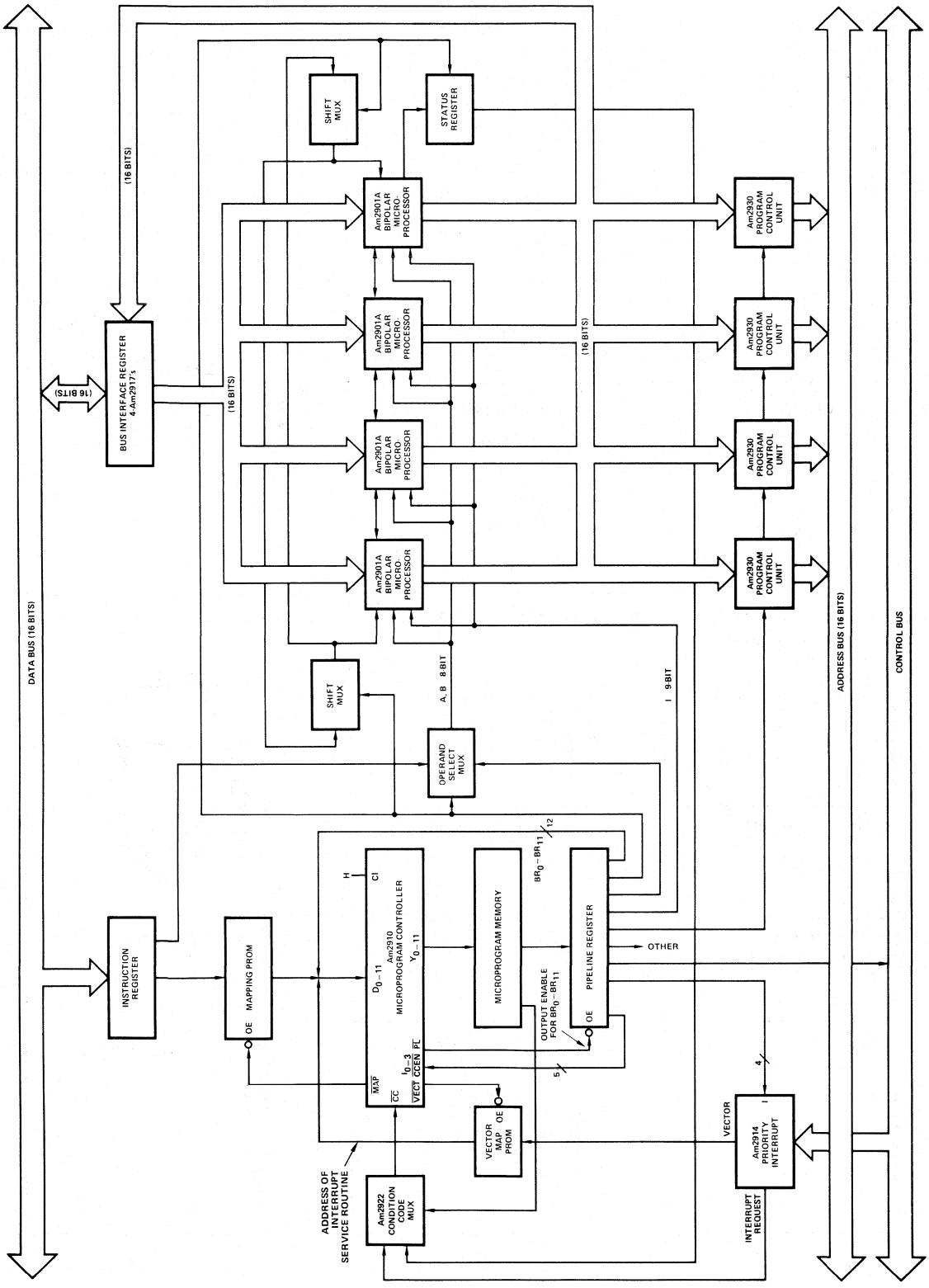


Figure 3. Typical Bipolar Microcomputer Using Am2910.

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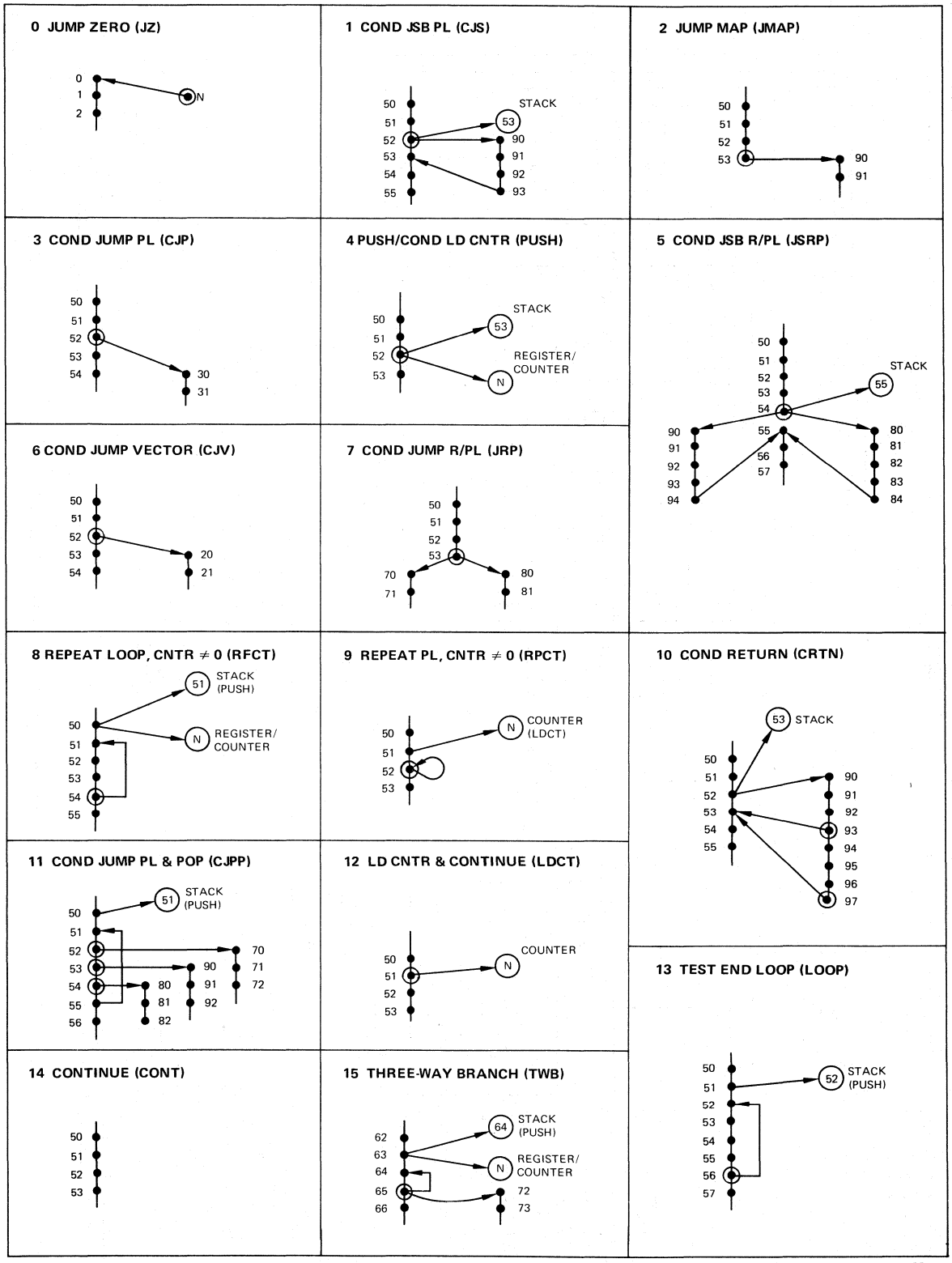


Figure 4. Am2910 Execution Examples.

THE Am2910 INSTRUCTION SET

The Am2910 provides 16 instructions which select the address of the next microinstruction to be executed. Four of the instructions are unconditional – their effect depends only on the instruction. Ten of the instructions have an effect which is partially controlled by an external, data-dependent condition. Three of the instructions have an effect which is partially controlled by the contents of the internal register/counter. The instruction set is shown in Table I. In this discussion it is assumed that C_i is tied HIGH.

In the ten conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is LOW, the test is considered to have been passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ HIGH, which unconditionally forces the action specified in the name; that is, it forces a pass. Other ways of using $\overline{CCEN}$ include (1) tying it HIGH, which is useful if no microinstruction is data-dependent; (2) tying it LOW if data-dependent instructions are never forced unconditionally; or (3) tying it to the source of Am2910 instruction bit I_0, which leaves instructions 4, 6, and 10 as data-dependent but makes others unconditional. All of these tricks save one bit of microcode width.

The effect of three instructions depends on the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected. These instructions are useful for executing a microinstruction loop a known number of times. Instruction 15 is affected both by the external condition code and the internal register/counter.

Perhaps the best technique for understanding the Am2910 is to simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, Figure 4 is included and depicts examples of all 16 instructions.

The examples given in Figure 4 should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed. For example, the CONTINUE instruction, instruction number 14, as shown in Figure 4, simply means that the contents of microprogram memory word 50 is executed, then the contents of word 51 is executed. This is followed by the contents of microprogram memory word 52 and the contents of microprogram memory word 53. The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word is in the pipeline register. While no special symbology is used for the conditional instructions, the text to follow will explain what the conditional choices are in each example.

It might be appropriate at this time to mention that AMD has a microprogram assembler called AMDASM, which has the capability of using the Am2910 instructions in symbolic representation. AMDASM's Am2910 instruction symbolics (or mnemonics) are given in Figure 4 for each instruction and are also shown in Table I.

Instruction 0, JZ (JUMP and ZERO, or RESET) unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.

Instruction 1 is a CONDITIONAL JUMP-TO-SUBROUTINE via the address provided in the pipeline register. As shown in Figure 4, the machine might have executed words at address 50, 51, and 52. When the contents of address 52 is in the pipeline register, the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead. Thus, the CONDITIONAL JUMP-TO-SUBROUTINE instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the TEST input is such that location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.

Instruction 2 is the JUMP MAP instruction. This is an unconditional instruction which causes the $\overline{MAP}$ output to be enabled so that the next microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine. In the example of Figure 4, microinstructions at locations 50, 51, 52, and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained in the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed.

Instruction 3, CONDITIONAL JUMP PIPELINE, derives its branch address from the pipeline register branch address value (BR_0 – BR_{11} in Figure 2). This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, state machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some function. This usually has the effect of resetting the input being tested until some point in the future. Figure 4 shows the conditional jump via the pipeline register address at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or location 30 in this example. If the test is passed, the value currently in the pipeline register (30) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is 53.

Instruction 4 is the PUSH/CONDITIONAL LOAD COUNTER instruction and is used primarily for setting up loops in microprogram firmware. In Figure 4, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field. Thus, a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will

THE Am2910 INSTRUCTION SET (Cont.)

describe how to use the pushed value and the register/counter for looping.

Instruction 5 is a CONDITIONAL JUMP-TO-SUBROUTINE via the register/counter or the contents of the PIPELINE register. As shown in Figure 4, a PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A return-from-subroutine (instruction number 10) returns the microprogram flow to address 55. In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Let's assume that the branch address fields of instruction 53 contain the value 90 so that it will be in the Am2910 register/counter when the contents of address 54 are in the pipeline register. This requires that the instruction at address 53 load the register/counter. Now, during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value = 90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value = 80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.

Instruction 6 is a CONDITIONAL JUMP VECTOR instruction which provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the Am2910 output, $\overline{VECT}$ is used to control a three-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter. In the example of Figure 4, if the CONDITIONAL JUMP VECTOR instruction is contained at location 52, execution will continue at vector address 20 if the $\overline{CC}$ input is LOW and the microinstruction at address 53 will be executed if the $\overline{CC}$ input is HIGH.

Instruction 7 is a CONDITIONAL JUMP via the contents of the Am2910 REGISTER/COUNTER or the contents of the PIPELINE register. This instruction is very similar to instruction 5; the conditional jump-to-subroutine via R or PL. The major difference between instruction 5 and instruction 7 is that no push onto the stack is performed with 7. Figure 4 depicts this instruction as a branch to one of two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 is being executed. As the contents of address 53 is clocked into the pipeline register, the value 70 is loaded into the register/counter in the Am2910. The value 80 is available when the contents of address 53 is in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.

Instruction 8 is the REPEAT LOOP, COUNTER ≠ ZERO instruction. This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/counter is decremented, and the address of the next microinstruction is taken from the top of the stack. If the register counter contains zero, the loop exit condition is occuring; control falls through to the next sequential microinstruction by selecting μPC; the stack is POP'd by decrementing the stack pointer, but the contents of the top of the stack are thrown away.

An example of the REPEAT LOOP, COUNTER ≠ ZERO instruction is shown in Figure 4. In this example, location 50 most likely would contain a PUSH/CONDITIONAL LOAD COUNTER instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

In this example, since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper value to be loaded by the instructions at address 50 is one less than the desired number of passes through the loop. This method allows a loop to be executed 1 to 4096 times. If it is desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

Instruction 9 is the REPEAT PIPELINE REGISTER, COUNTER ≠ ZERO instruction. This instruction is similar to instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested five deep. This instruction's operation is very similar to that of instruction 8. The differences are that on this instruction, a failed test condition causes the source of the next microinstruction address to be the D inputs; and, when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

In the example of Figure 4, the REPEAT PIPELINE, COUNTER ≠ ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number 12). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multi-instruction loops can be performed in this manner for a fixed number of times as determined by the counter.

Instruction 10 is the conditional RETURN-FROM-SUBROUTINE instruction. As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed. If the test is failed, the next sequential microinstruction is performed. The example in Figure 4 depicts the use of the conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes. This example first shows a jump-to-subroutine at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test is failed, the next microinstruction at address 94 will be executed. The program will continue to address 97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force

THE Am2910 INSTRUCTION SET (Cont.)

$\overline{CCEN}$ HIGH, disabling the test and the forced PASS causes an unconditional return.

Instruction 11 is the CONDITIONAL JUMP PIPELINE register address and POP stack instruction. This instruction provides another technique for loop termination and stack maintenance. The example in Figure 4 shows a loop being performed from address 55 back to address 51. The instructions at locations 52, 53, and 54 are all conditional JUMP and POP instructions. At address 52, if the $\overline{CC}$ input is LOW, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55. An instruction sequence as described here, using the CONDITIONAL JUMP PIPELINE and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level.

Instruction 12 is the LOAD COUNTER AND CONTINUE instruction, which simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a branch address or a counter value depending upon the microinstruction being executed. There are altogether three ways of loading the counter — the explicit load by this instruction 12; the conditional load included as part of instruction 4; and the use of the $\overline{RLD}$ input along with any instruction. The use of $\overline{RLD}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power, at the expense of one bit of microinstruction width. This instruction 12 is exactly equivalent to the combination of instruction 14 and $\overline{RLD}$ LOW. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RLD}$.

Instruction 13 is the TEST END-OF-LOOP instruction, which provides the capability of conditionally exiting a loop at the bottom; that is, this is a conditional instruction that will cause the microprogram to loop, via the file, if the test is failed else to continue to the next sequential instruction. The example in Figure 4 shows the TEST END-OF-LOOP microinstruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential microinstruction at address 57 is executed, which also causes the stack to be POP'd; thus, accomplishing the required stack maintenance.

Instruction 14 is the CONTINUE instruction, which simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever there is nothing better to do.

Instruction 15, THREE-WAY BRANCH, is the most complex. It provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack. Instruction 15 performs a decrement-and-branch-until-zero function similar to instruction 8. The next address is taken from the top of the stack until the count reaches zero; then the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of instruction 15 the test condition is passed, no branch is taken; the microprogram counter register furnishes the next address. When the loop is ended, either by the count becoming zero, or by passing the conditional test, the stack is POP'd by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.

The application of instruction 15 can enhance performance of a variety of machine-level instructions. For instance, (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

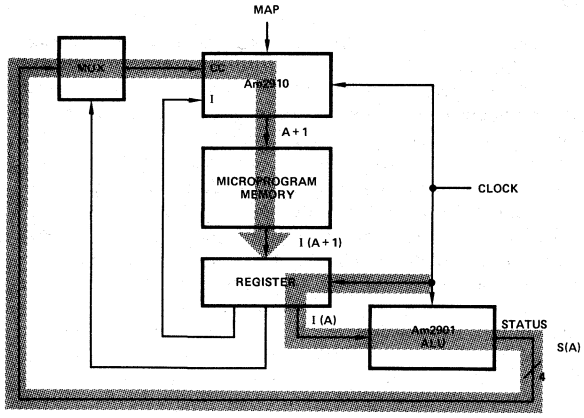
As one example, consider the case of a memory search instruction. As shown in Figure 4, the instruction at microprogram address 63 can be Instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before giving up. Location 64 contains a microinstruction which fetches the next operand from the memory area to be searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and also is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address. When the count becomes zero, the microprogram branches to location 72, which does whatever is necessary if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles this case. Whether the instruction ends by finding a match or not, the stack will have been POP'd once, removing the value 64 from the top of the stack.

OTHER ARCHITECTURES USING THE Am2910

(Shading shows path(s) which usually limit speed)

Figure 6.

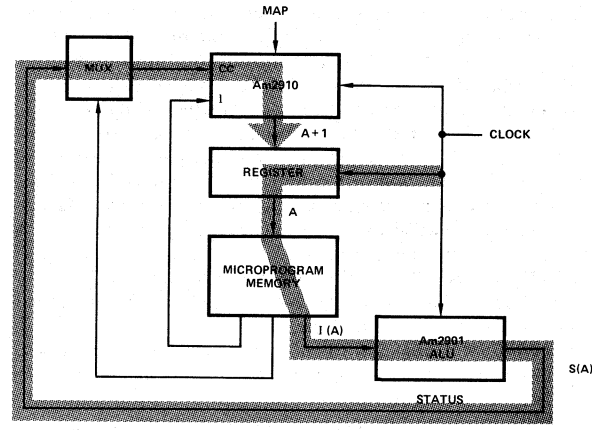
A. Instruction Based



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2901 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

MPR-114

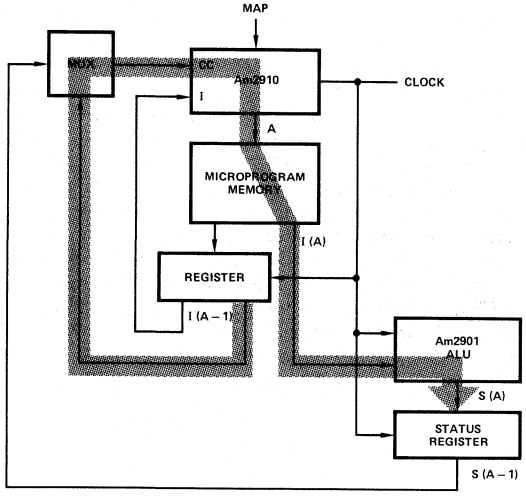
B. Addressed Based



The Register at the Am2910 output contains the address of the microinstruction being executed. The Microprogram Memory and Am2901 are in series in the critical path. This architecture provides about the same speed as the Instruction based architecture, but requires fewer register bits, since only the address (typically 10-12 bits) is stored instead of the instruction (typically 40-60 bits).

MPR-115

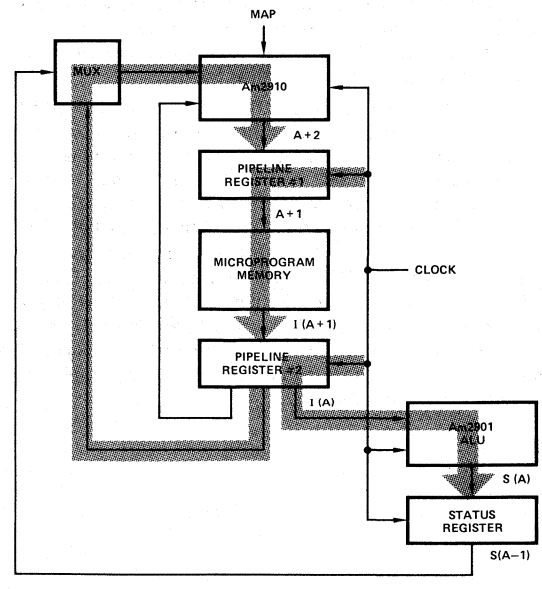
C. Data Based



The Status Register provides conditional Branch control based on results of previous ALU cycle. The Microprogram Memory and Am2901 are in series in the critical paths.

MPR-116

D. Two Level Pipeline Based



Two level pipeline provides highest possible speed. It is more difficult to program because the selection of a microinstruction occurs two instructions ahead of its execution.

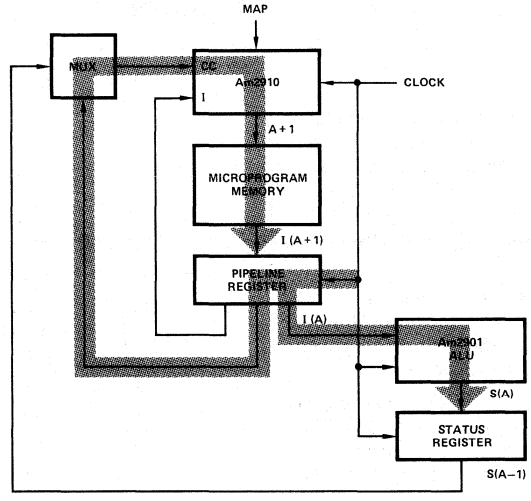
MPR-117

ARCHITECTURES USING THE Am2910

(Shading shows path(s) which usually limit speed)

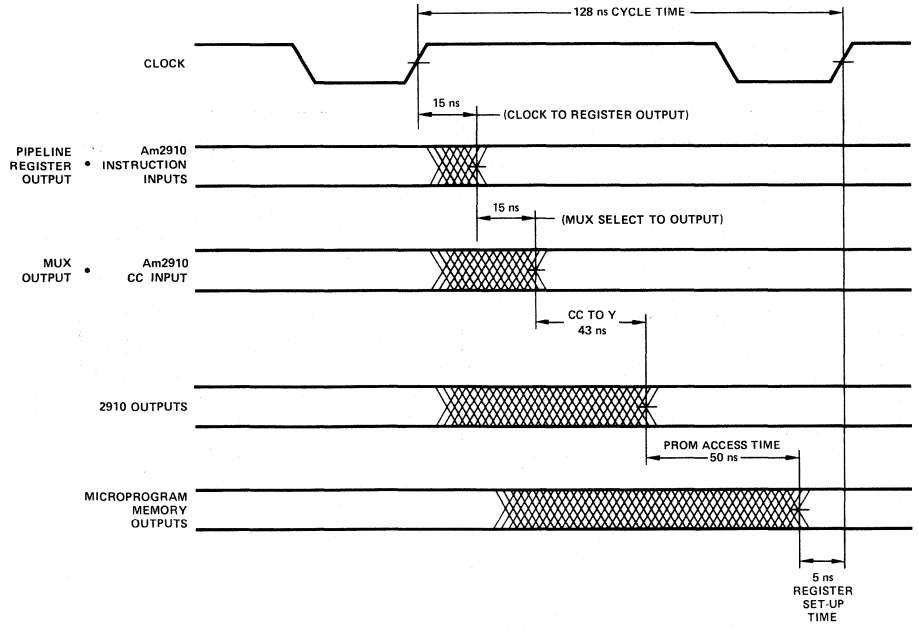
Figure 5.

One Level Pipeline Based
(Recommended)



One level pipeline provides better speed than most other architectures. The μProgram Memory and the Am2901 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs.

MPR-112



Typical CCU Cycle Timing Waveforms.

This drawing shows the timing relationships in the CCU illustrated above.

MPR-113

Am2912
Quad Bus Transceiver

Distinctive Characteristics

- Input to bus is inverting
- Quad high-speed open collector bus transceiver
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

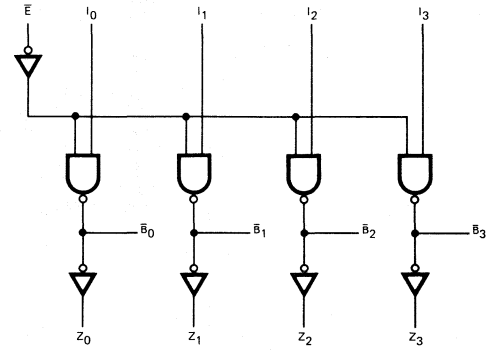
The Am2912 is a quad Bus Transceiver consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

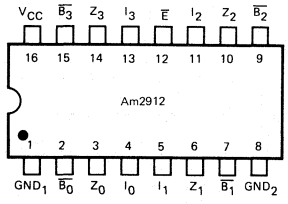
The Am2912 features advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

LOGIC DIAGRAM



BLI-061

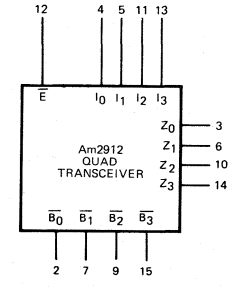
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-062

LOGIC SYMBOL



LIC-370

V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

BLI-063

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Am2912PC, DC, XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2912DM, FM, XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OH} = −1.0mA, V_{IN} = V_{IL} or V_{IH}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IL} or V_{IH}				0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V	Enable			20	µA
			Data			30	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V				100	µA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX. (Note 3)	MIL	−20		−55	mA
			COM'L	−18		−60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX., Enable = GND			45	70	mA

Bus Input/Output Characteristics

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA		0.33	0.5	Volts
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
			COM'L	I_{OL} = 40mA		0.33	0.5	
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.		V_O = 0.8V			−50	µA
			MIL	V_O = 4.5V			200	
			COM'L	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V, V_{CC} = MAX		MIL	2.4	2.0		Volts
				COM'L	2.25	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V, V_{CC} = MIN		MIL		2.0	1.6	Volts
				COM'L		2.0	1.75	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Data Input to Bus	R_B = 50Ω, C_B = 50pF (Note 1)		10	15	ns
t_{PHL}				10	15	
t_{PLH}	Enable Input to Bus			14	18	ns
t_{PHL}				13	18	
t_{PLH}	Bus to Receiver Out	R_B = 50Ω, R_L = 280Ω, C_B = 50pF (Note 1), C_L = 15pF		10	15	ns
t_{PHL}				10	15	
t_r	Bus	R_B = 50Ω, C_B = 50pF (Note 1)	4.0	10		ns
t_f	Bus		2.0	4.0		ns

Note 1. Includes probe and jig capacitance.

TRUTH TABLE

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

ORDERING INFORMATION

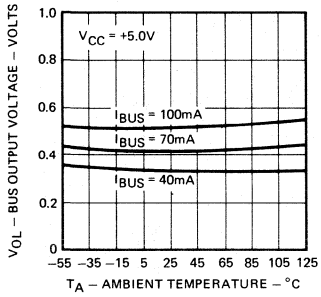
Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2912PC	P-16-1	C	C-1
AM2912DC	D-16-1	C	C-1
AM2912DC-B	D-16-1	C	B-1
AM2912DM	D-16-1	M	C-3
AM2912DM-B	D-16-1	M	B-3
AM2912FM	F-16-1	M	C-3
AM2912FM-B	F-16-1	M	B-3
AM2912XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2912XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

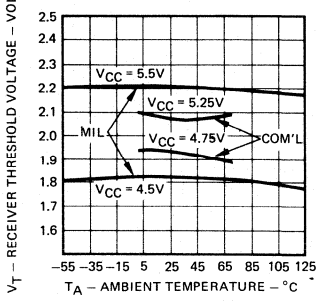
TYPICAL PERFORMANCE CURVES

Typical Bus Output Low Voltage Versus Ambient Temperature



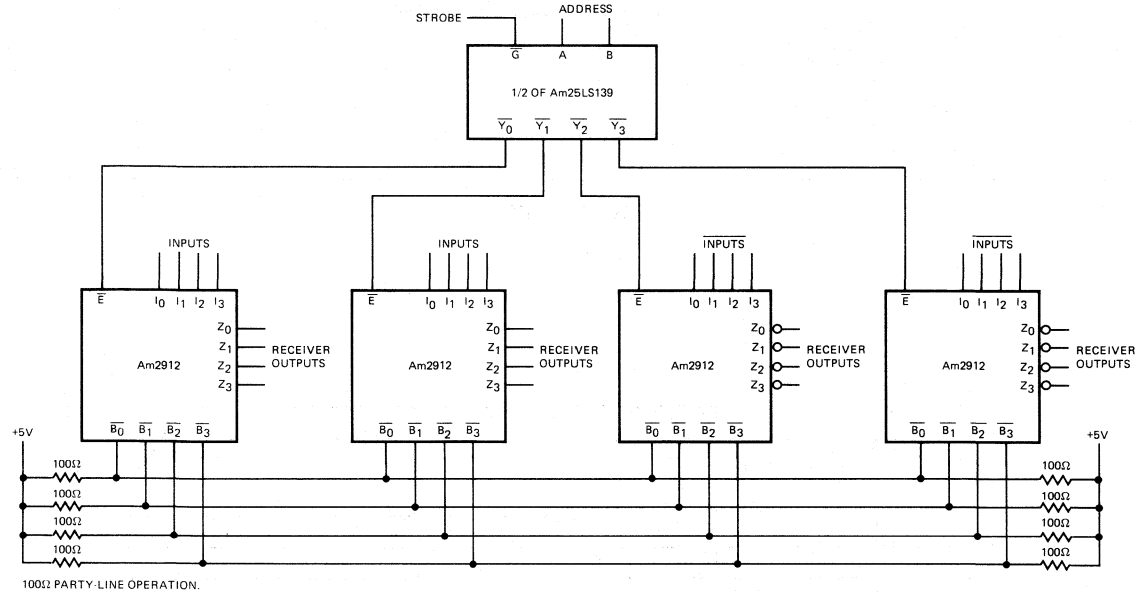
BLI-064

Receiver Threshold Variation Versus Ambient Temperature



BLI-065

TYPICAL APPLICATION

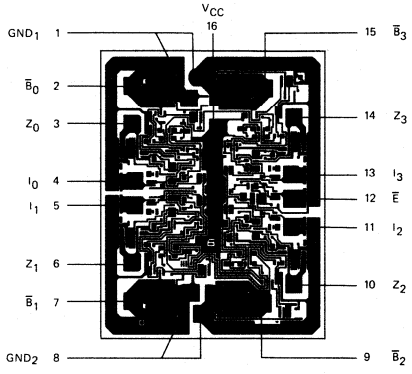


100Ω PARTY-LINE OPERATION.

BLI-066

Metallization and Pad Layout

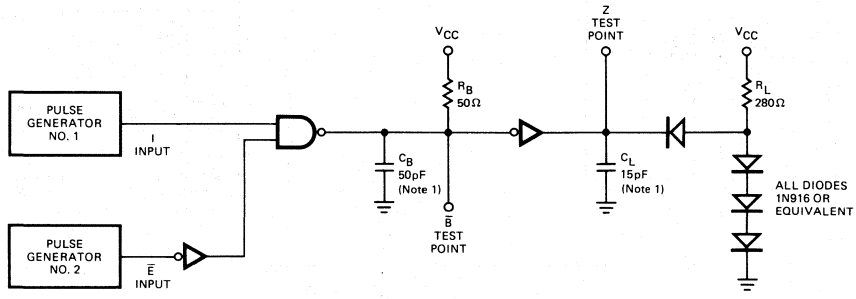
Am2912



DIE SIZE 0.059" X 0.075"

SWITCHING CHARACTERISTICS

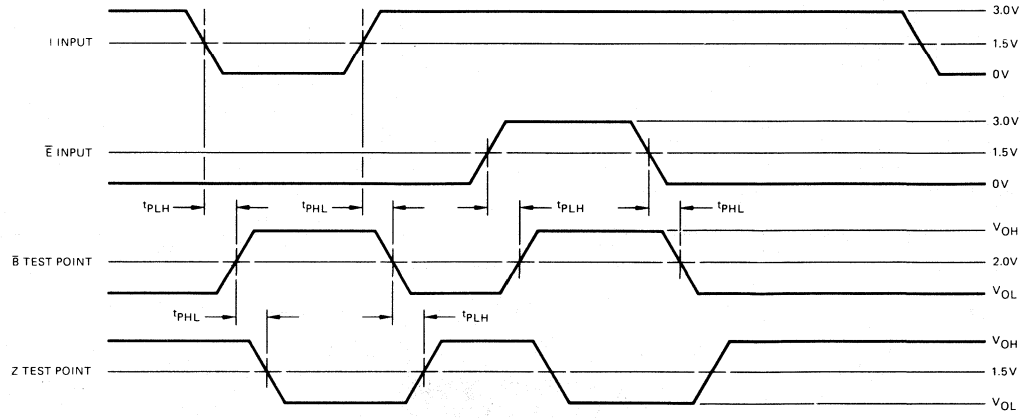
TEST CIRCUIT



BLI-067

Note 1. Includes Probe and Jig Capacitance.

WAVEFORMS



BLI-068

Am2913

Priority Interrupt Expander

Distinctive Characteristics

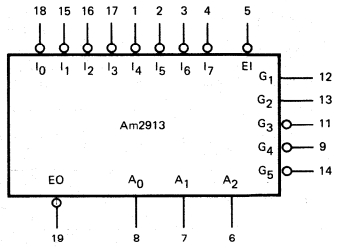
- Encodes eight lines to three-line binary
- Expands use of Am2914
- Cascadable
- Similar in function to Am54LS/74LS/25LS148/2513
- Gated three-state output
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Low-Power Schottky Priority Interrupt Expander is an extention of the Am2900 series of Bipolar Processor family and is used to expand and prioritize the output of the Am2914 Priority Interrupt circuit. Affording an increase of vectored priority interrupt in groups of eight, this unit accepts active LOW inputs and produces a three-state active HIGH output prioritized from active $\overline{I}_7$ to $\overline{I}_0$. The output is gated by five control signals, three active LOW and two active HIGH. Also provided is a cascade input ($\overline{EI}$) and Enable Output ($\overline{EO}$).

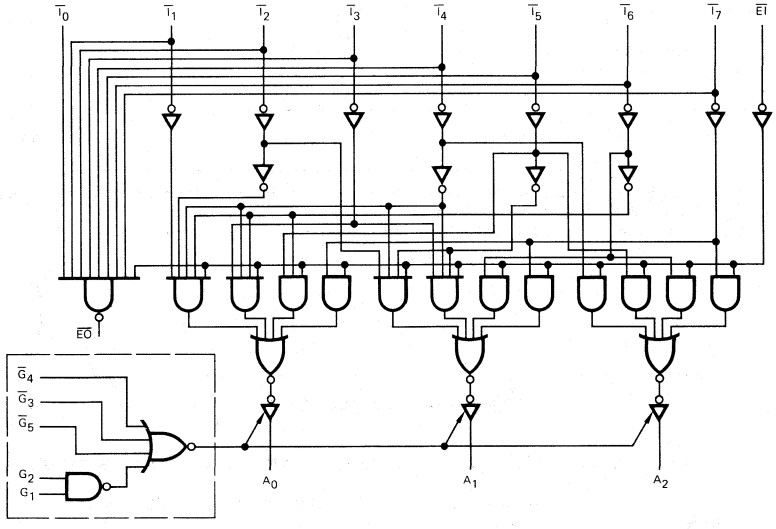
One Am2913 will accept and encode group signal lines from up to 8 Am2914's (64 levels of interrupt). Additional Am2913's may be used to encode more interrupt levels.

LOGIC SYMBOL



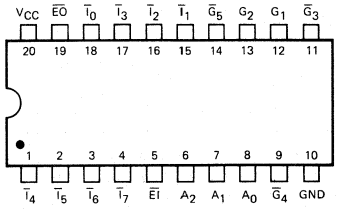
MPR-118

LOGIC DIAGRAM



MPR-119

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-120

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75V	MAX. = 5.25V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50V	MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.2		
			$\overline{EO}$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA (A_n$ Outputs)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				0.4	mA
			All others				0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				20	μA
			All others				40	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$	$\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				0.1	mA
			All others				0.2	
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				15	24	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs and outputs open.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2913PC	P-20	C	C-1
AM2913DC	D-20	C	C-1
AM2913DC-B	D-20	C	B-1
AM2913DM	D-20	M	C-3
AM2913DM-B	D-20	M	B-3
AM2913FM	F-20	M	C-3
AM2913FM-B	F-20	M	B-3
AM2913XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2913XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

MAXIMUM RATINGS (Above which the useful life may be impaired)

torage Temperature	−65°C to +150°C
emperature (Ambient) Under Bias	−55°C to +125°C
upply Voltage to Ground Potential Continuous	−0.5V to +7.0V
C Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
C Input Voltage	−0.5V to +7.0V
C Output Current, Into Outputs	30mA
C Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	$\overline{I}_i$ to A_n (In-phase)		17	25	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	$\overline{I}_i$ to A_n (Out-phase)		11	17	ns	
t_{PHL}			12	18		
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$		7.0	11	ns	
t_{PHL}			24	36		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		11	17	ns	
t_{PHL}			23	34		
t_{PLH}	$\overline{EI}$ to A_n		12	18	ns	
t_{PHL}			14	21		
t_{ZH}	G_1 or G_2 to A_n		23	40	ns	
t_{ZL}			20	37		
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n		20	30	ns	
t_{ZL}			18	27		
t_{HZ}	G_1 or G_2 to A_n		17	27	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			19	28		
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n		16	24	ns	
t_{LZ}			18	27		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2913 COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am2913 COM'L Max.	Am2913 MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am2913 MIL Max.	Units	Test Conditions
t_{PLH}	$\overline{I}_i$ to A_n (In-phase)		31		37	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			30		34		
t_{PLH}	$\overline{I}_i$ to A_n (Out-phase)		22		27	ns	
t_{PHL}			22		25		
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$		15		18	ns	
t_{PHL}			48		60		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		19		21	ns	
t_{PHL}			46		57		
t_{PLH}	$\overline{EI}$ to A_n		22		25	ns	
t_{PHL}			27		32		
t_{ZH}	G_1 or G_2 to A_n		42		49	ns	
t_{ZL}			43		49		
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n		36		43	ns	
t_{ZL}			35		43		
t_{HZ}	G_1 or G_2 to A_n		34		40	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			34		40		
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n		30		35	ns	
t_{LZ}			31		35		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Note: i = 0 to 7
n = 0 to 2

DEFINITIONS OF FUNCTIONAL TERMS

A0, A1, A2	Three-state, active high encoder outputs
$\overline{EI}$	Enable input provided to allow cascaded operation
$\overline{EO}$	Enable output provided to enable the next lower order priority chip
G_1, G_2	Active high three-state output controls
$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$	Active low three-state output controls
$\overline{I}_{0\text{-}7}$	Active low encoder inputs

TRUTH TABLE

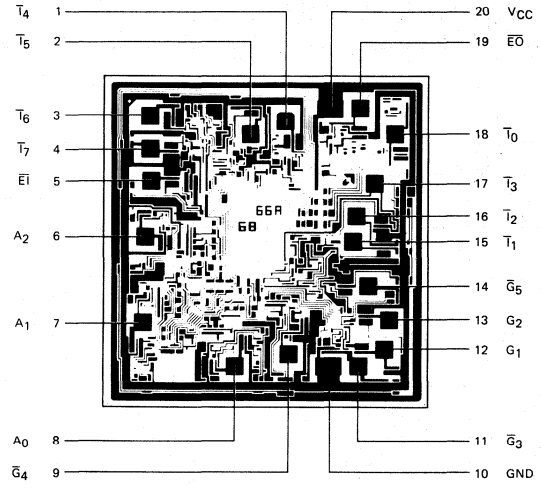
Inputs									Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G_1 = H, G_2 = H, G_3 = L, G_4 = L, G_5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

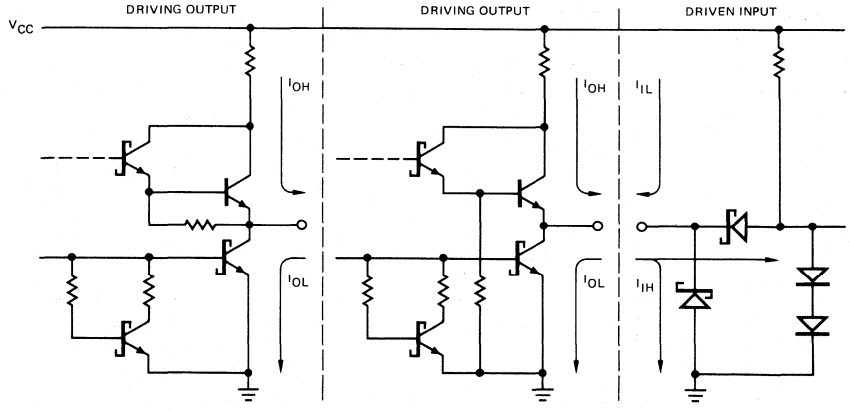
Z = HIGH Impedance

Metallization and Pad Layout



DIE SIZE 0.082" X 0.085"

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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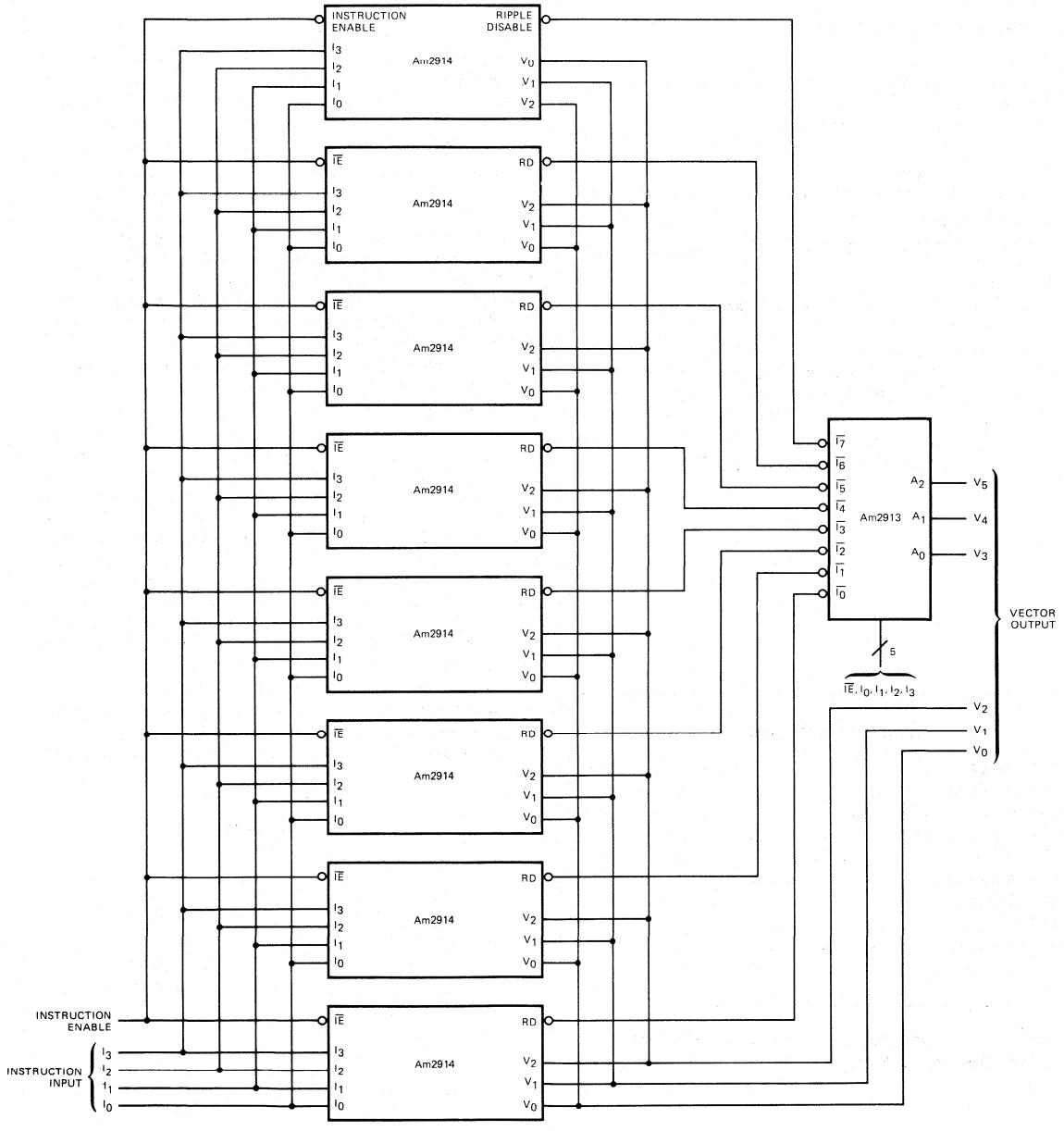


Shown above is the connection of the instruction lines and vector output lines in a 64-input priority interrupt system. The Am2913 is used to encode the most significant bits associated with the vector output.

MPR-122

Am2914

Vectored Priority Interrupt Controller

DISTINCTIVE CHARACTERISTICS

- Accepts 8 interrupt inputs
  Interrupts may be pulses or levels and are stored internally
- Built-in mask register
  Six different operations can be performed on mask register
- Built-in status register
  Status register holds code for lowest allowed interrupt
- Vectored output
  Output is binary code for highest priority un-masked interrupt
- Expandable
  Any number of Am2914's may be stacked for large interrupt systems
- Microprogrammable
  Executes 16 different microinstructions
  Instruction enable pin aids in vertical microprogramming
- High-speed operation
  Delay from an interrupt clocked into the interrupt register to interrupt request output is typically 60 ns

TABLE OF CONTENTS

For applications information, see Chapter VI of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

FUNCTIONAL DESCRIPTION

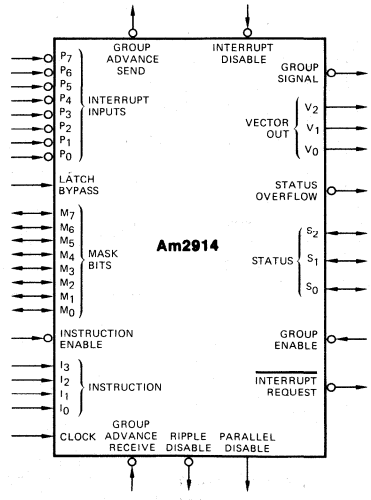
The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The high-speed of the Am2914 makes it ideal for use in Am2900 family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on 8 interrupt input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the edge-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Considerable flexibility is provided for controlling the mask register. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the results are sent to an 8-input priority encoder, which produces a three bit encoded vector representing the highest numbered input which is not masked.

An internal status register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the status register are compared with the output of the priority encoder, and an interrupt request output will occur if the vector is greater than or equal to status. Whenever a vector is read from the Am2914 the status register is automatically updated to point to one level higher than the vector read. (The status register can be loaded externally or read out at any time using the S pins.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A status overflow output indicates that an interrupt has been read at the highest priority.

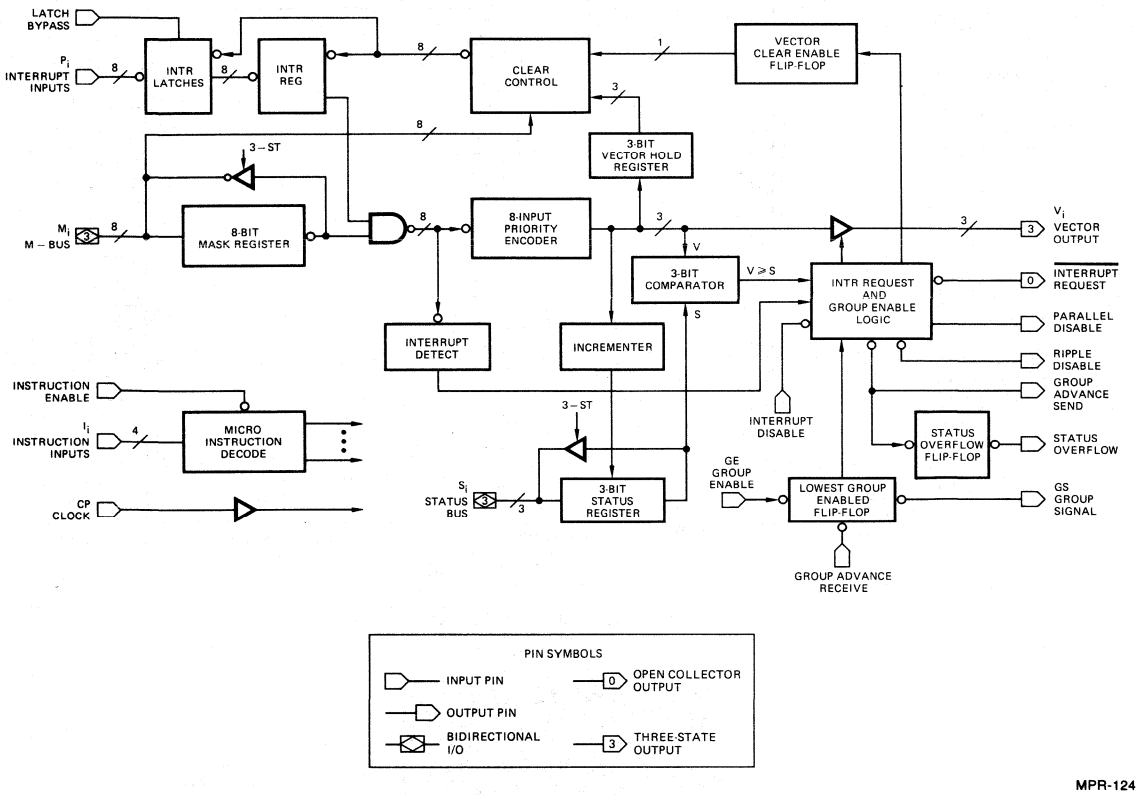
The Am2914 is controlled by a 4-bit instruction field I_0-I_3. The command on the instruction lines is executed if IE is LOW and is ignored if IE is HIGH, allowing the 4 I bits to be shared with other devices.

LOGIC SYMBOL



MPR-123

BLOCK DIAGRAM



MPR-124

BLOCK DIAGRAM DESCRIPTION

The Microinstruction Decode circuitry decodes the Interrupt Microinstructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal.

The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector is used for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus the Status Register always points to the lowest level at which an interrupt will be accepted.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of 2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

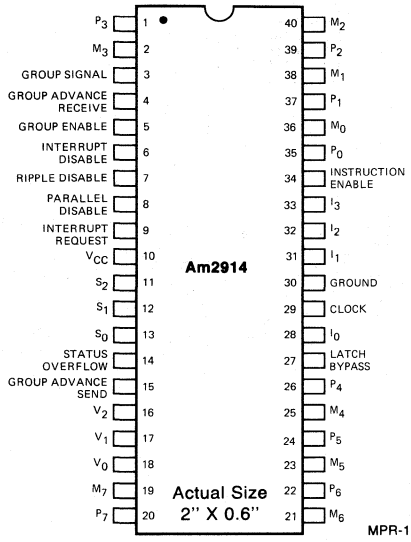
The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this group. When it is set, it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

CONNECTION DIAGRAMS — Top Views

DIP



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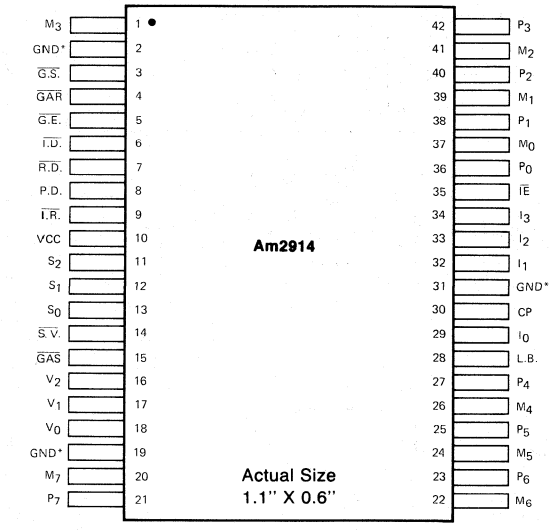
Flat Package

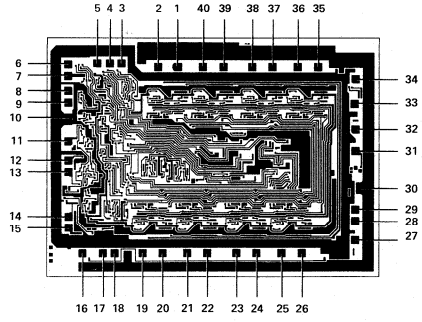


MPR-126

*Note: GND's and pins 2, 19, 31 must all be tied together externally.

Note: Pin 1 is marked for orientation.

Metallization and Pad Layout



DIE SIZE
0.133" X 0.187"
Numbers correspond to DIP pin-out.

TABLE I
MICROINSTRUCTION SET FOR Am2914 PRIORITY INTERRUPT CIRCUIT

Decimal $I_3I_2I_1I_0$	Mnemonic	Instruction
		Mask Register Functions
14	LDM	Load mask register from M bus
7	RDM	Read mask register to M bus
12	CLRM	Clear mask register (enables all priorities)
8	SETM	Set mask register (inhibits all interrupts)
10	BCLRM	Bit clear mask register from M bus
11	BSETM	Bit set mask register from M bus
		Status Register Functions
9	LDSTA	Load status register from S bus and LGE flip-flop from GE input
6	RDSTA	Read status register to S bus
		Interrupt Request Control
15	ENIN	Enable interrupt request
13	DISIN	Disable interrupt request
		Vectored Output
5	RDVC	Read vector output to V outputs, load V+1 into status register, load V into vector hold register and set vector clear enable flip-flop.
		Priority Interrupt Register Clear
1	CLRIN	Clear all interrupts
3	CLRMR	Clear interrupts from mask register data (uses the M bus)
2	CLRMB	Clear interrupts from M bus data
4	CLRVC	Clear the individual interrupt associated with the last vector read
		Master Clear
0	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request.

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			Am2914PC, DC	Am2914DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100% *	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/sec	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups. Maximum accept number is 3		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for Am2914PC.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2914PC	P-40	C	C-1
AM2914DC	D-40	C	C-1
AM2914DC-B	D-40	C	B-2 (Note 4)
AM2914DM	D-40	M	C-3
AM2914DM-B	D-40	M	B-3
AM2914FM	F-42	M	C-3
AM2914FM-B	F-42	M	B-3
AM2914XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2914XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +110°C V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +110°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	+0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to 5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Temperature	V_{CC}
Am2914PC, DC	0°C to +70°C	4.75V to 5.25V
Am2914DM, FM	−55°C to +110°C	4.50V to 5.50V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Am2914XC T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V

Am2914XM T_C = −55°C to +110°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA		2.4			Volts
			COM'L, I_{OH} = −2.6mA		2.4			
I_{CEX}	Output Leakage Current for IR Output	V_{CC} = MIN., V_O = 5.5V					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	M_{0-7}				−0.15	mA
			S_{0-2}				−0.1	
			L. B.				−0.4	
			$\overline{I. D.}$				−2.0	
			$\overline{IE}$				−1.08	
			All Others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	M_{0-7}				150	µA
			S_{0-2}				100	
			$\overline{GE}$, $\overline{GAR}$				40	
			$\overline{IE}$				60	
			$\overline{I. D.}$				60	
			All Others				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZL}	Off-State Output Current	V_{CC} = MAX.	V_{OUT} = 0.5V	M_{0-7}			−150	µA
				S_{0-2}			−100	
				V_{0-2}			−50	
I_{OZH}			V_{OUT} = 2.4V	M_{0-7}			150	
				S_{0-2}			100	
				V_{0-2}			50	
I_{CC}	Power Supply Current	V_{CC} = 5.0V, 25°C				170	−	mA
		V_{CC} = MAX.	COM'L	0°C			305	
				70°C			250	
			MIL	−55°C			310	
				110°C			200	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS AT 25°C AND 5.0 VOLTS

Note: Guaranteed limits at 25°C and 5.0V are group A, subgroup 9 tests
All outputs fully loaded. C_L = 50pF. Measurements made at 1.5V with
input levels of 0V and 3.0V. All numbers are in ns.
For interrupt request output, R_L = 470Ω

TABLE I. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	GUARANTEED
Minimum Clock LOW Time	30
Minimum Clock HIGH Time	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	25
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	10

TABLE II. COMBINATIONAL PROPAGATION DELAYS (ns)

	TYPICAL						GUARANTEED					
To Output / From Input	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	36	40	40	–	–	30	48	55	55	–	–	47
I_{0123}	36	40	40	–	–	30	48	55	55	–	–	47
Irpt. Disable	–	–	25	35	8	19	–	–	37	42	18	25

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TABLE III. DELAYS FROM CLOCK TO OUTPUTS (ns)

Clock Path	TYPICAL							GUARANTEED						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Mask Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Status Register	45	55	28	31	37	–	–	59	74	57	57	58	–	–
Lowest Group Enabled Flip-Flop	–	–	22	25	–	–	17	–	–	42	45	–	–	32
Irpt Request Enable Flip-Flop	–	40	–	–	–	–	–	–	56	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	17	–	–	–	–	–	–	30	–

TABLE IV. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	GUARANTEED	
	Set-up Time	Hold Time
S-Bus	11	8
M-Bus	11	8
$\overline{P_0}$-$\overline{P_7}$	11	6
Latch Bypass	16	0
$\overline{IE}$ I_{0123} (See Note)	46 t_{pwL} + 29	0
$\overline{GE}$	11	11
$\overline{GAR}$	11	11
$\overline{Irpt\ Disable}$	35	0
P_0-P_7 Hold Time Relative to LB	–	21

Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

(Group A, subgroup 10 and 11 tests and limits)

All outputs fully loaded, C_L = 50pF. Measurements made at 1.5V with input levels of 0V and 3.0V. For Interrupt Request Output, R_L = 470Ω.

TABLE V. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%	Am2914DM, FM, XM T_C = –55°C to +110°C, 5V ± 10%
Minimum Clock LOW Time	30	30
Minimum Clock HIGH Time	30	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	40	40
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	8	8
Minimum Clock Period, $\overline{IE}$ = H on current cycle and previous cycle	50	55
Minimum Clock Period, $\overline{IE}$ = L on current cycle or previous cycle	100	110

TABLE VI. MAXIMUM COMBINATIONAL PROPAGATION DELAYS (ns)

	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%						Am2914DM, FM, XM T_C = –55°C to +110°C, 5V ± 10%					
To Output / From Input	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	52	60	65	–	–	56	60	68	70	–	–	62
I_{0123}	52	60	65	–	–	56	60	68	70	–	–	62
Irpt. Disable	–	–	45	52	20	30	–	–	48	60	22	33

TABLE VII. MAXIMUM DELAYS FROM CLOCK TO OUTPUTS (ns)

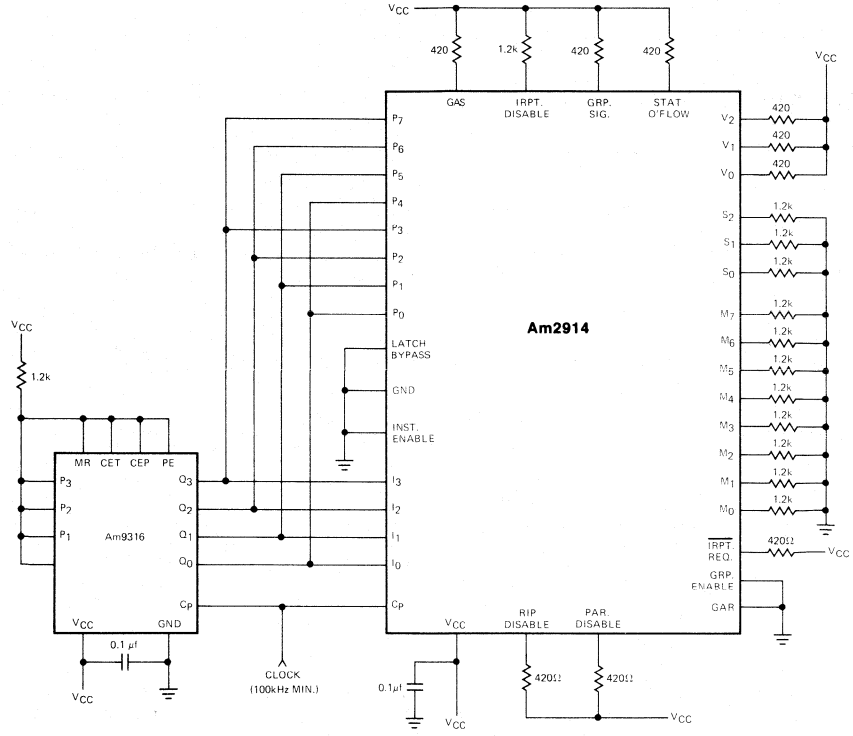
Clock Path	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%							Am2914DM, FM, XM T_C = –55°C to +110°C, 5V ± 10%						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Mask Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Status Register	67	88	63	63	70	–	–	73	96	66	66	76	–	–
Lowest Group Enabled Flip-Flop	–	–	48	52	–	–	38	–	–	54	58	–	–	45
Irpt Request Enable Flip-Flop	–	62	–	–	–	–	–	–	66	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	35	–	–	–	–	–	–	40	–

TABLE VIII. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%		Am2914DM, FM, XM T_C = –55°C to +110°C, 5V ± 10%	
	Set-Up Time	Hold Time	Set-Up Time	Hold Time
S-Bus	15	10	15	10
M-Bus	15	10	15	10
$\overline{P_0}$-$\overline{P_7}$	15	8	15	8
Latch Bypass	20	0	20	0
$\overline{IE}$ I_{0123} (See Note)	55 t_{pwL} + 33	0	55 t_{pwL} + 40	0
$\overline{GE}$	15	13	15	13
$\overline{GAR}$	15	13	15	13
$\overline{Irpt\ Disable}$	42	0	42	0
P_0-P_7 Hold Time Relative to LB	—	25	—	25

Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.



Am2914 Burn-in Circuit

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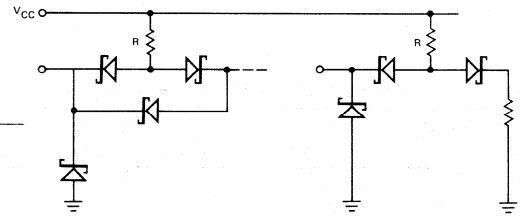
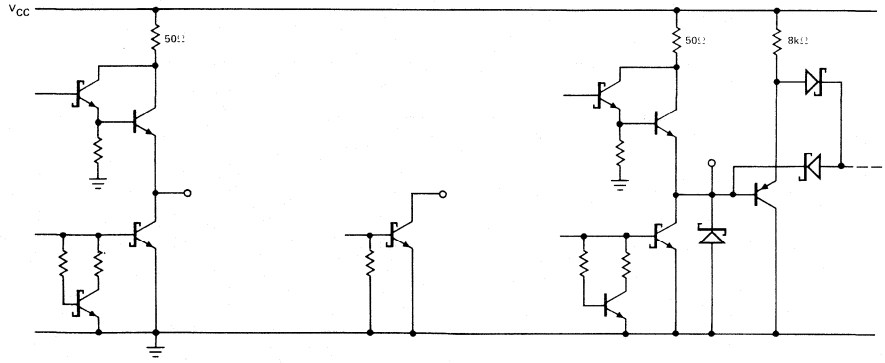
INPUT/OUTPUT CIRCUITS



INPUT	R
I_0-I_3, CP, $\overline{GE}$, $\overline{GAR}$	10K
$\overline{LB}$	20K
$\overline{IE}$	6.7K
$\overline{ID}$	4K

INPUT	R
$\overline{P_7}$-$\overline{P_0}$	10K



OUTPUTS		OUTPUT	OUTPUTS
V_0-V_3	$\overline{SO}$	$\overline{IR}$	M_0-M_7
$\overline{GAS}$	PD		S_0-S_3
$\overline{GS}$	$\overline{RD}$		

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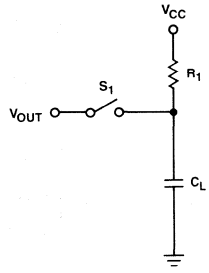
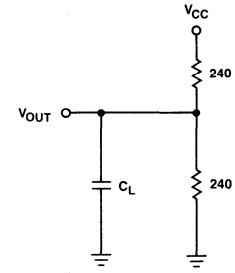
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2914

C. OPEN-COLLECTOR OUTPUTS



D. THREE-STATE OUTPUTS



Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2914

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
3	Group Signal	C	2K	–
4	Group Advance Receive	C	2K	–
7	Ripple Disable	C	2K	–
8	Parallel Disable	C	2K	–
9	Interrupt Request	C	330	–
13-11	S_{0-2}	D	240	240
14	Status Overflow	C	2K	–
18-16	V_{0-2}	D	240	240
–	M_{0-7}	D	240	240

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

A MICROPROGRAMMABLE, BIPOLAR, LSI INTERRUPT STRUCTURE USING THE Am2914

INTRODUCTION

Advanced Micro Devices' introduction of the Am2914 Vectored Priority Interrupt Controller now makes possible the structuring of a microprogrammable bipolar LSI interrupt system. The design engineer may use the Am2914 to simplify his design process, dramatically reduce the system cost, size and package count, and increase the speed, capability and reliability of his interrupt system.

The Am2914 is a modular, low cost, standard LSI component that may be microprogrammed to meet the requirements of specific applications. Today's engineer may utilize the Am2914 microprogrammability to provide functional flexibility and ease of engineering change, while taking advantage of its modularity to provide hardware regularity and future expansion capability.

THE INTERRUPT CONCEPT

In any state machine, a requirement exists for the efficient synchronization and response to asynchronous events such as power failure, machine malfunctions, control panel service requests, external timer signals, supervisory calls, program errors, and input/output device service requests. The merit of such an "asynchronous event handler" may be measured in terms of response time, system throughput, real time overhead, hardware cost and memory space required.

The simplest approach to asynchronous event handling is the poll approach. A status indicator is associated with each possible asynchronous event. The processor tests each indicator in sequence and, in effect, "asks" if service is required. This program-driven method is inefficient for a number of reasons. Much time is consumed polling when no service is required; programs must have frequent test points to poll indicators, and since indicators are polled in sequence, considerable time may elapse before the processor responds to an event. Thus, system throughput is low; real time overhead and response time are high, and a large memory space is required.

The interrupt method is a much more efficient way of servicing asynchronous requests. An asynchronous event requiring service generates an interrupt request signal to the processor. When the processor receives the interrupt request, it may suspend the program it is currently executing, execute an interrupt service routine which services the asynchronous request, then resume the execution of the suspended program. In this system, the execution of the service routine is initiated by an interrupt request; thus, the system is interrupt driven and service routines are executed only when service is requested. Although hardware cost may be higher in this type of system, it is more efficient since system throughput is higher, response time is faster, real time overhead is lower and less memory space is required.

INTERRUPT SYSTEM FUNCTIONAL DEFINITION

A complete and clear functional definition is key to the design of a good interrupt system. The following features are useful.

Multiple Interrupt Request Handling: Since interrupt requests are generated from a number of different sources, the interrupt system's ability to handle interrupt requests from several sources is important.

Interrupt Request Prioritization: Since the processor can service only one interrupt request at a time, it is important that the interrupt system has the ability to prioritize the requests and determine which has the highest priority.

Interrupt Service Routine "Nesting": This feature allows an interrupt service routine for a given priority request to be interrupted in turn, but only by a higher priority interrupt request. The service routine for the higher priority request is executed, then the execution of the interrupted service routine is resumed. If there are "n" interrupt requests, an "n" deep "nest" is possible.

Dynamic Interrupt Enabling/Disabling: The ability to enable/disable all interrupts "on the fly" under microprogram control can be used to prevent interruption of certain processes.

Dynamic Interrupt Request Masking: The ability to selectively inhibit or "mask" individual interrupt requests under microprogram control is useful.

Interrupt Request Vectoring: Many times, a particular interrupt request requires the execution of a unique interrupt service routine. For this reason, the generation of a unique binary coded vector for each interrupt request is very helpful. This vector can be used as a pointer to the start of a unique service routine.

Interrupt Request Priority Threshold: The ability to establish a priority threshold is valuable. In this type of operation, only those interrupt requests which have higher priority than a specified threshold priority are accepted. The threshold priority can be defined by microprogram or can be automatically established by hardware at the interrupt currently being serviced plus one. This automatic threshold prevents multiple interrupts from the same source. Also useful is the ability to read the threshold priority under microprogram control. Thus, the interrupt request being serviced may be determined by the microprogram.

Interrupt Request Clearing Flexibility: Flexibility in the method of clearing interrupt requests allows different modes of interrupt system operation. Of particular value are the abilities to clear the interrupt currently being serviced, clear all interrupts, or clear interrupts via a programmable mask register or bus.

Microprogrammability: Microprogrammability permits the construction of a general purpose or "universal" interrupt structure which can be microprogrammed to meet a specific application's requirements. The universality of the structure allows standardization of the hardware and amortization of the hardware development costs across a much broader user base. The end result is a flexible, low cost interrupt structure.

Hardware Modularity: Modular interrupt system hardware is beneficial in two ways. First, hardware modularity provides expansion capability. Additional modules may be added as the need to service additional requests arises. Secondly, hardware modularity provides a structural regularity which simplifies the system structure and also reduces the number of hardware part numbers.

Fast Interrupt System Response Time: Quick interrupt system response provides more efficient system operation. Fast response reduces real time overhead and increases overall system throughput.

INTERRUPT SYSTEM IMPLEMENTATION USING THE Am2914

The Am2914 provides all of the foregoing features on a single LSI chip. The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The Am2914's high speed is ideal for use in Am2900 Family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on eight Interrupt Input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses (HIGH-LOW-HIGH) on these lines, or the latch may be bypassed so that the request lines drive the D-inputs to the edge-triggered Interrupt Register directly. An eight-bit Mask Register is used to mask individual interrupts. Considerable flexibility is provided for controlling the Mask Register. Requests in the Interrupt Register (P_0-P_7) are ANDed with the corresponding bits in the mask register (M_0-M_7) and the results are sent to an eight-input priority encoder, which produces a three-bit encoded vector representing the highest priority input which is not masked.

An internal Status Register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the Status Register are compared with the output of the priority encoder, and an Interrupt Request output will occur if the vector is greater than or equal to the contents of the Status Register. Whenever a vector is read from the Am2914, the Status Register is automatically updated to point to one level higher than the vector read. (The Status Register can be loaded externally or read out at any time using the S-Bus.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A Status Overflow output indicates that an interrupt has been read at the highest priority.

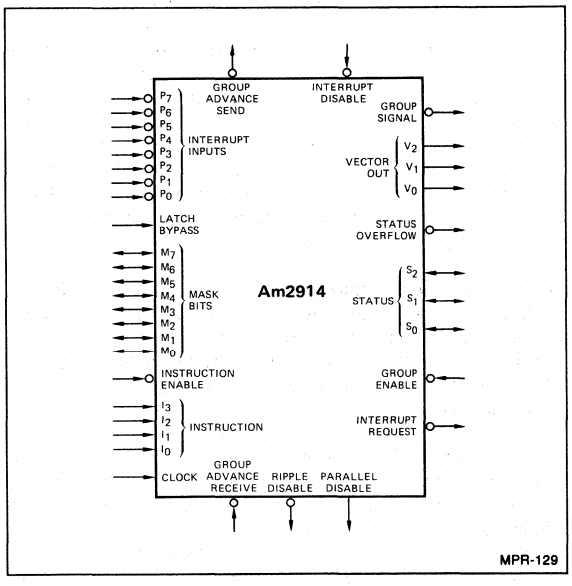


Figure 1. Am2914 Logic Symbol.

The Am2914 is controlled by a four-bit microinstruction field I_0-I_3. The microinstruction is executed if $\overline{IE}$ (Instruction Enable) is LOW and is ignored if $\overline{IE}$ is HIGH, allowing the four I bits to be shared with other functions. Sixteen different microinstructions are executed. Figure 2 shows the microinstructions and the microinstruction codes.

MICROINSTRUCTION DESCRIPTION	MICROINSTRUCTION CODE $I_3I_2I_1I_0$
MASTER CLEAR	0000
CLEAR ALL INTERRUPTS	0001
CLEAR INTERRUPTS FROM M-BUS	0010
CLEAR INTERRUPTS FROM MASK REGISTER	0011
CLEAR INTERRUPT, LAST VECTOR READ	0100
READ VECTOR	0101
READ STATUS REGISTER	0110
READ MASK REGISTER	0111
SET MASK REGISTER	1000
LOAD STATUS REGISTER	1001
BIT CLEAR MASK REGISTER	1010
BIT SET MASK REGISTER	1011
CLEAR MASK REGISTER	1100
DISABLE INTERRUPT REQUEST	1101
LOAD MASK REGISTER	1110
ENABLE INTERRUPT REQUEST	1111

Figure 2. Am2914 Microinstruction Set.

In this microinstruction set, the *Master Clear* microinstruction is selected as binary zero so that during a power up sequence, the microinstruction register in the microprogram control unit of the central processor can be cleared to all zeros. Thus, on the next clock cycle, the Am2914 will execute the *Master Clear* function. This includes clearing the Interrupt Latches and Register as well as the Mask Register and Status Register. The LGE flip-flop of the least significant group is set LOW because the Group Advance Receive input is tied LOW. All other Group Advance Receive inputs are tied to Group Advance Send outputs and these are forced HIGH during this instruction. This clear instruction also sets the Interrupt Request Enable flip-flop so that a fully interrupt driven system can be easily initiated from any interrupt.

The *Clear All Interrupts* microinstruction clears the Interrupt Latches and Register.

The *Clear Interrupts from Mask Register* microinstruction clears those Interrupt Latches and Register bits which have corresponding Mask Register bits set equal to one. The M-Bus is used by the Am2914 during the execution of this microinstruction and must be floating.

The *Clear Interrupts from M-Bus* microinstruction clears those Interrupt Latches and Register bits which have corresponding M-Bus bits set equal to one.

The *Clear Interrupt, Last Vector Read* microinstruction clears the Interrupt Latch and Register bit associated with the last vector read.

The *Read Vector* microinstruction is used to read the vector value of the highest priority request causing the interrupt. The vector outputs are three-state drivers that are enabled onto the $V_0V_1V_2$ bus during this instruction. This microinstruction also automatically loads the value "vector plus one" into the Status Register. In addition, this instruction sets the Vector Clear Enable flip-flop and loads the current vector value into the Vector Hold Register so that this value can be used by the *Clear Interrupt, Last Vector Read* microinstruction. This allows the user to read the vector associated with the interrupt, and at some later time clear the Interrupt Latch and Register bit associated with the vector read.

The *Load Status Register* microinstruction loads S-Bus data into the Status Register and also loads the LGE flip-flop from the Group Enable input.

During the *Read Status Register* microinstruction, the Status Register outputs are enabled onto the Status Bus (S_0-S_2). The Status Bus is a three-bit, bi-directional, three-state bus.

The *Load Mask Register* microinstruction loads data from the three-state, bi-directional M-Bus into the Mask Register.

The *Read Mask Register* microinstruction enables the Mask Register outputs onto the bi-directional, three-state M-Bus.

The *Set Mask Register* microinstruction sets all the bits in the Mask Register to one. This results in all interrupts being inhibited.

The entire Mask Register is cleared by the *Clear Mask Register* microinstruction. This enables all interrupts subject to the Interrupt Enable flip-flop and the Status Register.

The *Bit Clear Mask Register* microinstruction may be used to selectively clear individual Mask Register bits. This microinstruction clears those Mask Register bits which have corresponding M-Bus bits equal to one. Mask Register bits with corresponding M-Bus bits equal to zero are not affected.

The *Bit Set Mask Register* microinstruction sets those Mask Register bits which have corresponding M-Bus bits equal to one. Other Mask Register bits are not affected.

All Interrupt Requests may be disabled by execution of the *Disable Interrupt Request* microinstruction. This microinstruction resets an Interrupt Request Enable flip-flop on the chip.

The *Enable Interrupt Request* microinstruction sets the Interrupt Enable flip-flop. Thus, Interrupt Requests are enabled subject to the contents of the Mask and Status Registers.

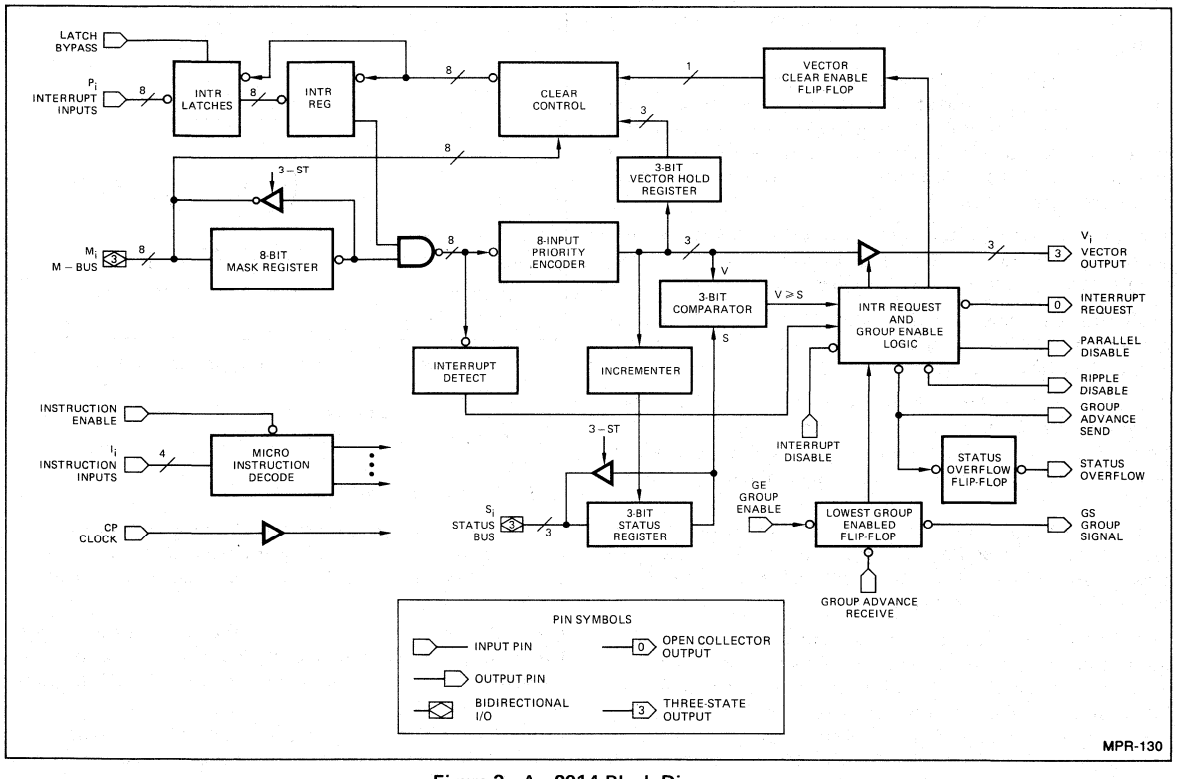


Figure 3. Am2914 Block Diagram.

Am2914 BLOCK DIAGRAM DESCRIPTION

The Am2914 block diagram is shown in Figure 3. The Micro-instruction Decode circuitry decodes the Interrupt Micro-instructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal if the Interrupt Input is LOW.

The Interrupt latches are set/reset latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M-Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector can be used later for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S-Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus, the Status Register points to a level one greater than the vector just read.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this chip. When it is set it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

The Am2914 can be microprogrammed in many different ways. Figure 4 shows an example interrupt sequence. The *Read Vector* microinstruction is necessary in order to read the interrupt priority level. Since vector plus one is automatically loaded into the Status Register when a *Read Vector* microinstruction is executed, the Status Register possibly will overflow and disable all interrupts. For this reason, the Status Register must be reloaded periodically. The other Am2914 microinstructions are optional.

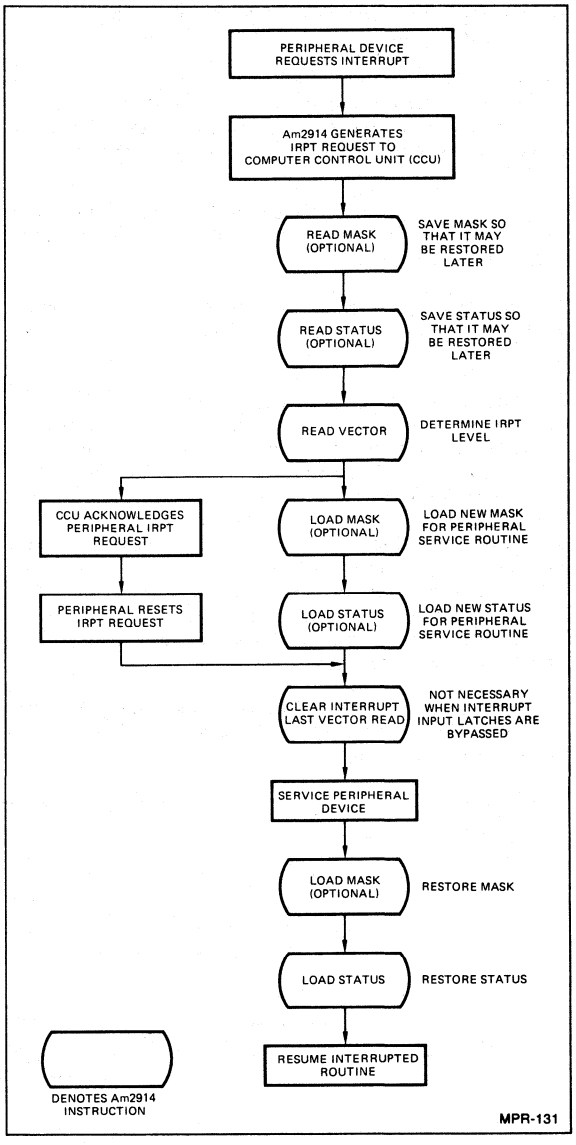


Figure 4. Example Interrupt Sequence.

CASCADING THE Am2914

A number of input/output signals are provided for cascading the Am2914 Vectored Priority Interrupt Encoder. A definition of these I/O signals and their required connections follows:

Group Signal ($\overline{GS}$) – This signal is the output of the Lowest Group Enabled flip-flop and during a Read Status microinstruction is used to generate the high order bits of the Status word.

Group Enable ($\overline{GE}$) – This signal is one of the inputs to the Lowest Group Enable flip-flop and is used to load the flip-flop during the Load Status microinstruction.

Group Advance Send ($\overline{GAS}$) – During a Read Vector microinstruction, this output signal is LOW when the highest priority vector (vector seven) of the group is being read. In a cascaded system Group Advance Send must be tied to the Group Advance Receive input of the next higher group in order to transfer status information.

Group Advance Receive ($\overline{GAR}$) – During a Master Clear or Read Vector microinstruction, this input signal is used with other internal signals to load the Lowest Group Enabled flip-flop. The Group Advance Receive input of the lowest priority group must be tied to ground.

Status Overflow ($\overline{SV}$) – This output signal becomes LOW after the highest priority vector (vector seven) of the group has been read and indicates the Status Register has overflowed. It stays LOW until a Master Clear or Load Status microinstruction is executed. The Status Overflow output of the highest priority group should be connected to the Interrupt Disable input of the same group and serves to disable all interrupts until new status is loaded or the system is master cleared. The Status Overflow outputs of lower priority groups should be left open (see Figure 7).

Interrupt Disable ($\overline{ID}$) – When LOW, this input signal inhibits the Interrupt Request output from the chip and also generates a Ripple Disable output.

Ripple Disable ($\overline{RD}$) – This output signal is used only in the Ripple Cascade Mode (see below). The Ripple Disable output is LOW when the Interrupt Disable input is LOW, the Lowest Group Enabled flip-flop is LOW, or an Interrupt Request is generated in the group. In the ripple cascade mode, the

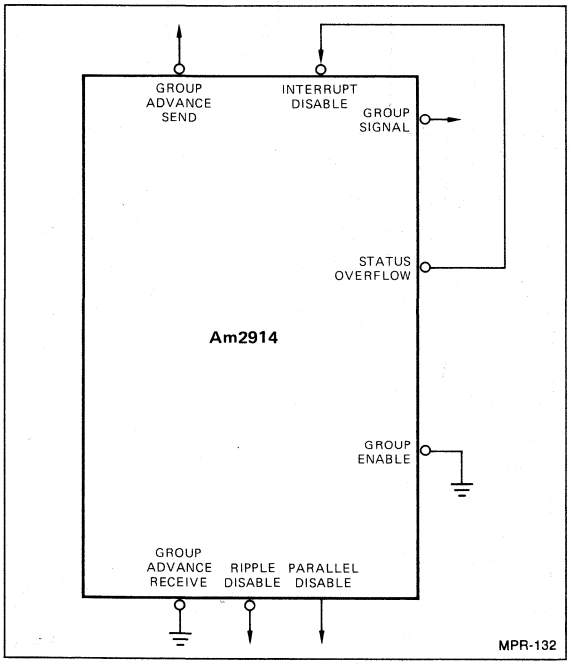


Figure 5. Cascade Lines Connection for Single Chip System.

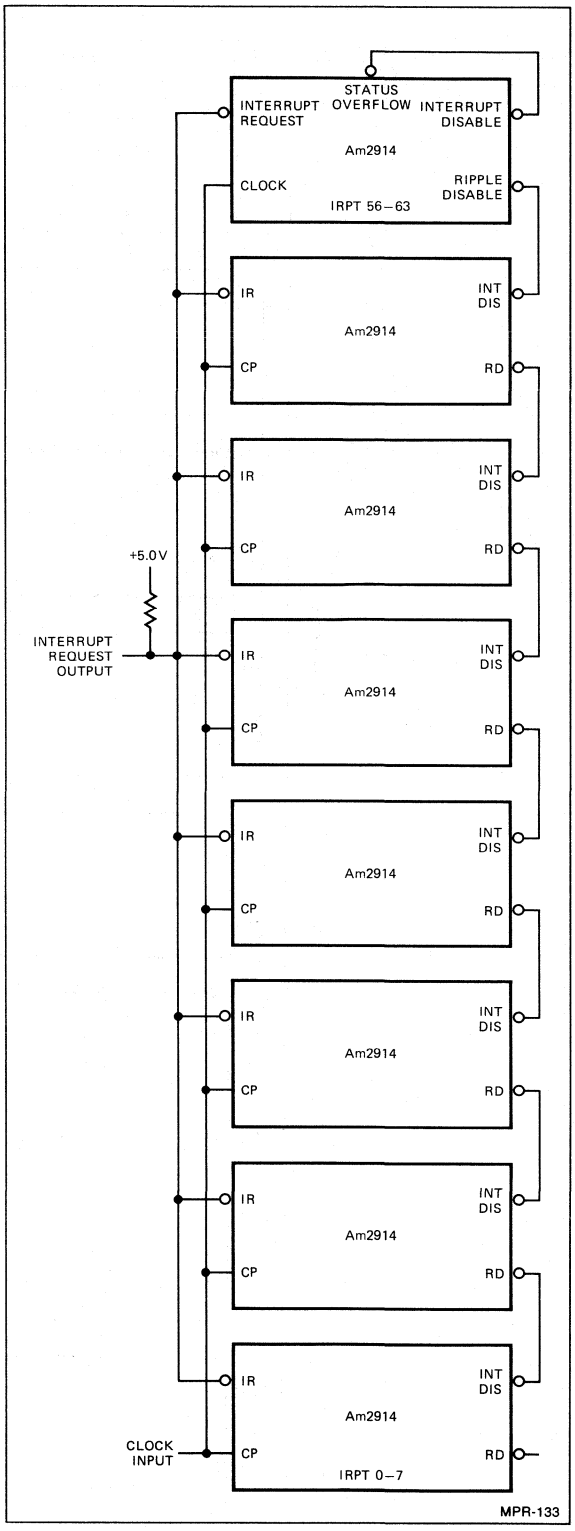


Figure 6. Interrupt Disable Connections for Ripple Cascade Mode.

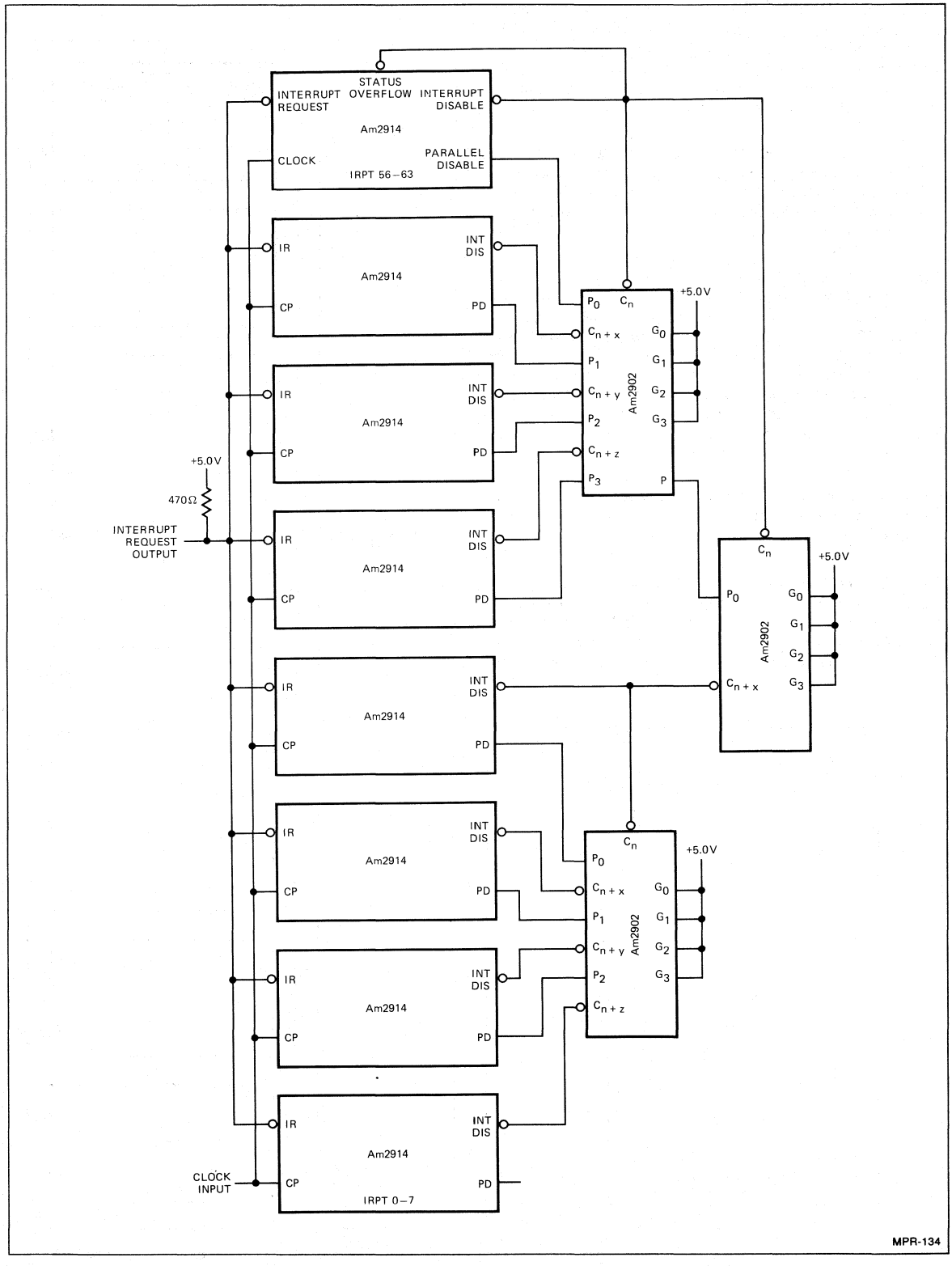


Figure 7. Interrupt Disable Connections for Parallel Cascade Mode.

Ripple Disable output is tied to the Interrupt Disable input of the next lower priority group (see Figure 6).

Parallel Disable (PD) – This output is used only in the parallel cascade mode (see below). It is HIGH when the Lowest Group Enabled flip-flop is LOW or an Interrupt Request is generated in the group. It is not affected by the Interrupt Disable input.

A single Am2914 chip may be used to prioritize and encode up to eight interrupt inputs. Figure 5 shows how the above cascade lines should be connected in such a single chip system.

The Group Advance Receive and Group Enable inputs should be connected to ground so that the Lowest Group Enabled flip-flop is forced LOW during a *Master Clear* or *Load Status* microinstruction. Status Overflow should be connected to Interrupt Disable in order to disable interrupts when vector seven is read. The Group Advance Send, Ripple Disable, Group Signal and Parallel Disable pins should be left open.

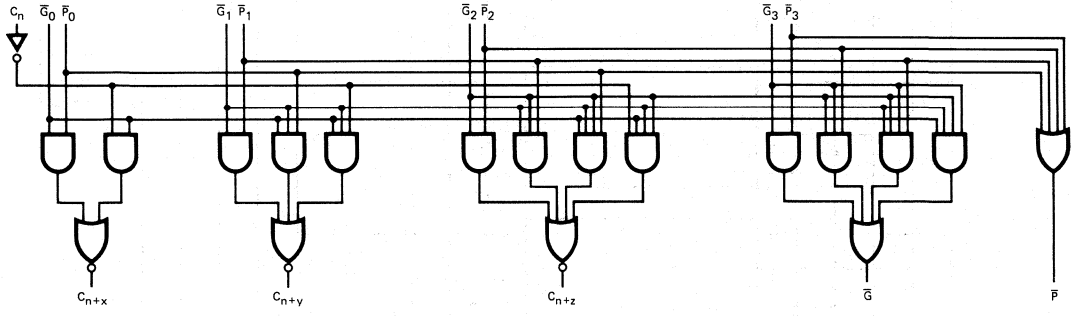
The Am2914 may be cascaded in either a Ripple Cascade Mode or a Parallel Cascade Mode. In the Ripple Cascade Mode, the Interrupt Disable signal, which disables lower priority interrupts, is allowed to ripple through lower priority groups. Figures 6, 9 and 11 show the cascade connections required for a ripple cascade 64 input interrupt system.

In the parallel cascade mode, a parallel lookahead scheme is employed using the high-speed Am2902 Lookahead Carry Generator. Figures 7, 9 and 10 show the cascade connections required for a parallel cascade 64-input interrupt system. For this application, the Am2902 is used as a lookahead interrupt disable generator. A Parallel Disable output from any group results in the disabling of all lower priority groups in parallel. Figure 8 shows the Am2902 logic diagram and equations.

In Figures 9 and 10, the Am2913 Priority Interrupt Expander is shown forming the high order bits of the vector and status, respectively. The Am2913 is an eight-line to three-line priority encoder with three-state outputs which are enabled by the five output control signals G1, G2, $\overline{G3}$, $\overline{G4}$, and $\overline{G5}$. In Figure 9, the Am2913 is connected so that its outputs are enabled during a Read Vector instruction, and in Figure 10 the Am2913 is connected so that its outputs are enabled during a Read Status instruction. The Am2913 logic diagram and truth table are shown in Figure 11.

The Am25LS138 three-line to eight-line Decoder also is shown in Figure 10. It is used to decode the three high order status bits during a Load Status instruction. The Am25LS138 logic diagram and truth table are shown in Figure 12.

6



$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

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Figure 8. Am2902 Carry Look-Ahead Generator Logic Diagram and Equations.

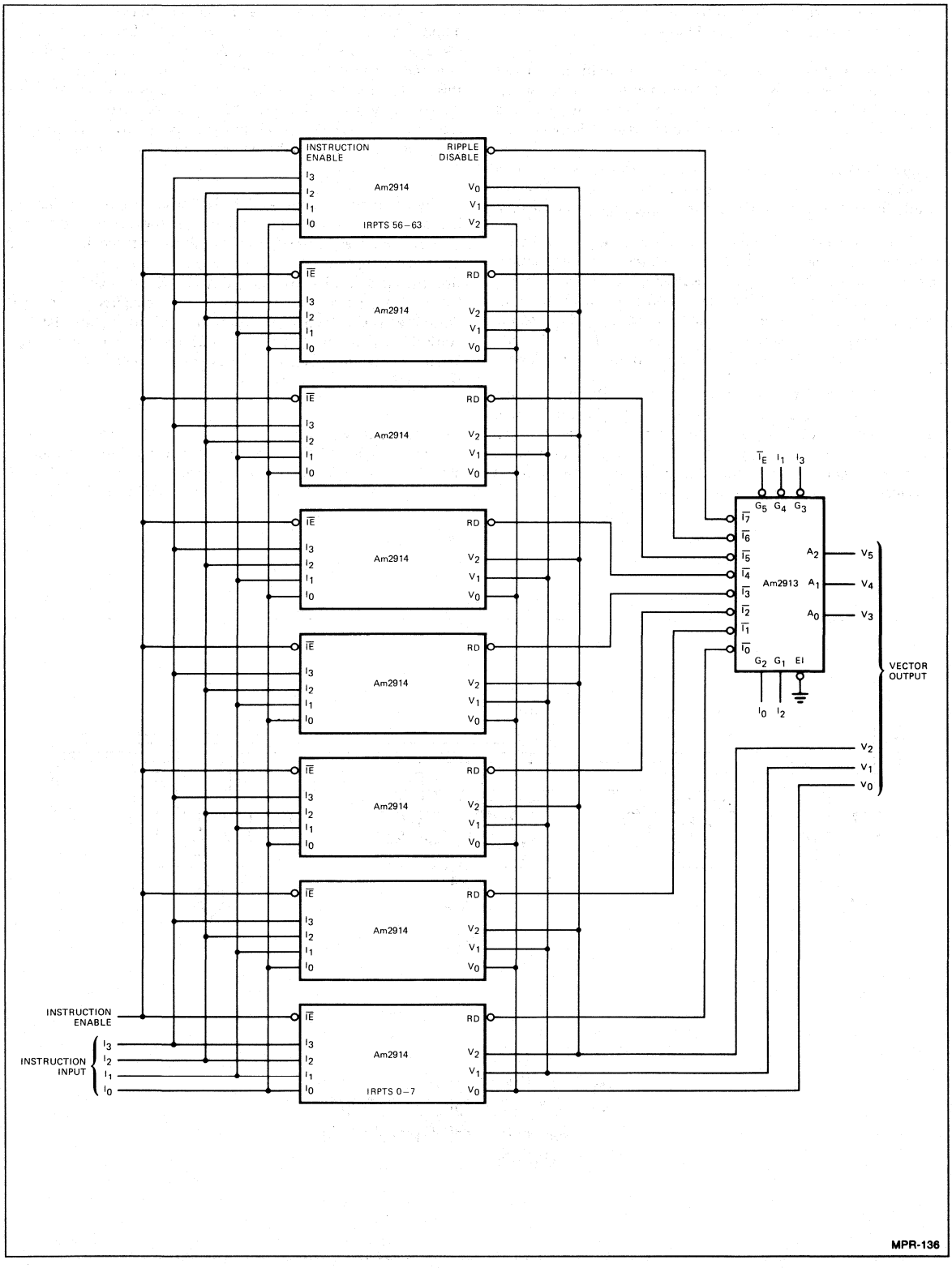


Figure 9. Vector Connections for both the Parallel and Ripple Cascade Modes.

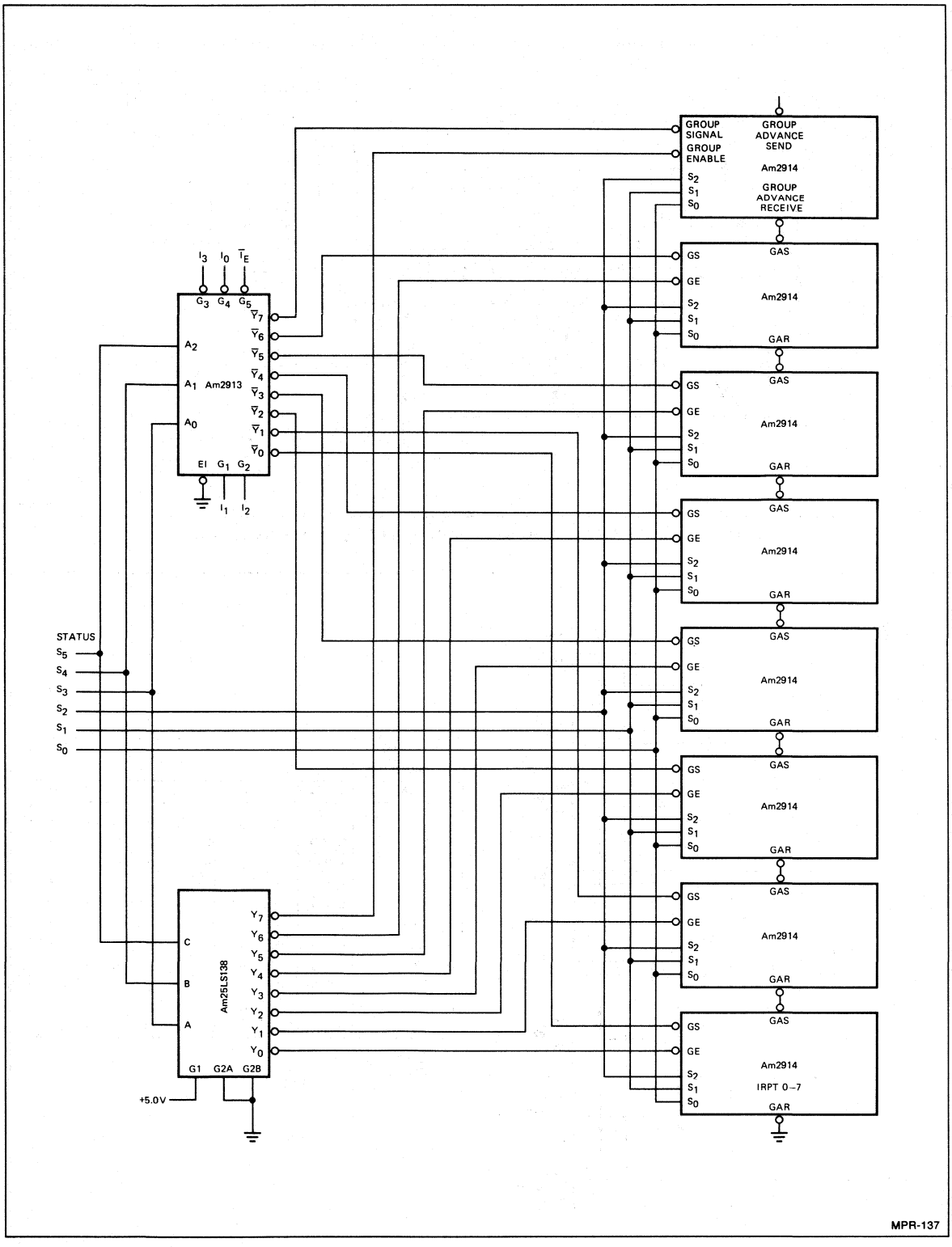
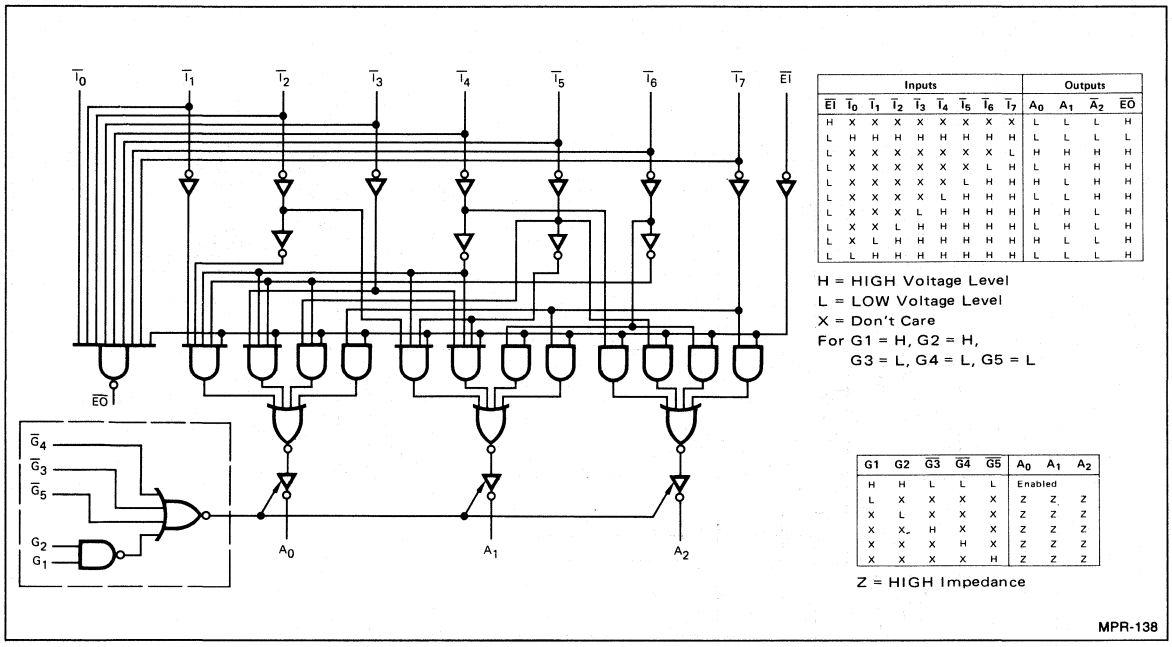


Figure 10. Group Signal, Group Enable, Group Advance Send, Group Advance Receive and Status Connections for Both the Parallel and Ripple Cascade Modes.



Inputs								Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G1 = H, G2 = H,
G3 = L, G4 = L, G5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

Z = HIGH Impedance

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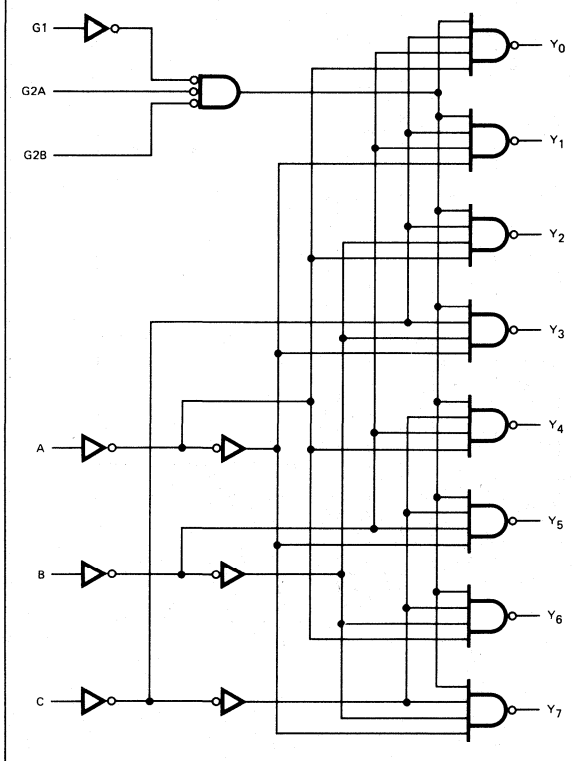
Figure 11. Am2913 Priority Interrupt Expander Logic Diagram and Truth Table.



Inputs						Outputs							
Enable			Select										
G1	G2A	G2B	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't Care

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Figure 12. Am25LS138 3 to 8 Line Decoder Logic Diagram and Truth Table.

EXAMPLE INTERRUPT SYSTEMS DESIGNS FOR AN Am2900 SYSTEM

A classical computer architecture is shown in Figure 13. The Computer Control Unit controls the internal busses and subsystems of the processor, synchronizes internal and external events and grants or denies permission to external systems. The data bus is commonly used by all of the subsystems in the computer. Information, instructions, address operands, data and sometimes control signals are transmitted down the data bus under control of a microprogram. The microprogram selects the source of the data as well as the destination(s) of the data. The Address Bus is typically used to select a word in memory for an internal computer function or to select an input/output port for an external subsystem or peripheral function. The source of the data for the address bus, also selected by microprogram commands, may be the program counter, the memory address register, a direct memory address controller, an interface controller, etc.

The arithmetic/logic unit (ALU) is that portion of the processor that computes. Under control of the microprogram, the ALU performs a number of different arithmetic and logic functions on data in the working registers or from the data bus. The ALU also provides a set of condition codes as a result of the current arithmetic or logic operation. The condition codes, along with other computer status information, are stored in a register for later use by the programmer or computer control unit.

The program counter and the memory address register are the two main sources of memory word and I/O address select data on the address bus. The program counter contains the address of the next instruction or instruction operand that is to be fetched from main memory, and the memory address register contains instruction address operands which are necessary to fetch the data required for the execution of the current instruction.

A subroutine address stack is provided to allow the return address linkage to be handled easily when exiting a subroutine. The address stack is a last-in, first-out stack that is controlled by a jump-to-subroutine, PUSH, or a return-from-subroutine, POP, instruction from the CCU microinstruction word.

The next microprogram address control (NMAC) circuitry controls the generation of microinstruction addresses. Based on microprogram control, interrupt requests, test conditions and commands from a control panel or other processor, the NMAC determines the address of the next microinstruction to be executed.

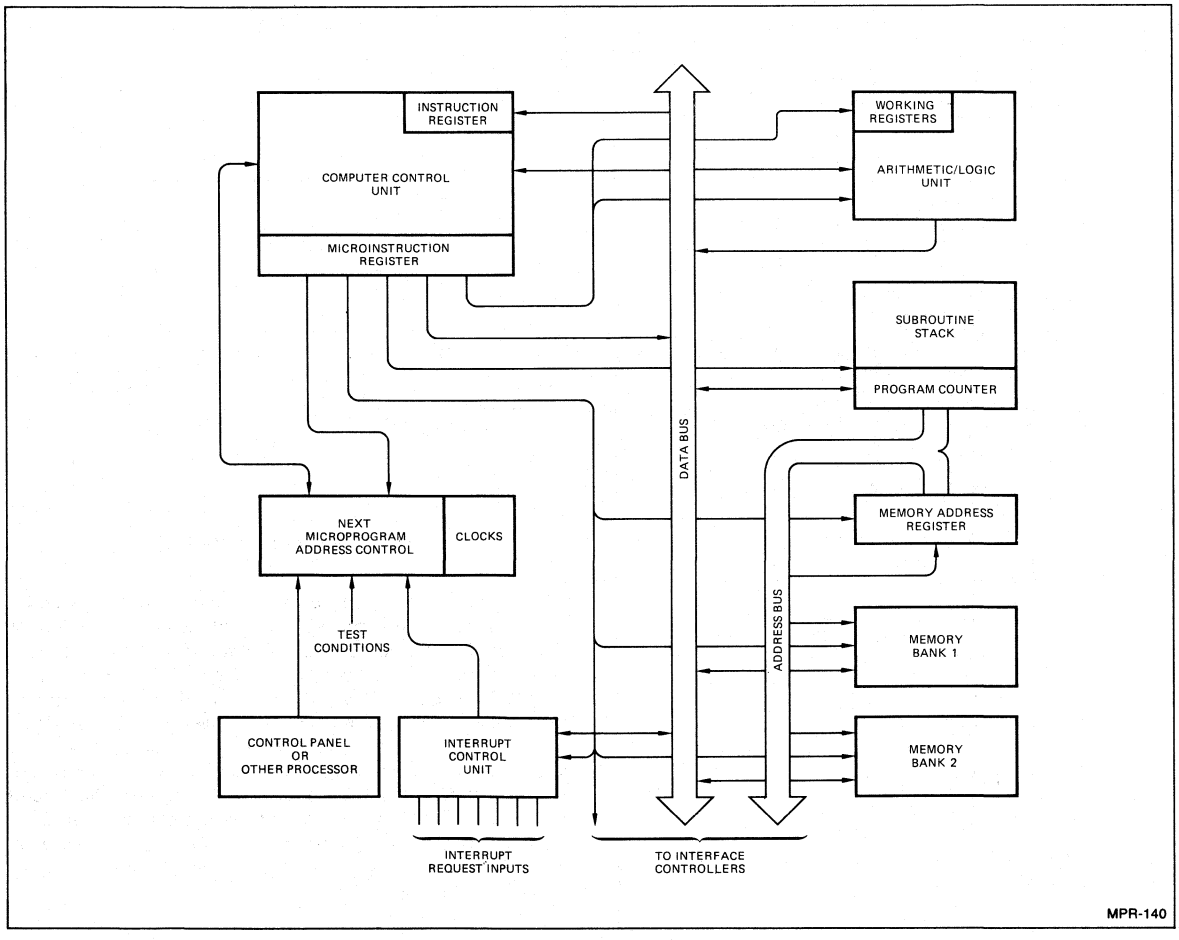


Figure 13. Generalized Computer Architecture.

Am2914 PRIORITY INTERRUPT ENCODER DETAILED LOGIC DESCRIPTION

INTRODUCTION

A clear understanding of the Am2914 Priority Interrupt controller's operation facilitates its efficient use. With that idea in mind, a detailed logic description of the Am2914 is presented here. A detailed logic diagram and control signal truth table are shown, and significant aspects of the Am2914 design are described verbally.

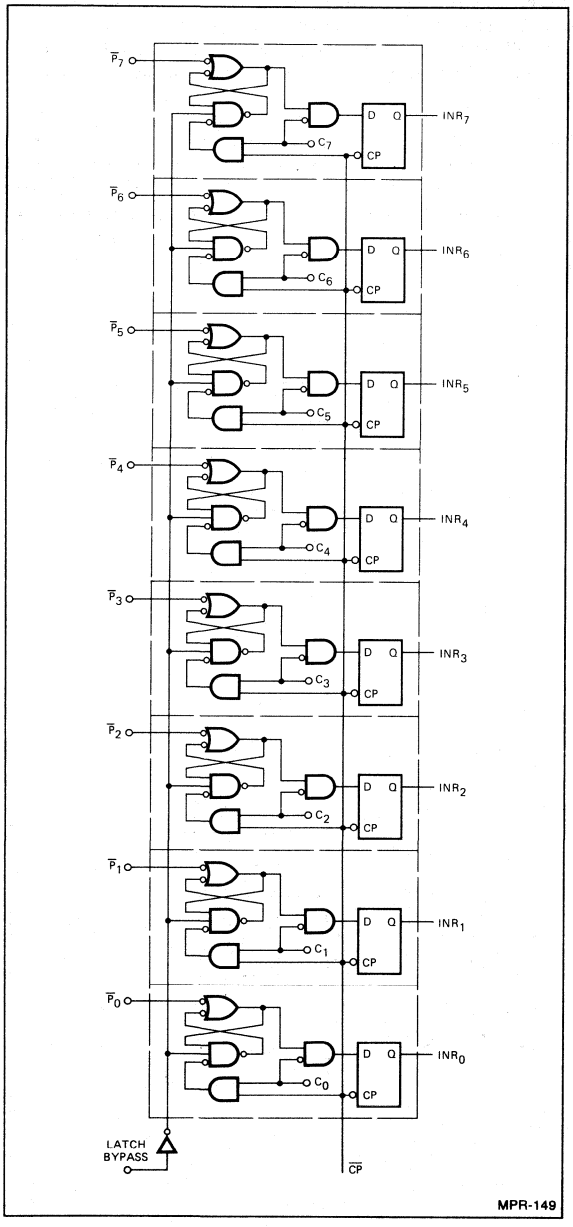


Figure 1. Interrupt Latches and Register.

LOGIC DIAGRAM DESCRIPTION

The Interrupt Latches and Register are shown in Figure 1. The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent. The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register. It is updated on the LOW-to-HIGH transition of the clock pulse (HIGH-to-LOW transition of the $\overline{CP}$ signal) as are all of the flip-flops on the chip.

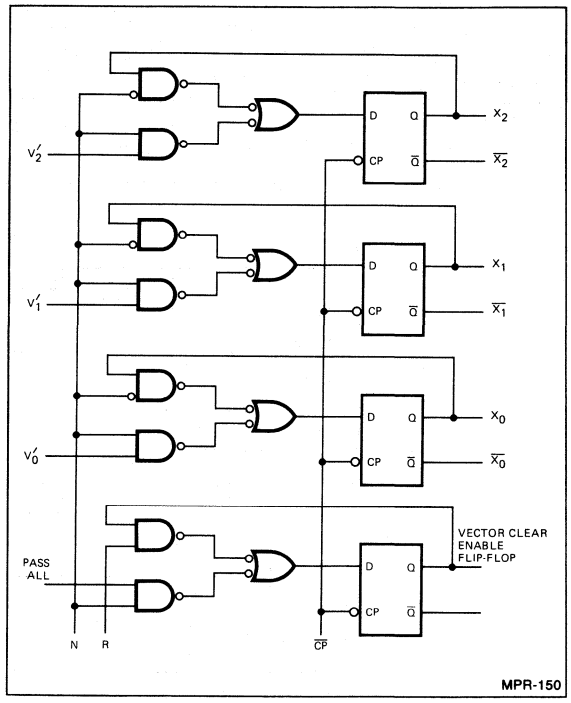


Figure 2. Vector Hold Register

When a Read Vector instruction is executed, the binary coded vector is loaded into the Vector Hold Register of Figure 2. This stored vector can be used later for clearing the interrupt associated with the last vector that was read. The Vector Clear Enable Flip-Flop of Figure 2 is set when a Read Vector instruction is executed and the PASS ALL signal is HIGH. A HIGH PASS ALL signal level indicates that this group is enabled and that an interrupt request in this group was detected and passed priority. The Vector Hold Register and the Vector Clear Enable Flip-Flop are cleared when a Master Clear, Clear All Interrupts, or Clear Interrupt Last Vector Read is executed. Table 1 shows the generation of the "N and R" control signals for each of these operations.

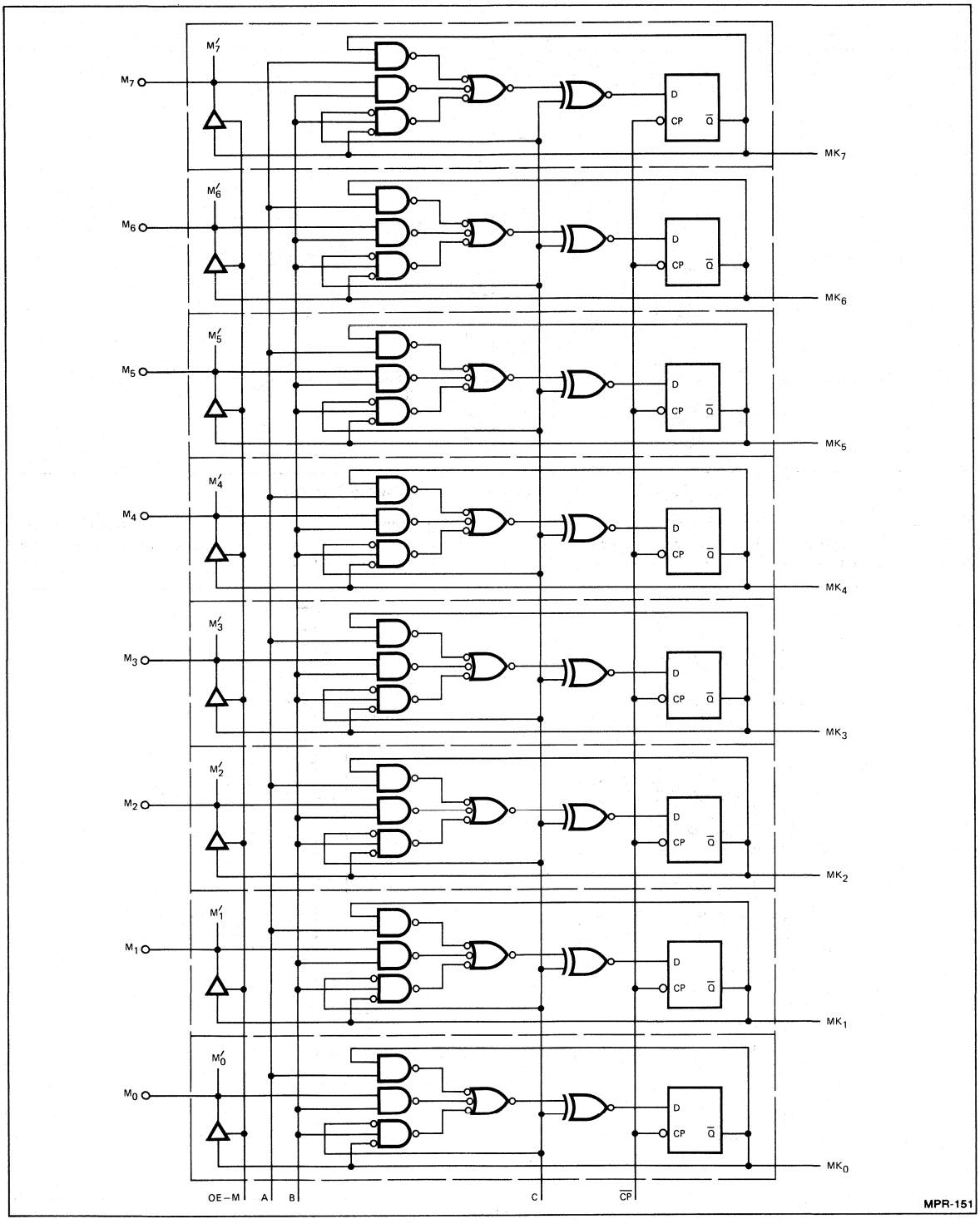


Figure 3. Mask Register.

The Mask Register shown in Figure 3 holds the eight mask bits associated with the eight interrupt levels. The register may be set or cleared, bit set or bit cleared from the "M" bus, or loaded or read to the "M" bus. Table 1 shows the generation of the "A", "B", "C" and "OE-M" control signals for each of these operations.

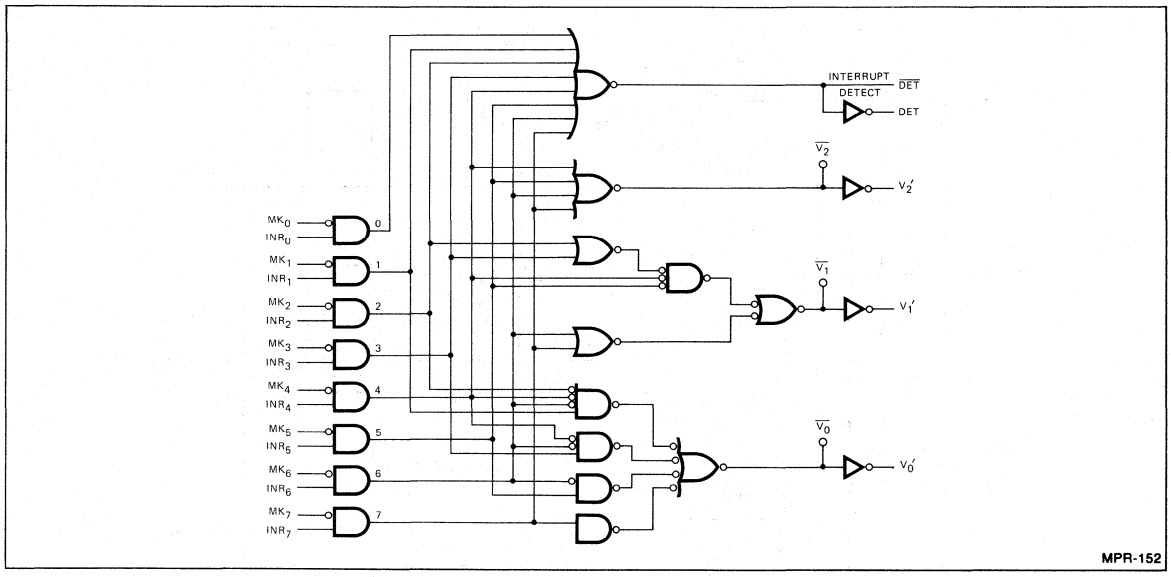


Figure 4. Interrupt Request Detect and Priority Decoder.

The Interrupt Request Detect and Priority Encode circuitry are shown in Figure 4. The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector, V_0-V_2.

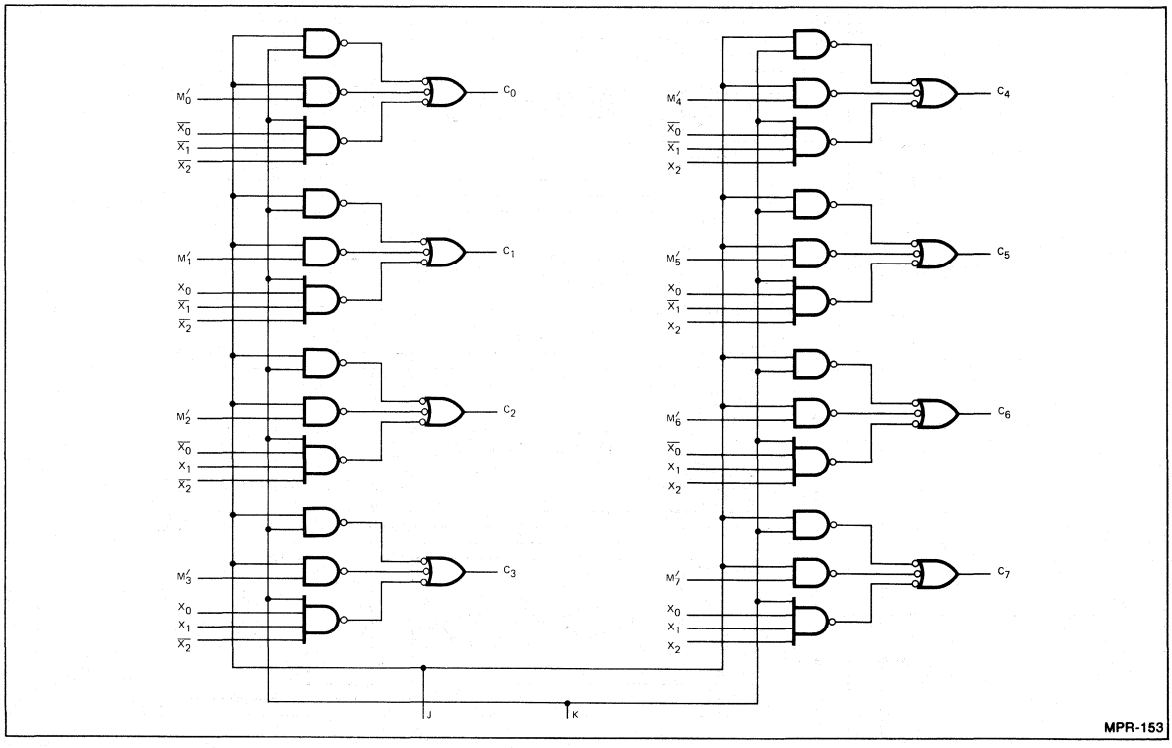


Figure 5. Clear Control.

The Clear Control logic of Figure 5 generates the eight individual clear signals for the eight Interrupt Register bits. Under microinstruction control, all interrupts, interrupts with corresponding mask register bits set, interrupts with corresponding mask bus bits equal to one, or the interrupt associated with the last vector read may be cleared. Table 1 shows the generation of the "J" and "K" control signals for each of these operations.

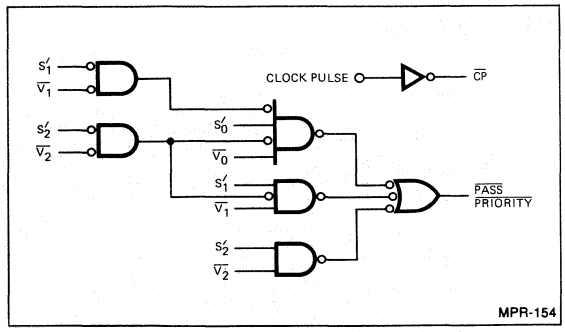


Figure 6. Three-Bit comparator.

The three-bit Comparator of Figure 6 compares the interrupt vector with the contents of the Status Register. A LOW signal level at the PASS PRIORITY output indicates that the interrupt vector is greater than or equal to the contents of the Status Register.

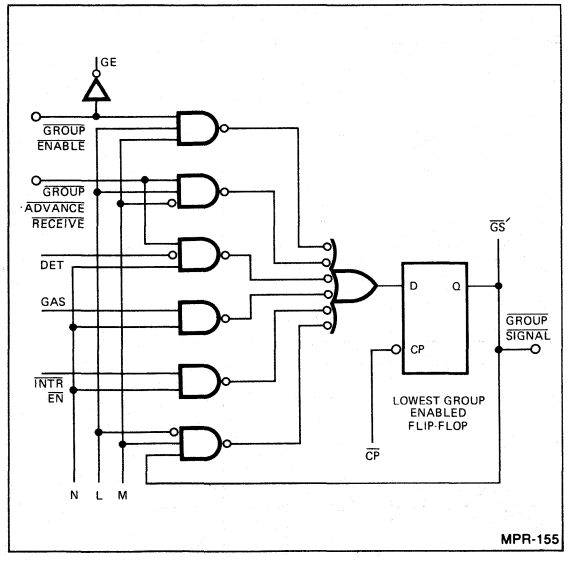


Figure 7. Group Enable Logic.

The Lowest Group Enabled Flip-Flop, Figure 7, is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the group which contains the lowest priority interrupt which will be accepted and is used to form the high order status bits. When a Load Status instruction is executed, the flip-flop is loaded from the GROUP ENABLE input. When a Master Clear instruction is executed, it is loaded from the GROUP ADVANCE RECEIVE input. The flip-flop is set HIGH when a Read Vector instruction is executed if a Group Advance is not received and no interrupt in this group is detected, if a Group Advance is sent from this group, or if interrupts from this group are disabled. For all other instructions, the flip-flop remains the same. Table 1 shows the generation of the "N", "L" and "M" control signals for these operations.

The Status Register holds the status bits and may be loaded from or read to the "S" bus as shown in Figure 8. Note that when a Load Status instruction is executed, status from the "S" bus is loaded into the Status Register only if the GROUP ENABLE input is LOW; if the GROUP ENABLE input is HIGH, the Status Register is cleared. Also note that during a Read Status instruction, the Status Register outputs are enabled onto the "S" bus only if the Lowest Group Enabled Flip-Flop of this group is LOW. When a Read Vector instruction is executed, the incrementer increases the vector by one and the result is loaded into the Status Register. Thus, the Status Register always points to the lowest level at which an interrupt will be accepted. Table 1 shows the generation of the "F", "G" and "OE-S" control signals for Status Register operations.

The Interrupt Request Logic, shown in Figure 9, generates the RIPPLE DISABLE, PARALLEL DISABLE, INTERRUPT REQUEST, GROUP ADVANCE SEND, and STATUS OVERFLOW output signals. The PARALLEL DISABLE signal is generated when the Lowest Group Enabled signal is LOW or an interrupt request in this group is detected and passes priority. The RIPPLE DISABLE signal is generated when the PARALLEL DISABLE signal is generated and also when the INTERRUPT DISABLE input signal is LOW. The INTERRUPT REQUEST output signal is generated when interrupt requests in this group are enabled and a request is detected and passes priority. The GROUP ADVANCE SEND output signal is generated when a vector of value seven is being read. The Status Overflow Flip-Flop is set LOW when a vector of value seven is read and indicates the Status Register has overflowed. The Interrupt Request Enable Flip-Flop is either set or reset by the Enable Request or Disable Request microinstructions respectively, and is used to enable or disable the INTERRUPT REQUEST output. Table 1 shows the generation of control signals "D", "E", "S" and "H".

Note that the vector outputs are enabled only when a Read Vector is being executed. Also note that when a Read Vector instruction is executed, the vector outputs will be disabled after the execution of the instruction since the Status Register is loaded with V+1, and the INTERRUPT REQUEST will no longer be generated.

The Microinstruction Decode circuitry, Figure 10, decodes the Am2914 microinstructions and generates the required internal control signals. Table 1 shows the truth table for these functions and Figure 11 shows the function tables.

Table 1. Am2914 Control Signal Truth Table.

0 = LOW, 1 = HIGH

Microinstruction						Function	Mask Register				Status Register			Group Enable		Clear Control		Irpt Request Enable		Vector Hold Register		Other	
Decimal	$\overline{I_E}$	I_3	I_2	I_1	I_0	Description	A	B	C	OE-M	F	G	$\overline{OE\text{-}S}$	L	M	J	K	D	E	N	R	S	H
0	0	0	0	0	0	Master Clear	0	0	1	0	0	0	1	1	0	1	1	0	1	0	0	1	1
1	0	0	0	0	1	Clear All Interrupts	1	0	1	0	0	1	1	0	1	1	1	1	X	0	0	1	0
2	0	0	0	1	0	Clear Intr Via M Bus	1	0	1	0	0	1	1	0	1	1	0	1	X	0	1	1	0
3	0	0	0	1	1	Clear Intr Via M Reg	1	0	1	1	0	1	1	0	1	1	0	1	X	0	1	1	0
4	0	0	1	0	0	Clear Intr, Last Vector	1	0	1	0	0	1	1	0	1	0	1/0	1	X	0	0	1	0
5	0	0	1	0	1	Read Vector	1	0	1	0	0/1	0	1	0	0	0	0	1	X	1	0	0	1
6	0	0	1	1	0	Read Status Reg	1	0	1	0	0	1	0	0	1	0	0	1	X	0	1	1	0
7	0	0	1	1	1	Read Mask Reg	1	0	1	1	0	1	1	0	1	0	0	1	X	0	1	1	0
8	0	1	0	0	0	Set Mask Reg	0	0	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
9	0	1	0	0	1	Load Status Reg	1	0	1	0	1	1	1	1	1	0	0	1	X	0	1	1	1
10	0	1	0	1	0	Bit Clear Mask Reg	0	1	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
11	0	1	0	1	1	Bit Set Mask Reg	1	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
12	0	1	1	0	0	Clear Mask Reg	0	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
13	0	1	1	0	1	Disable Request	1	0	1	0	0	1	1	0	1	0	0	0	0	0	1	1	0
14	0	1	1	1	0	Load Mask Reg	0	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
15	0	1	1	1	1	Enable Request	1	0	1	0	0	1	1	0	1	0	0	0	1	0	1	1	0
X	1	X	X	X	X	Instruction Disable	1	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0

Notes: 1. Control line "F" during "READ VECTOR" instruction is 0 when "PASS ALL" is LOW and 1 when "PASS ALL" is HIGH.
2. Control line "K" during "Clear Intr, Last Vector" instruction is 0 when "Vector Clear Enable" is LOW and 1 when "Vector Clear Enable" is HIGH.

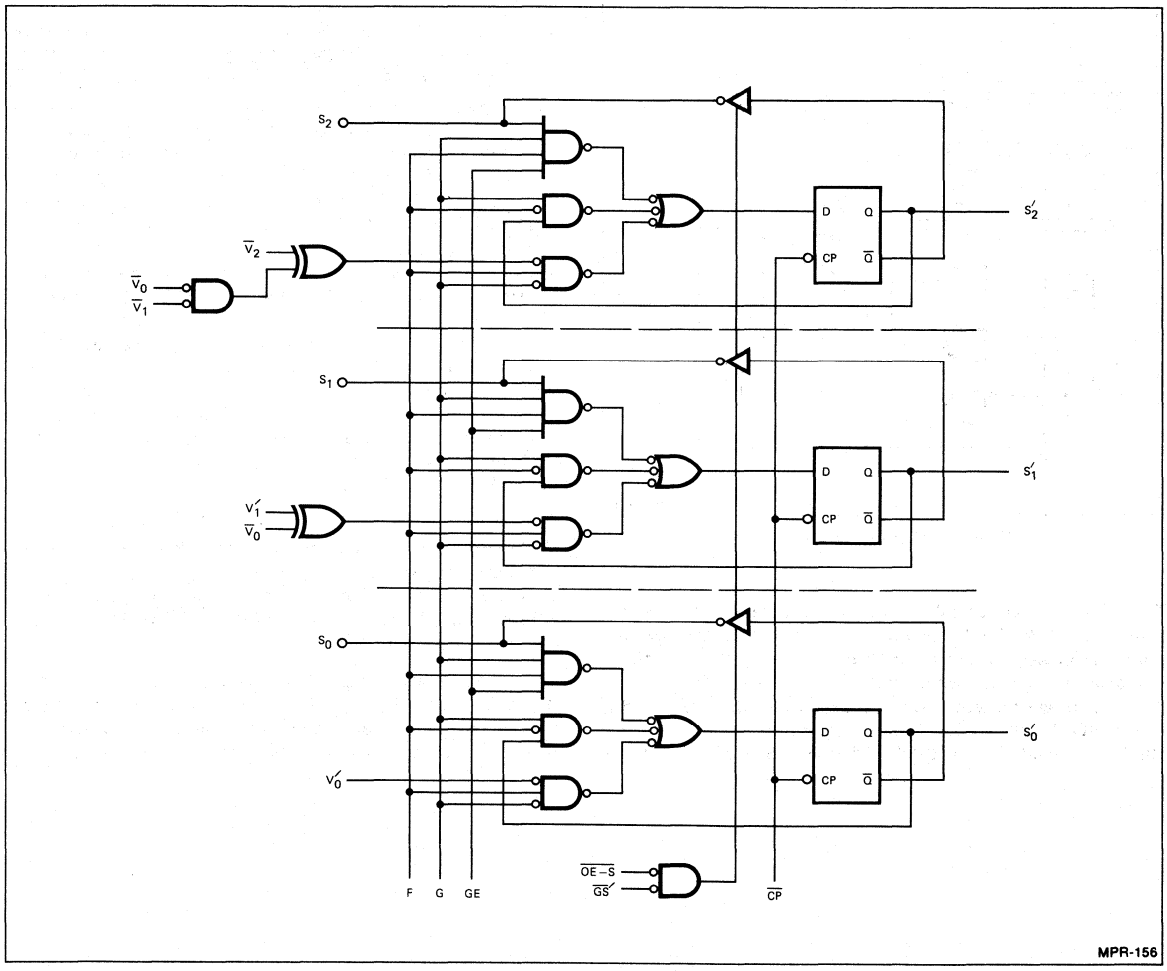


Figure 8. Incrementer and Status Register.

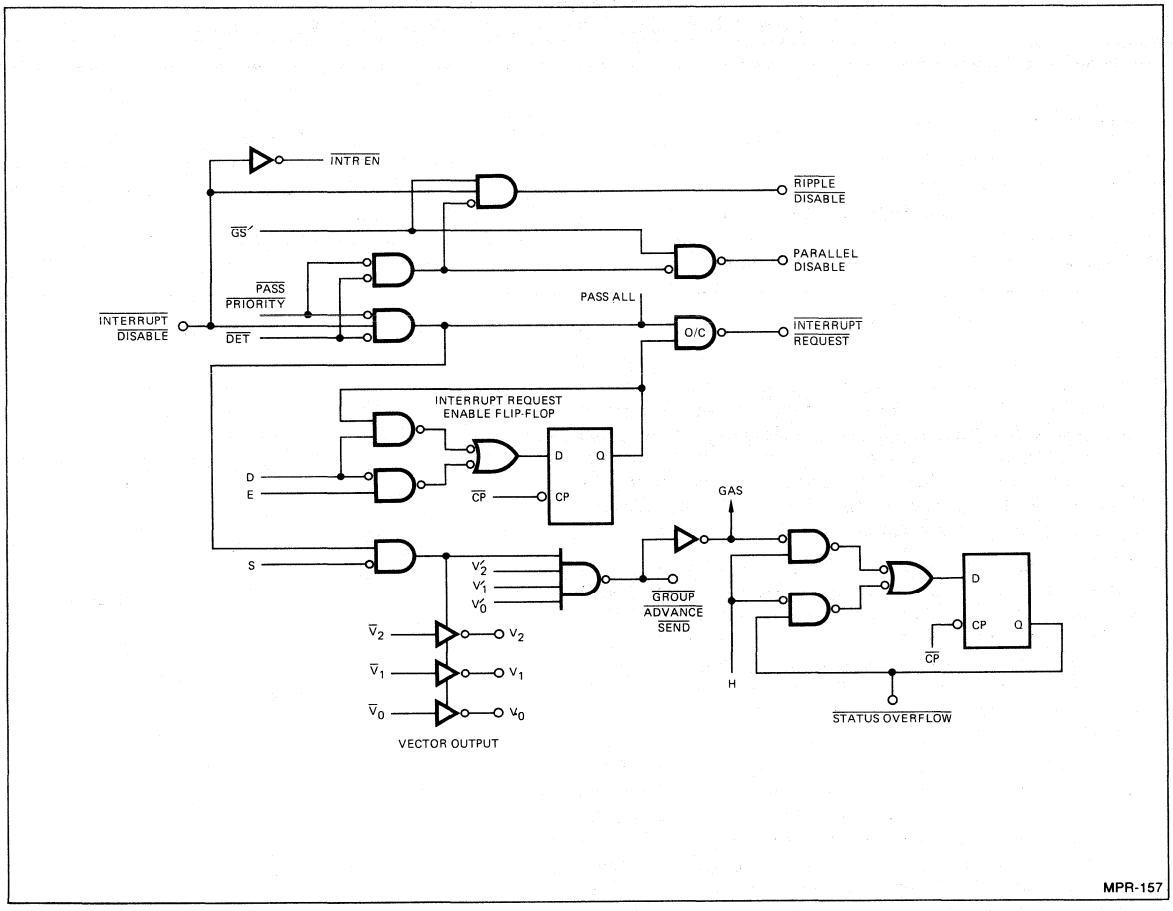


Figure 9. Interrupt Request Logic.

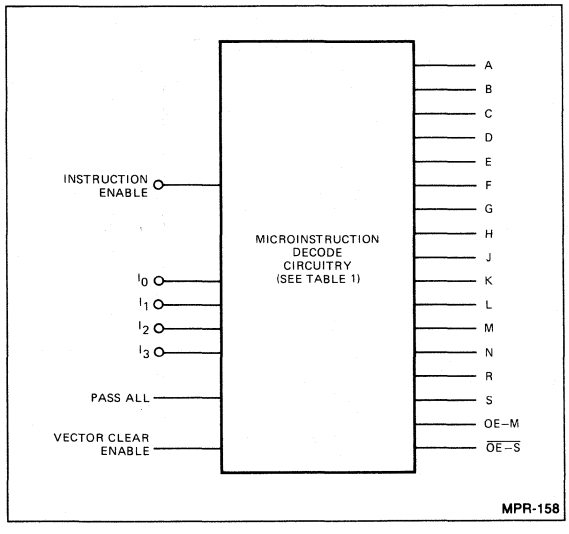


Figure 10.

MASK REGISTER

A	B	C	FUNCTION
0	0	0	SET
0	0	1	CLEAR
0	1	0	BIT CLEAR
0	1	1	LOAD
1	0	1	HOLD
1	1	1	BIT SET

CLEAR CONTROL

J	K	FUNCTION
0	0	NO CLEAR
0	1	CLEAR IRPT, VECTOR
1	0	CLEAR IRPTS VIA M
1	1	CLEAR ALL IRPTS

VECTOR HOLD REGISTER

N	FUNCTION
0	HOLD
1	LOAD

LOWEST GROUP ENABLED FLIP-FLOP

L	M	FUNCTION
0	0	UPDATE
0	1	HOLD
1	0	LOAD VIA GROUP ADVANCE RECEIVE
1	1	LOAD VIA GROUP ENABLE

STATUS REGISTER

F	G	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD VECTOR + 1
1	1	LOAD VIA "S" BUS

INTERRUPT REQUEST ENABLE FLIP-FLOP

D	E	FUNCTION
0	0	DISABLE IRPTS
0	1	ENABLE IRPTS
1	X	HOLD

VECTOR CLEAR ENABLE FLIP-FLOP

N	R	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD

STATUS OVERFLOW FLIP-FLOP

H	FUNCTION
0	HOLD
1	LOAD

Figure 11. Control Function Tables.

Am2915A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

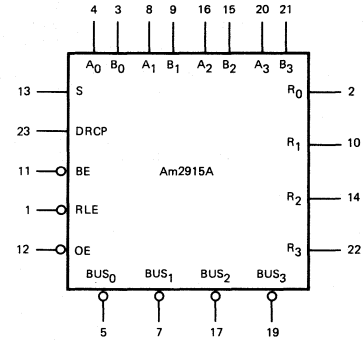
The Am2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input (BE) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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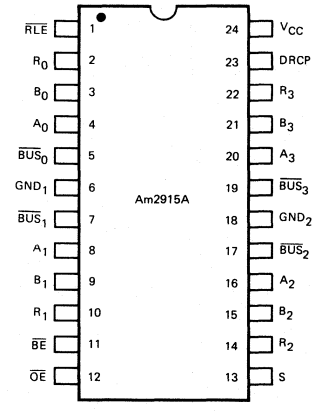
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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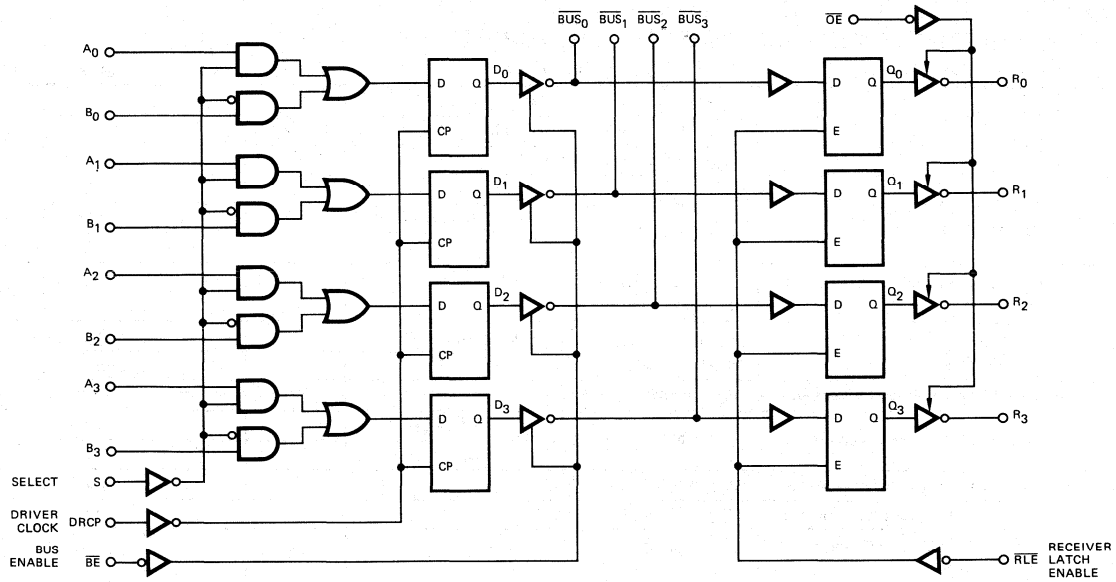
LOGIC DIAGRAM



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6

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2915AXM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2915AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

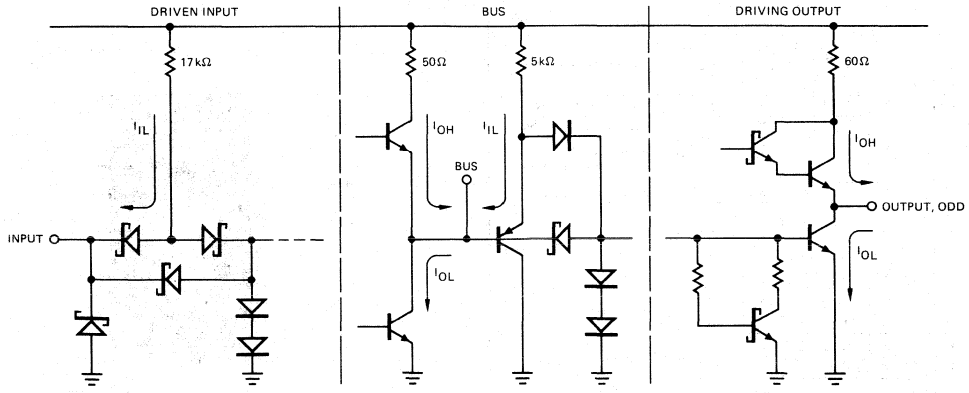
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		$V_{CC} = 5.0$V, $I_{OH} = -100\mu$A		3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0$mA		0.27	0.4	Volts
			$I_{OL} = 8.0$mA		0.32	0.45	
			$I_{OL} = 12$mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0$V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4$V			50	μA
			$V_O = 0.4$V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2915AXM Min.	Am2915AXM Typ. (Note 2)	Am2915AXM Max.	Am2915AXC Min.	Am2915AXC Typ. (Note 2)	Am2915AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)	$C_L = 15$pF, $R_L = 2.0$kΩ	15			12			ns
t_h			8.0			6.0			
t_s	Select Input (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output	$C_L = 5$pF, $R_L = 2.0$kΩ		14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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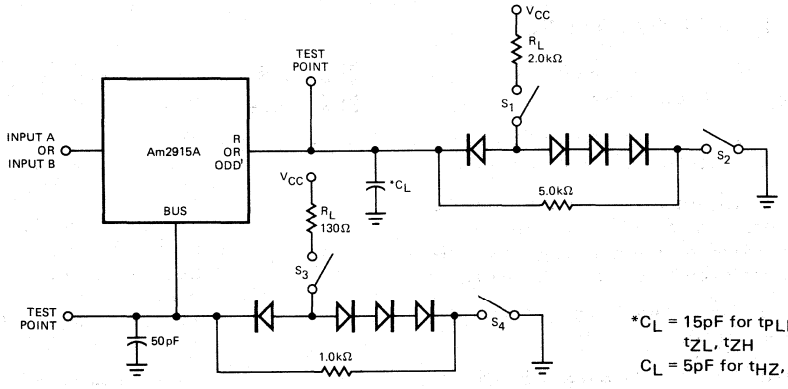
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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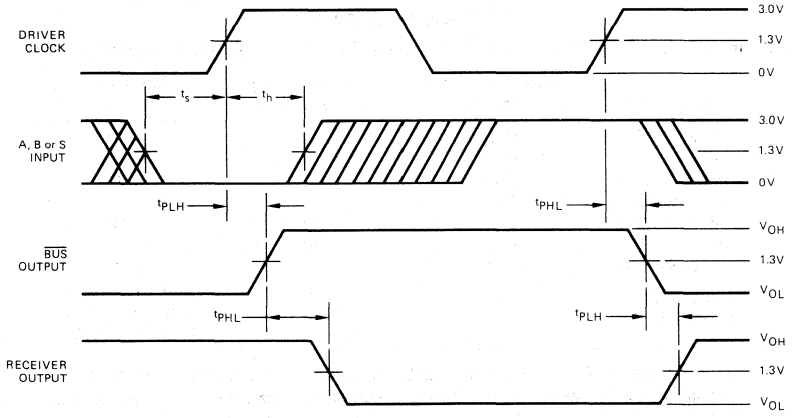
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

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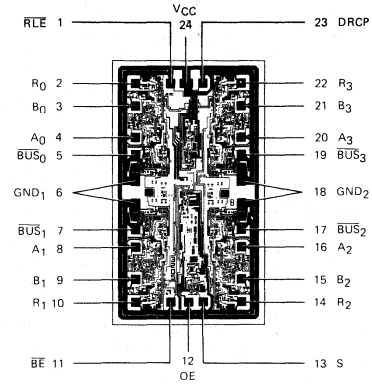
FUNCTIONAL TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

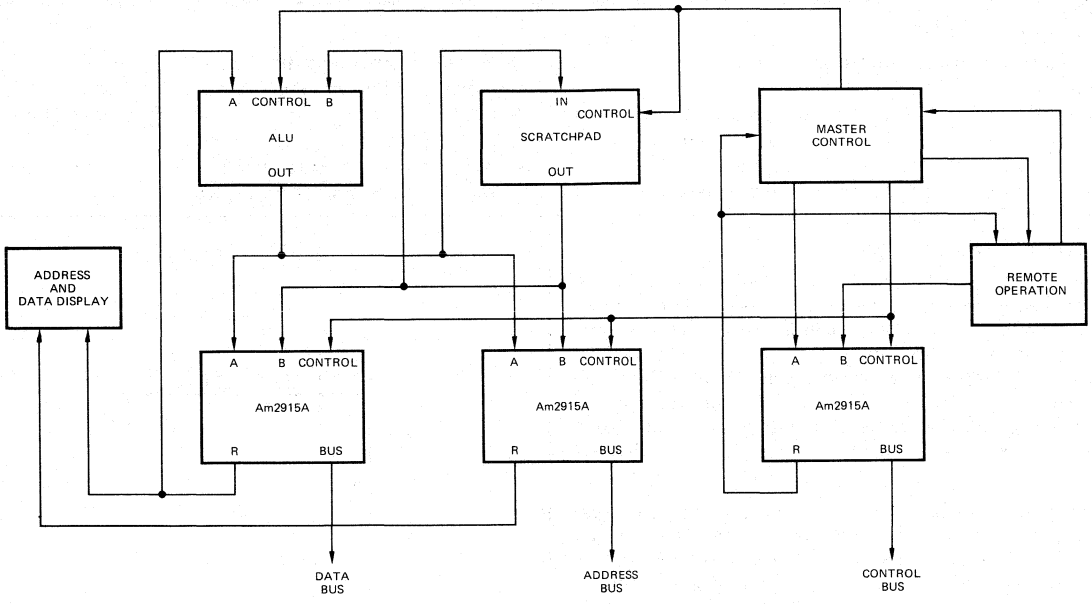
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2915APC	P-24	C	C-1
AM2915ADC	D-24	C	C-1
AM2915ADC-B	D-24	C	B-1
AM2915ADM	D-24	M	C-3
AM2915ADM-B	D-24	M	B-3
AM2915AFM	F-24-1	M	C-3
AM2915AFM-B	F-24-1	M	B-3
AM2915AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2915AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



The Am2915A is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

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6

Am2916A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

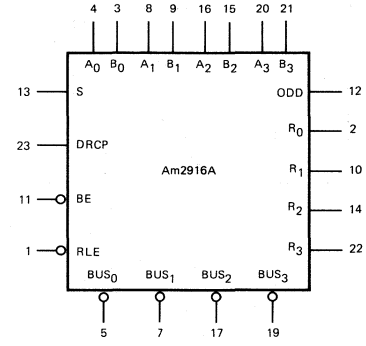
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data in non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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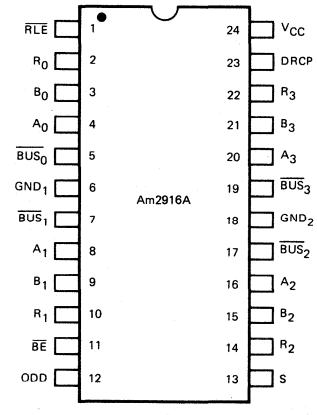
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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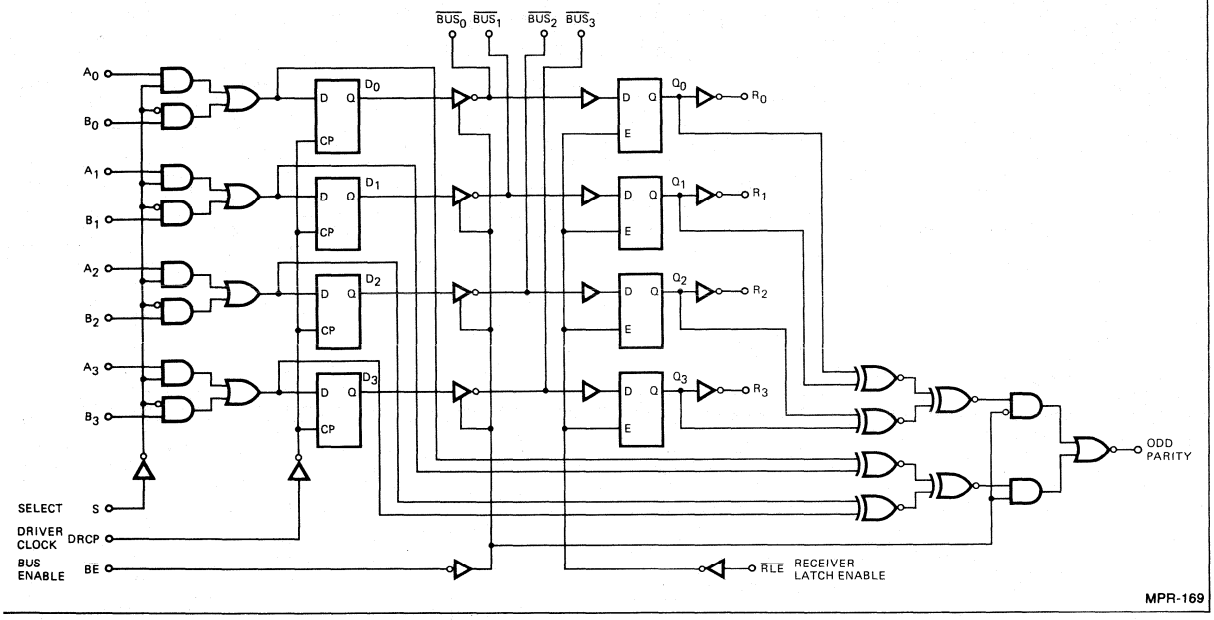
LOGIC DIAGRAM



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6

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2916AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2916AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

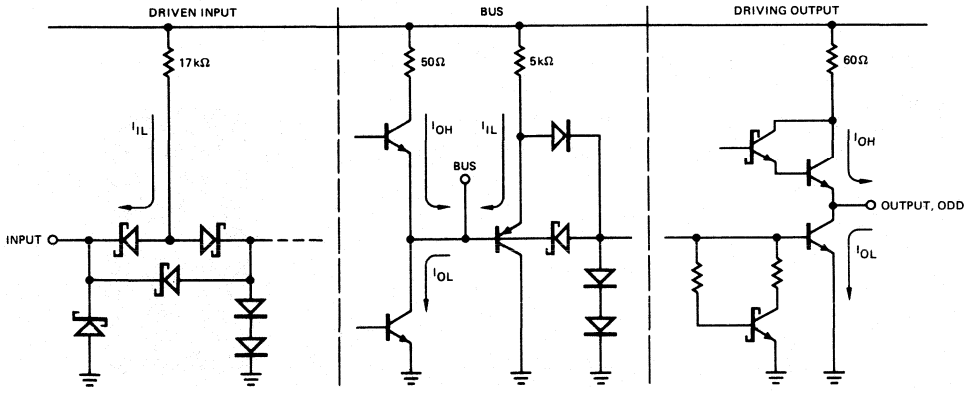
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		$V_{CC} = 5.0$V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0$mA		0.27	0.4	Volts
			$I_{OL} = 8.0$mA		0.32	0.45	
			$I_{OL} = 12$mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0$V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2916AXM Min.	Am2916AXM Typ. (Note 2)	Am2916AXM Max.	Am2916AXC Min.	Am2916AXC Typ. (Note 2)	Am2916AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF R_L(BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)	$C_L = 15$pF $R_L = 2.0$kΩ	15			12			ns
t_h			8.0			6.0			
t_s	Select Inputs (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoul not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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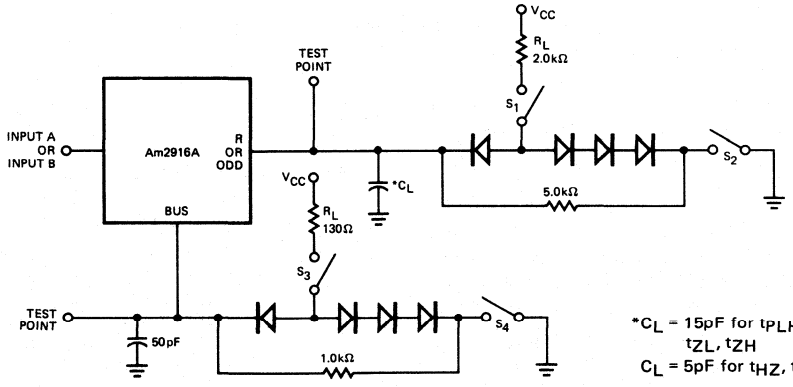
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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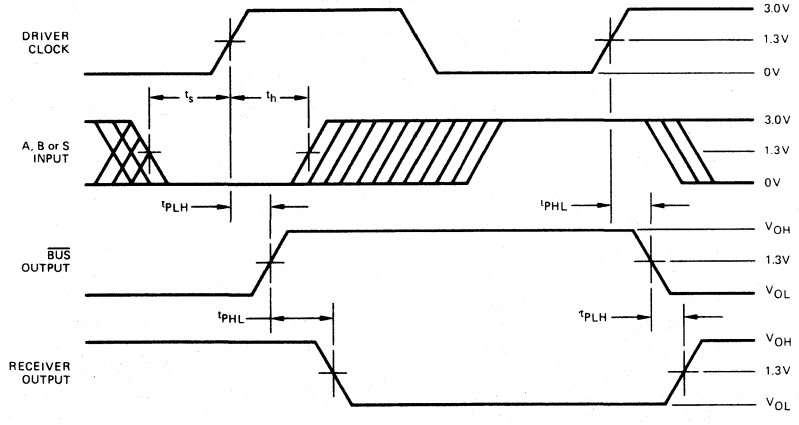
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

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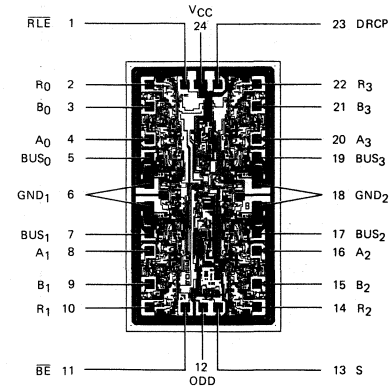
FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 — The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 — The "B" word data input into the two input multiplexers of the driver register.

S — Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP — Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ — Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ — The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 — The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ — Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ — Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

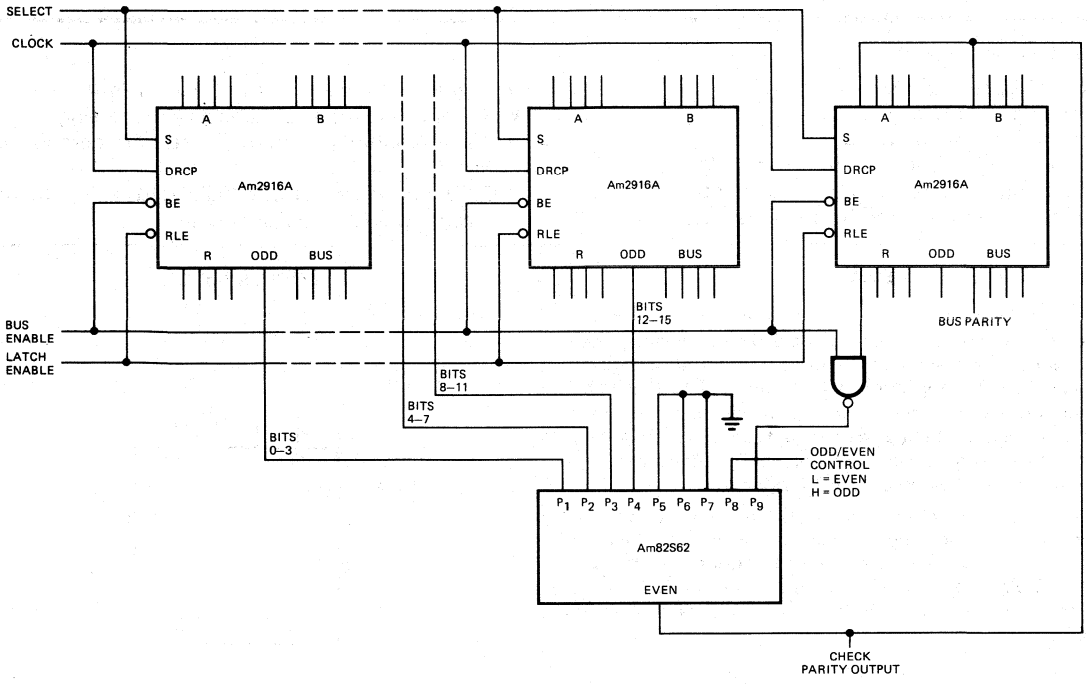
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2916APC	P-24	C	C-1
AM2916ADC	D-24	C	C-1
AM2916ADC-B	D-24	C	B-1
AM2916ADM	D-24	M	C-3
AM2916ADM-B	D-24	M	B-3
AM2916AFM	F-24-1	M	C-3
AM2916AFM-B	F-24-1	M	B-3
AM2916AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2916AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



Generating or checking parity for 16 data bits.

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6

Am2917A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

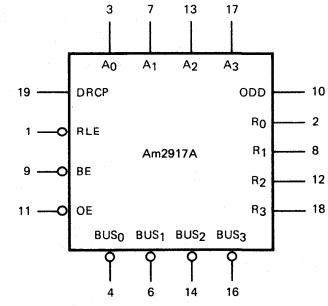
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

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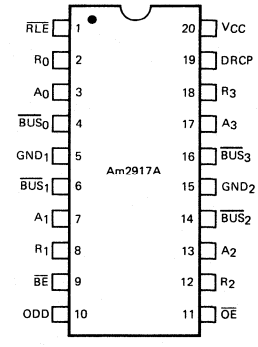
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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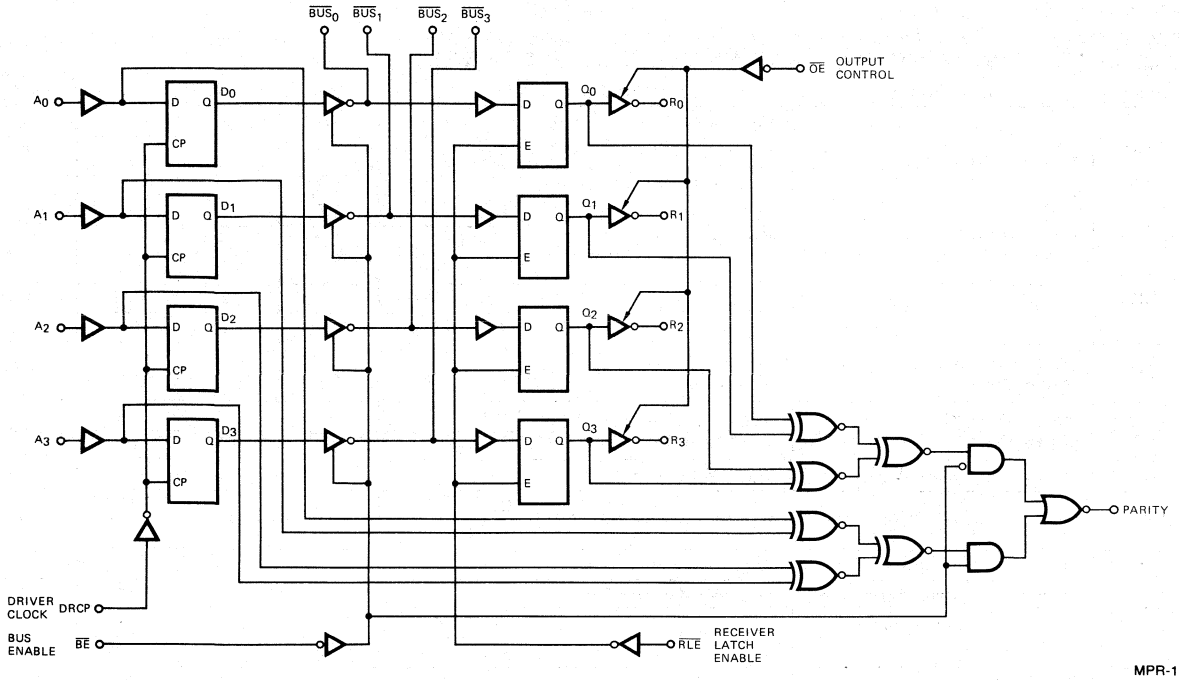
LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

torage Temperature	−65°C to +150°C
emperature (Ambient) Under Bias	−55°C to +125°C
upply Voltage to Ground Potential	−0.5 V to +7 V
C Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
C Input Voltage	−0.5 V to +7 V
C Output Current, Into Outputs (Except BUS)	30 mA
C Output Current, Into Bus	100 mA
C Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2917AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 48 mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20 mA	2.4			Volts
			MIL, I_{OH} = −15 mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5 V V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0 V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2917AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

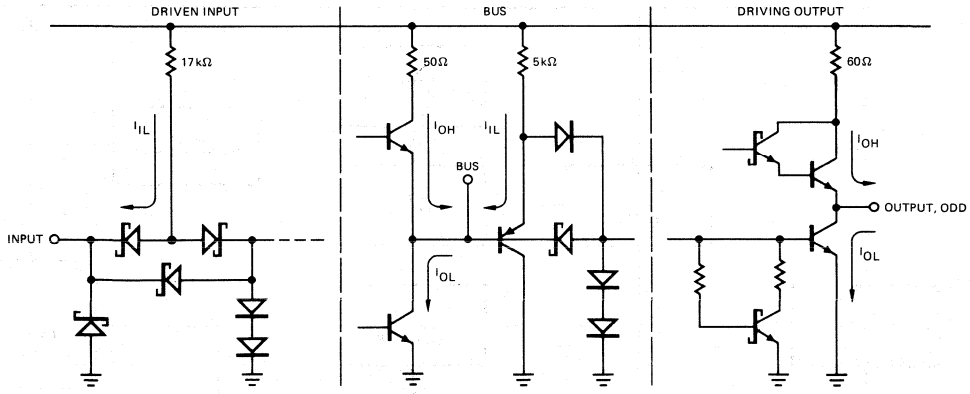
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0 mA		0.27	0.4	Volts
			I_{OL} = 8.0 mA		0.32	0.45	
			I_{OL} = 12 mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			50	μA
			V_O = 0.4 V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2917AXM Min.	Am2917AXM Typ. (Note 2)	Am2917AXM Max.	Am2917AXC Min.	Am2917AXC Typ. (Note 2)	Am2917AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF R_L (BUS) = 130 Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	A Data Inputs	C_L = 15 pF R_L = 2.0 kΩ	15			12			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output Control to Output	C_L = 5 pF, R_L = 2.0 kΩ		14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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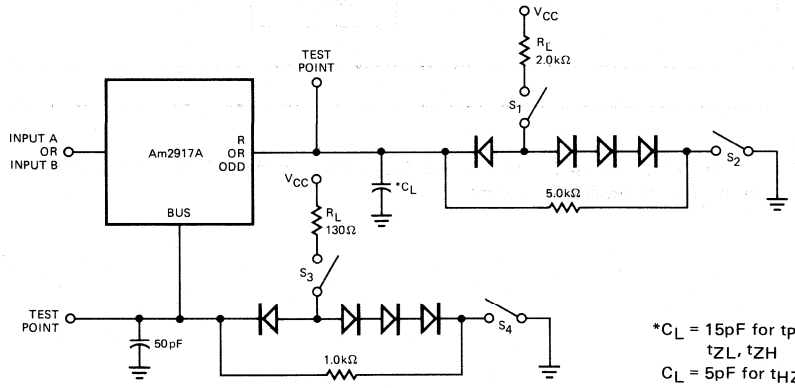
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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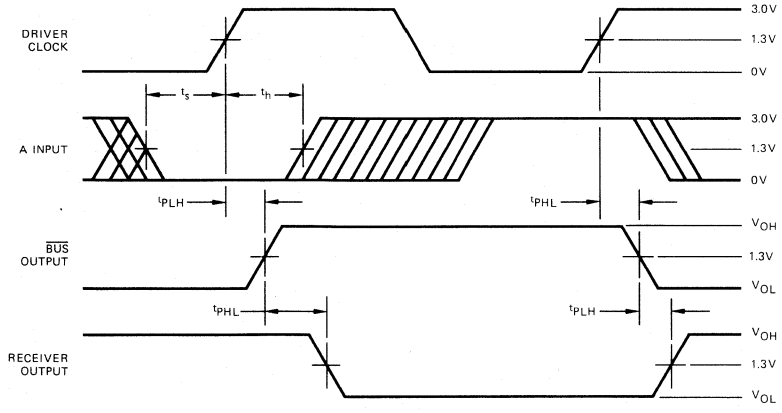
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

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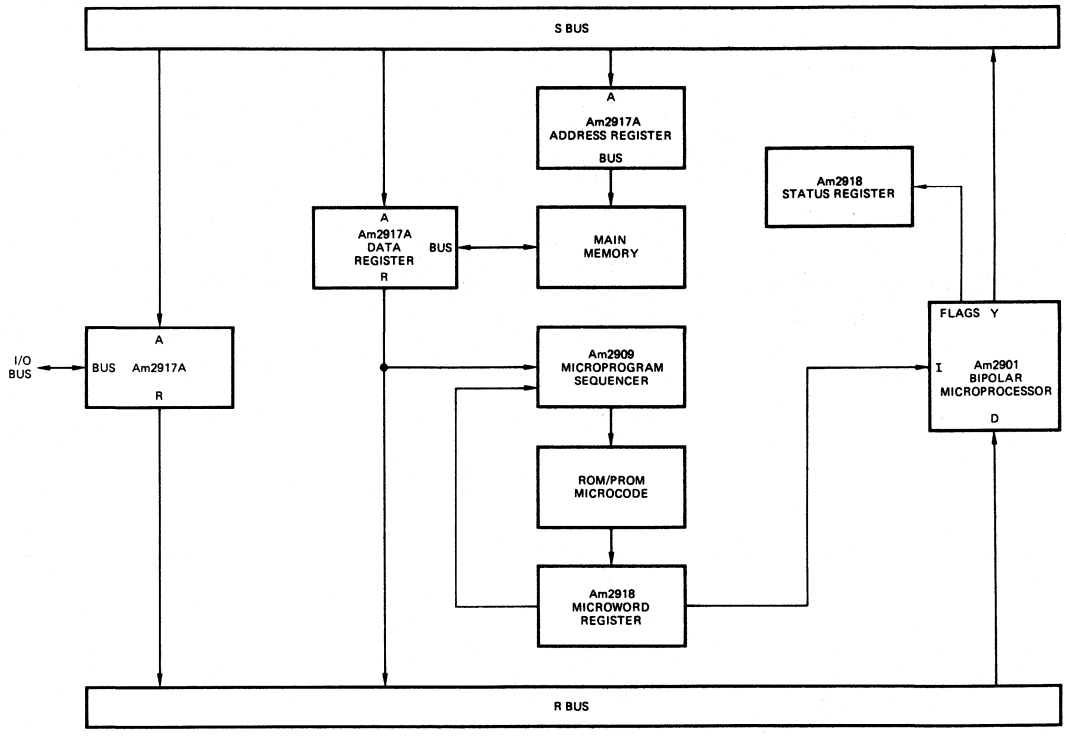
APPLICATIONS



The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

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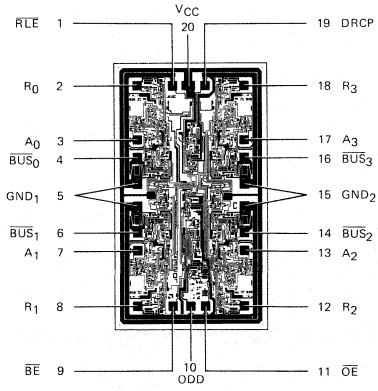
FUNCTION TABLE

INPUTS				INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	BUS_i	R_i	
X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	H	X	X	X	Z	Receiver output disable
X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	H	L	L	X	H	H	L	
X	X	H	X	X	NC	X	X	Latch received data
↑	X	X	X	L	X	X	X	Load driver register
↑	X	X	X	H	X	X	X	
L	X	X	X	NC	X	X	X	No driver clock restrictions
H	X	X	X	NC	X	X	X	
X	L	X	X	L	X	H	X	Drive Bus
X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2917APC	P-20	C	C-1
AM2917ADC	D-20	C	C-1
AM2917ADC-B	D-20	C	B-1
AM2917ADM	D-20	M	C-3
AM2917ADM-B	D-20	M	B-3
AM2917AFM	F-20	M	C-3
AM2917AFM-B	F-20	M	B-3
AM2917AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2917AXM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	$ODD = A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	$ODD = Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

6

Am2918

Quad D Register With Standard And Three-State Outputs

Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

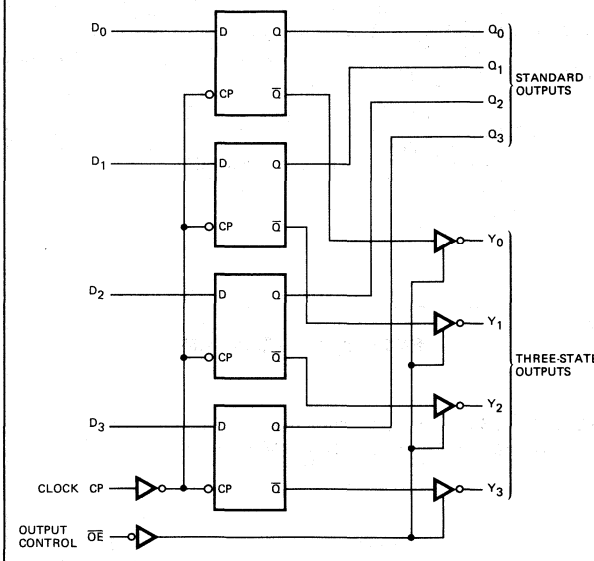
FUNCTIONAL DESCRIPTION

New Schottky circuits such as the Am2918 register provide the design engineer with additional flexibility in system configuration — especially with regard to bus structure, organization and speed. The Am2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the Am2918 register. Other applications of Am2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

LOGIC DIAGRAM



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ORDERING INFORMATION

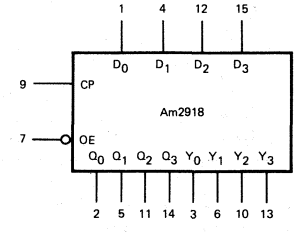
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2918PC	P-16	C	C-1
AM2918DC	D-16	C	C-1
AM2918DC-B	D-16	C	B-1
AM2918DM	D-16	M	C-3
AM2918DM-B	D-16	M	B-3
AM2918FM	F-16	M	C-3
AM2918FM-B	F-16	M	B-3
AM2918XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2918XM	Dice	M	

Notes:

1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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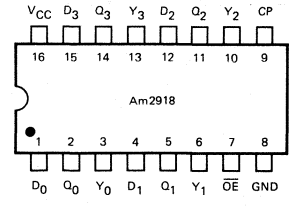
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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XIMUM RATINGS (Above which the useful life may be impaired)

rage Temperature	−65°C to +150°C
nperature (Ambient) Under Bias	−55°C to +125°C
ply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30mA
Input Current	−30mA to +5.0mA

ECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

2918XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
2918XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ± 10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

ameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1mA MIL	2.5	3.4		Volts
				I_{OH} = −1mA COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA; V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	µA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

tes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

itching Characteristics (T_A = +25°C, V_{CC} = 5.0V, R_L = 280Ω)

ameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output		C_L = 15pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)				6.0	9.0	ns
t_{PHL}					8.5	13	
t_{ZH}	Output Control to Output		C_L = 15 pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			C_L = 5.0 pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15pF	75	100		MHz

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

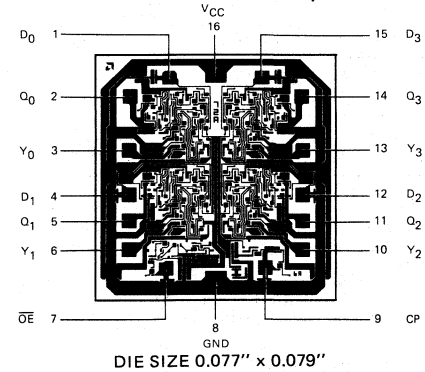
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

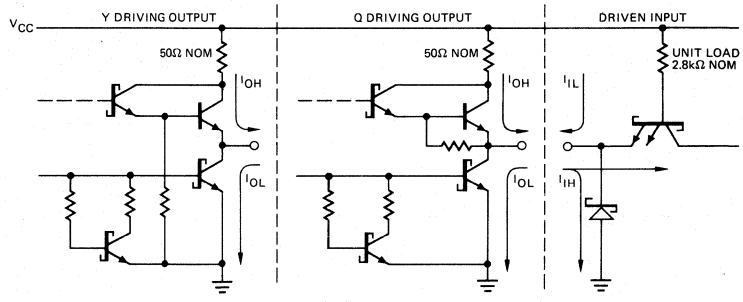
*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

Metallization and Pad Layout



DIE SIZE 0.077" x 0.079"

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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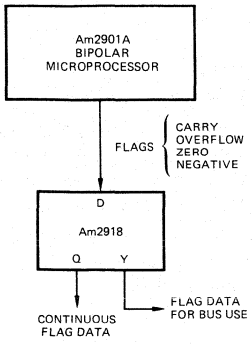
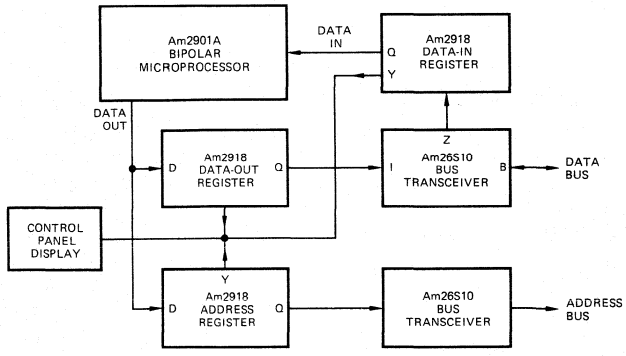
APPLICATIONS



The Am2918 as a 4-Bit status register



The Am2918 used as data-in, data-out and address registers.

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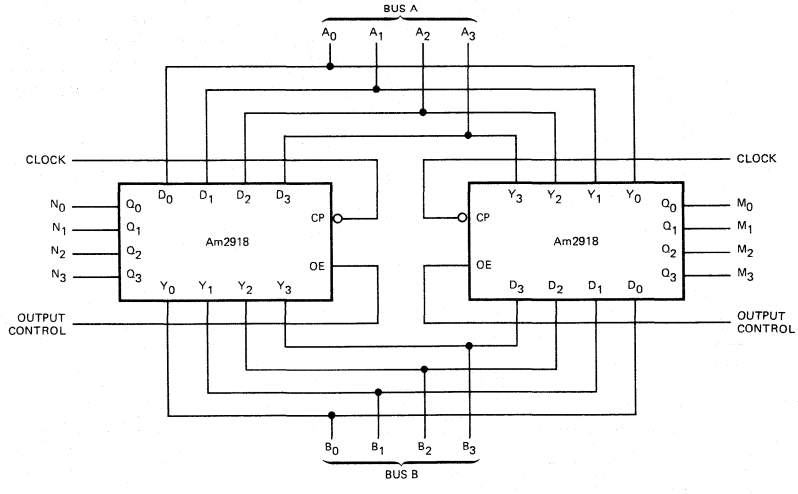

The Am2918 can be connected for bi-directional interface between two buses. The device on the left stores data from the A-bus and drives the A-bus. The device on the right stores data from the B-bus and drives the A-bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.

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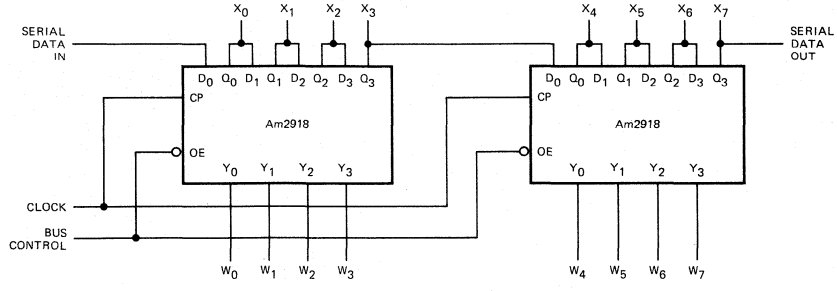

8-Bit serial to parallel converter with three-state output (W) and direct access to the register word (X).

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Am29LS18

Quad D Register With Standard And Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Low-power Schottky version of the popular Am2918
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am29LS18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

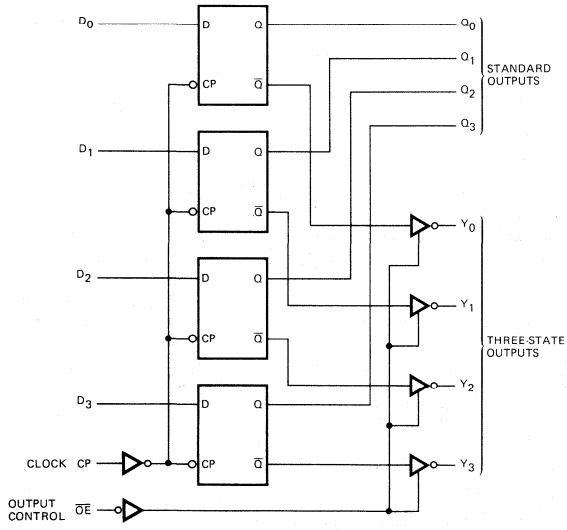
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am29LS18 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am29LS18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

LOGIC DIAGRAM



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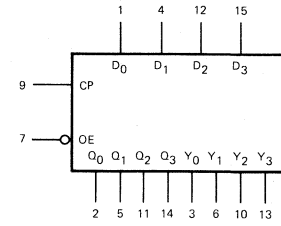
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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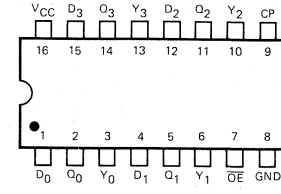
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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LECTRICAL CHARACTERISTICS

ıe Following Conditions Apply Unless Otherwise Specified:

ɔM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75 V MAX. = 5.25 V)
IL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50 V MAX. = 5.50 V)

C CHARACTERISTICS OVER OPERATING RANGE

ırameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q, $I_{OH} = -660\mu A$	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y MIL, $I_{OH} = -1.0mA$		2.4	3.4		
			Y COM'L, $I_{OH} = 2.6mA$		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				17	28	mA

otes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

AXIMUM RATINGS (Above which the useful life may be impaired)

orage Temperature	−65°C to +150°C
ımperature (Ambient) Under Bias	−55°C to +125°C
ıpply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
C Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
C Input Voltage	−0.5 V to +7.0 V
C Output Current, Into Outputs	30 mA
C Input Current	−30 mA to +5.0 mA

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SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				18	27		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	
t_{PHL}				18	27		
t_{pw}	Clock Pulse Width	LOW	18			ns	
		HIGH	15				
t_s	Data		15			ns	
t_h	Data		5.0			ns	
t_{ZH}	$\overline{OE}$ to Y_i			7.0	11	ns	
t_{ZL}				8	12		
t_{HZ}	$\overline{OE}$ to Y_i			14	21	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				12	18		
f_{max}	Maximum Clock Frequency (Note 1)		35	50		MHz	

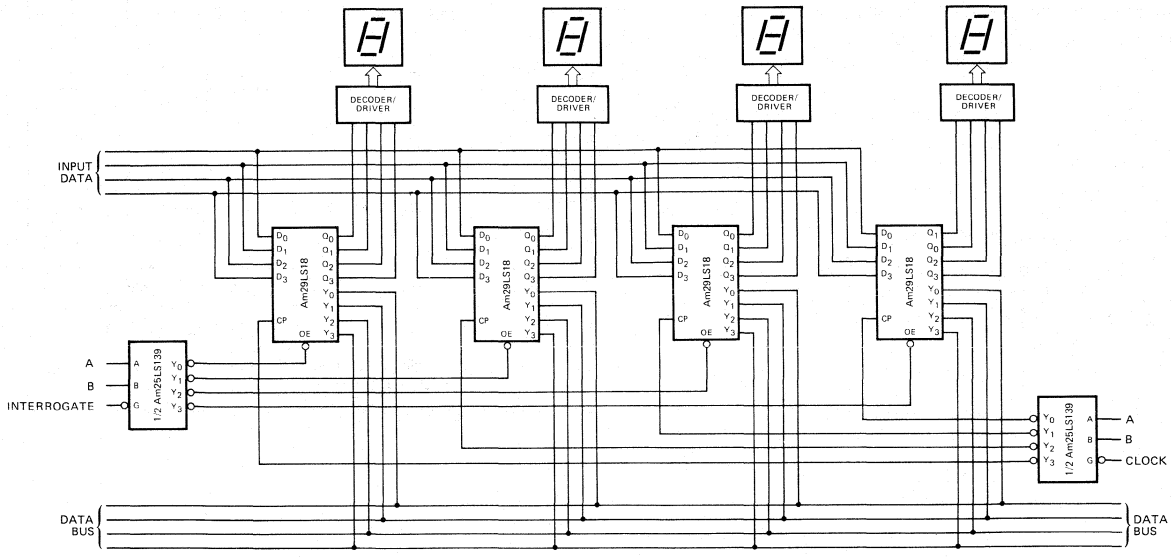
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am29LS18PC, DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%		Am29LS18DM, FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
			Min.	Max.	Min.	Max.		
t_{PLH}	Clock to Q_i			38		45	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				38		45		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			35		40	ns	
t_{PHL}				35		40		
t_{pw}	Clock Pulse Width	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		5.0		5.0		ns	
t_{ZH}	$\overline{OE}$ to Y_i			15		17	ns	
t_{ZL}				16		17		
t_{HZ}	$\overline{OE}$ to Y_i			27		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24		30		
f_{max}	Maximum Clock Frequency (Note 1)		30				MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

APPLICATIONS



The Am29LS18 used as a display register with bus interrogate capability.

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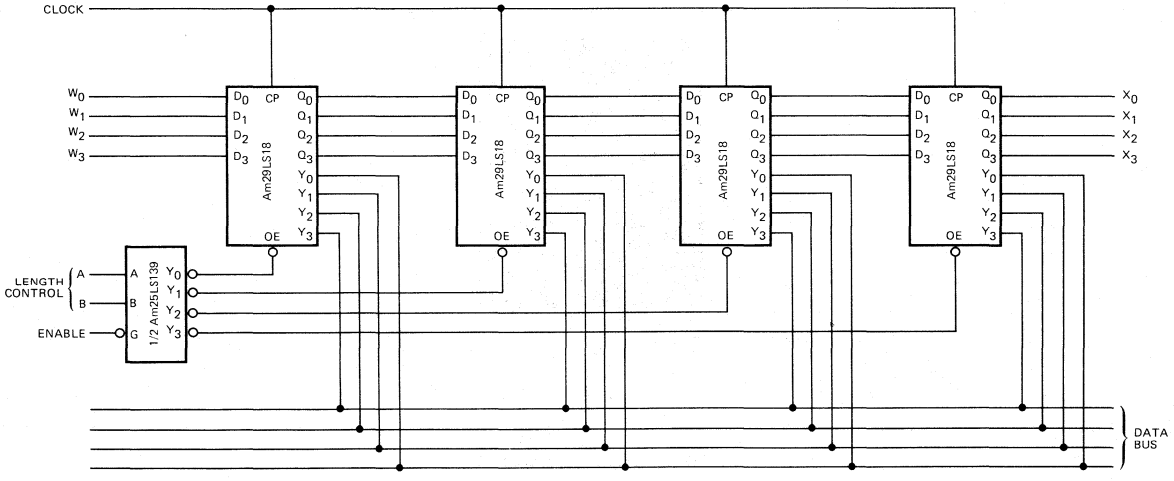
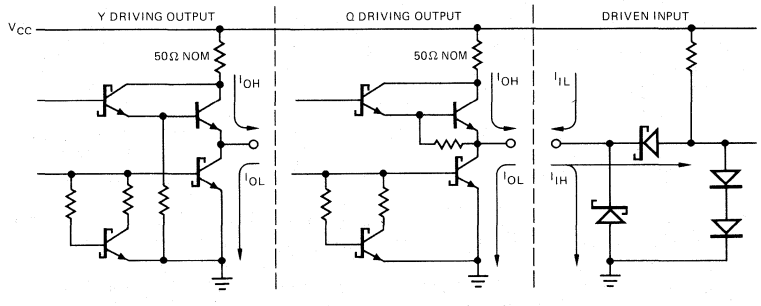


The Am29LS18 as a variable length (1, 2, 3 or 4 word) shift register.

MPR-194

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

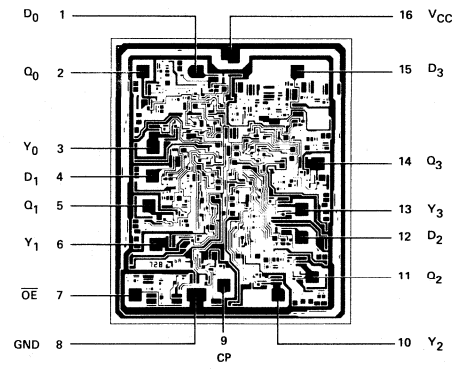
INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

Metallization and Pad Layout



DIE SIZE 0.083" x 0.099"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29LS18PC	P-16	C	C-1
AM29LS18DC	D-16	C	C-1
AM29LS18DC-B	D-16	C	B-1
AM29LS18DM	D-16	M	C-3
AM29LS18DM-B	D-16	M	B-3
AM29LS18FM	F-16	M	C-3
AM29LS18FM-B	F-16	M	B-3
AM29LS18XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29LS18XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = – 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2919

Quad Register With Dual Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Two sets of three-state outputs
- Four D-type flip-flops
- Polarity control on one set of outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2919 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am2919 is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

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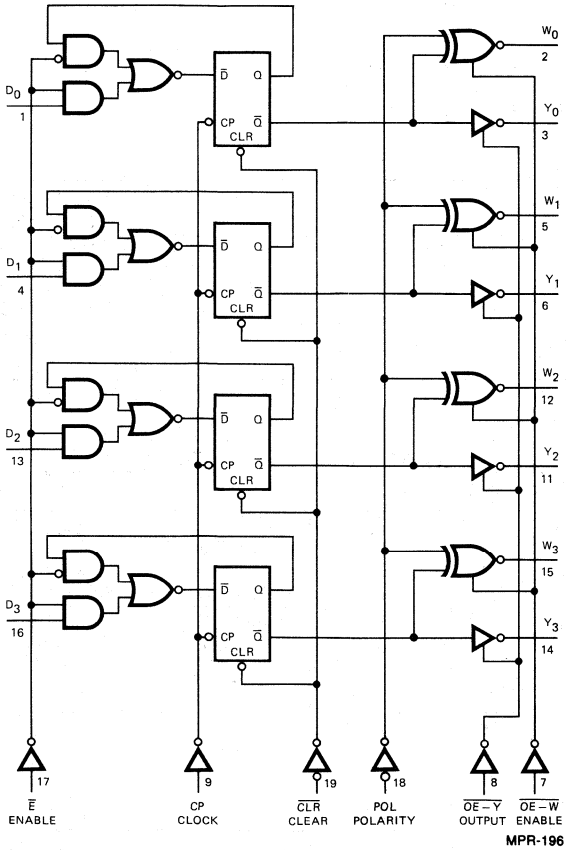
LOGIC DIAGRAM



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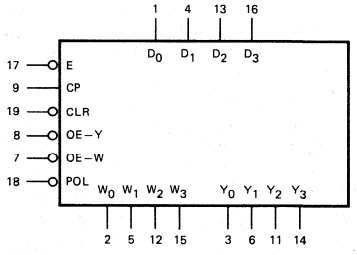
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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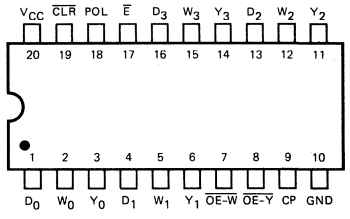
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.	MIL		24	36	mA
			COM'L		24	39	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

FUNCTION TABLE

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE\text{-}W}$	$\overline{OE\text{-}Y}$	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L = LOW H = HIGH Z = High Impedance NC = No Change X = Don't Care ↑ = LOW-to-HIGH Transition

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PHL}	Clock to Y_i			22	33	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				20	30		
t_{PLH}	Clock to W_i (Either Polarity)			24	36	ns	
t_{PHL}				24	36		
t_{PHL}	Clear to Y_i			29	43	ns	
t_{PLH}	Clear to W_i			25	37	ns	
t_{PHL}				30	45		
t_{PLH}	Polarity to W_i			23	34	ns	
t_{PHL}				25	37		
t_{pw}	Clear		18			ns	
t_{pw}	Clock Pulse Width	LOW	15			ns	
		HIGH	18				
t_s	Data		15			ns	
t_h	Data		5			ns	
t_s	Data Enable		20			ns	
t_h	Data Enable		0			ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		20	15		ns	
t_{ZH}	Output Enable to W or Y			11	17	ns	
t_{ZL}				13	20		
t_{HZ}	Output Enable to W or Y			13	20	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				11	17		
f_{max}	Maximum Clock Frequency (Note 1)		35	45		MHz	C_L = 15pF, R_L = 2.0kΩ

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am2919PC, DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am2919PC, DC Max.	Am2919DM, FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am2919DM, FM Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i			39		42	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				39		45		
t_{PLH}	Clock to W_i (Either Polarity)			41		43	ns	
t_{PHL}				44		48		
t_{PHL}	Clear to Y_i			52		58	ns	
t_{PLH}	Clear to W_i			42		43	ns	
t_{PHL}				51		53		
t_{PLH}	Polarity to W_i			41		45	ns	
t_{PHL}				42		44		
t_{pw}	Clear		20		20		ns	
t_{pw}	Clock	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		10		10		ns	
t_s	Data Enable		25		25		ns	
t_h	Data Enable		0		0		ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		23		24		ns	
t_{ZH}	Output Enable to W_i or Y_i			24		27	ns	
t_{ZL}				29		35		
t_{HZ}	Output Enable to W_i or Y_i			33		45	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				22		26		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	C_L = 50pF, R_L = 2.0kΩ

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

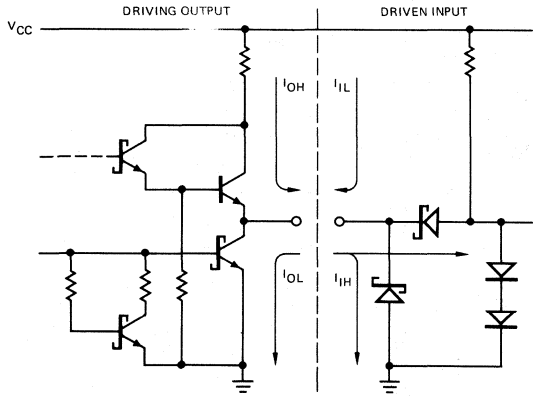
D_i	Any of the four D flip-flop data lines.
$\overline{E}$	Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.
CP	Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.
$\overline{OE\text{-}W}$, $\overline{OE\text{-}Y}$	Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE\text{-}W}$ controls the W set of outputs, and $\overline{OE\text{-}Y}$ controls the Y set.
Y_i	Any of the four non-inverting three-state output lines.
W_i	Any of the four three-state outputs with polarity control.
POL	Polarity Control. The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.
$\overline{CLR}$	Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	D_0	1.0	–	–	–	–
2	W_0	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	D_1	1.0	–	–	–	–
5	W_1	–	50	130	33	33
6	Y_1	–	50	130	33	33
7	$\overline{OE\text{-}W}$	1.0	–	–	–	–
8	$\overline{OE\text{-}Y}$	1.0	–	–	–	–
9	CP	1.0	–	–	–	–
10	GND	–	–	–	–	–
11	Y_2		50	130	33	33
12	W_2		50	130	33	33
13	D_2	1.0	–	–	–	–
14	Y_3	–	50	130	33	33
15	W_3	–	50	130	33	33
16	D_3	1.0	–	–	–	–
17	$\overline{E}$	1.0	–	–	–	–
18	POL	1.0	–	–	–	–
19	$\overline{CLR}$	1.0	–	–	–	–
20	V_{CC}	–	–	–	–	–

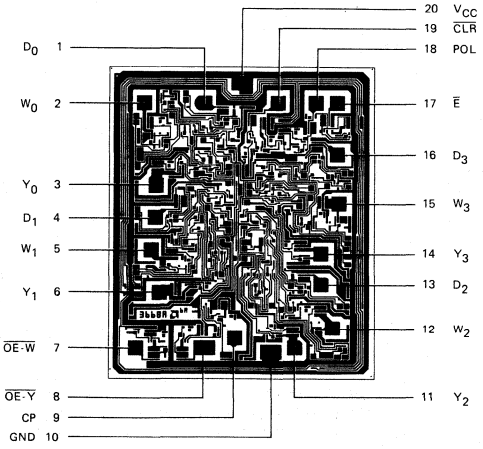
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-199

Metallization and Pad Layout



DIE SIZE 0.083" X 0.099"

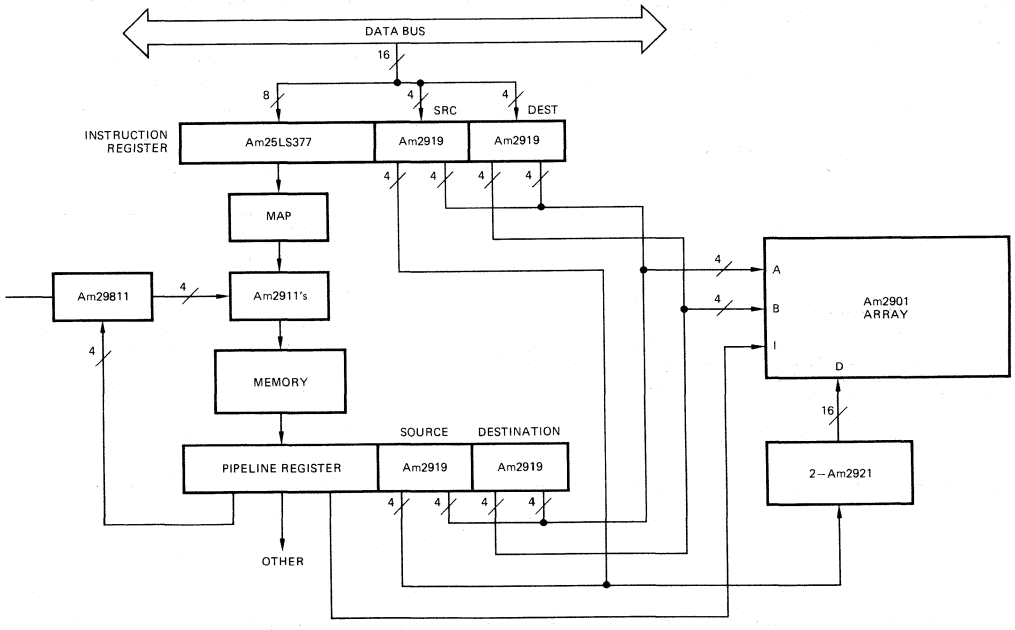
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2919PC	P-20	C	C-1
AM2919DC	D-20	C	C-1
AM2919DC-B	D-20	C	B-1
AM2919DM	D-20	M	C-3
AM2919DM-B	D-20	M	B-3
AM2919FM	F-20	M	C-3
AM2919FM-B	F-20	M	B-3
AM2919XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2919XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



The Am2919 provides for easy control of the selection of source and destination register addresses for the Am2901. These controls can emanate from both the instruction register and the pipeline register. The control is accomplished by three-state action at the Am2919 outputs. Four different register outputs can be selected by the B address which is the destination register in the Am2901. Two registers can be selected for the Am2901 A input which is a second RAM source.

The other pair of three-state outputs can be used for function control select as shown with the Am2921. Here, bit set, bit clear, bit toggle and bit test on any of the 16 bits can be performed.

MPR-200

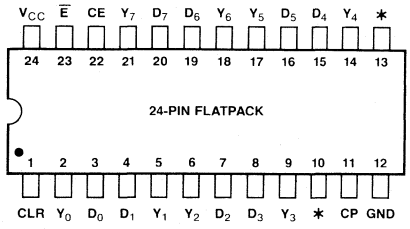
Am2920

Octal D-Type Flip-Flop With Clear, Clock Enable And Three-State Control

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation. *Reserved – do not use.

FUNCTIONAL DESCRIPTION

The Am2920 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

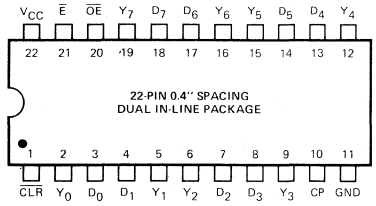
When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

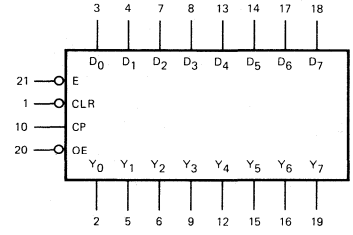
This device is packaged in a space-saving (0.4-inch row spacing) 22-pin package and in a 24-pin flatpack.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

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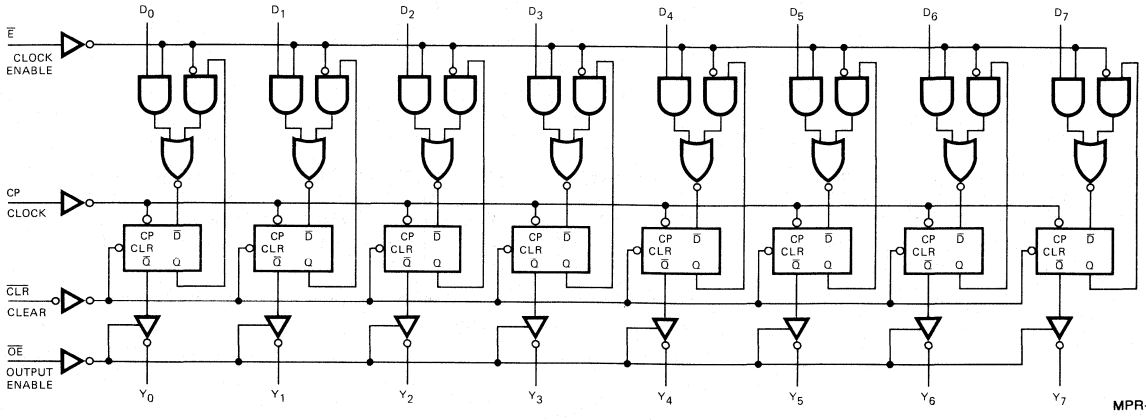
LOGIC DIAGRAM



MPR-201

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			24	37	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

6

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2920PC	P-22	C	C-1
AM2920DC	D-22	C	C-1
AM2920DC-B	D-22	C	B-1
AM2920DM	D-22	M	C-3
AM2920DM-B	D-22	M	B-3
AM2920FM	F-24	M	C-3
AM2920FM-B	F-24	M	B-3
AM2920XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2920XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				24	36		
t_{PHL}	Clear to Y			22	35	ns	
t_s	Data (D_i)		10	3		ns	
t_h	Data (D_i)		10	3		ns	
t_s	Enable ($\overline{E}$)	Active	15	10		ns	
		Inactive	20	12			
t_h	Enable ($\overline{E}$)		0	0		ns	
t_s	Clear Recovery (In-Active) to Clock		11	7		ns	
t_{pw}	Clock	HIGH	20	14		ns	
		LOW	25	13			
t_{pw}	Clear		20	13		ns	
t_{ZH}	$\overline{OE}$ to Y_i			9	13	ns	
t_{ZL}				14	21		
t_{HZ}	$\overline{OE}$ to Y_i			20	30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24	36		
f_{max}	Maximum Clock Frequency (Note 1)			40		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am2920PC,DC T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	Am2920PC,DC Max.	Am2920DM,FM T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	Am2920DM,FM Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			33		39	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				45		54		
t_{PHL}	Clear to Y			43		61	ns	
t_s	Data (D_i)		12		15		ns	
t_h	Data (D_i)		12		15		ns	
t_s	Enable ($\overline{E}$)	Active	17		20		ns	
		Inactive	20		23			
t_h	Enable ($\overline{E}$)		0		0		ns	
t_s	Clear Recovery (In-Active) to Clock		13		15		ns	
t_{pw}	Clock	HIGH	25		30		ns	
		LOW	30		35			
t_{pw}	Clear		22		25		ns	
t_{ZH}	$\overline{OE}$ to Y_i			19		25	ns	
t_{ZL}				30		39		
t_{HZ}	$\overline{OE}$ to Y_i			35		40	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				39		42		
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i — The D flip-flop data inputs.

$\overline{CLR}$ — When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.

CP — Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i — The register three-state outputs.

$\overline{E}$ — Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.

$\overline{OE}$ — Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

FUNCTION TABLE

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

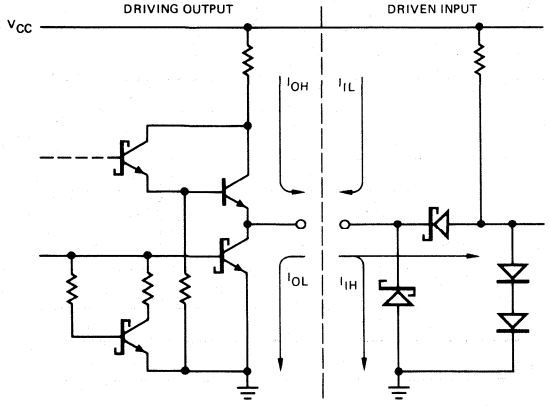
H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

		Am2920				
			Output HIGH		Output LOW	
Pin No.'s	Input/Output	Input Load	MIL	COM'L	MIL	COM'L
1	$\overline{CLR}$	1	—	—	—	—
2	Y_0	—	50	130	22	22
3	D_0	1	—	—	—	—
4	D_1	1	—	—	—	—
5	Y_1	—	50	130	22	22
6	Y_2	—	50	130	22	22
7	D_2	1	—	—	—	—
8	D_3	1	—	—	—	—
9	Y_3	—	50	130	22	22
10	CP	1	—	—	—	—
11	GND	—	—	—	—	—
12	Y_4	—	50	130	22	22
13	D_4	1	—	—	—	—
14	D_5	1	—	—	—	—
15	Y_5	—	50	130	22	22
16	Y_6	—	50	130	22	22
17	D_6	1	—	—	—	—
18	D_7	1	—	—	—	—
19	Y_7	—	50	130	22	22
20	$\overline{OE}$	1	—	—	—	—
21	$\overline{E}$	1	—	—	—	—
22	V_{CC}	—	—	—	—	—

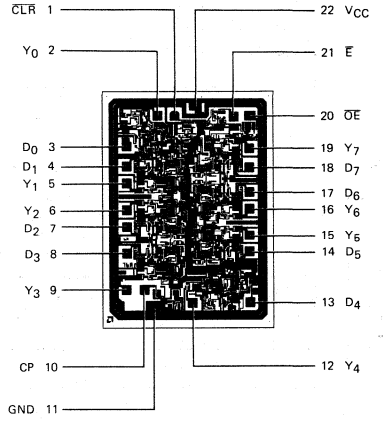
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-204

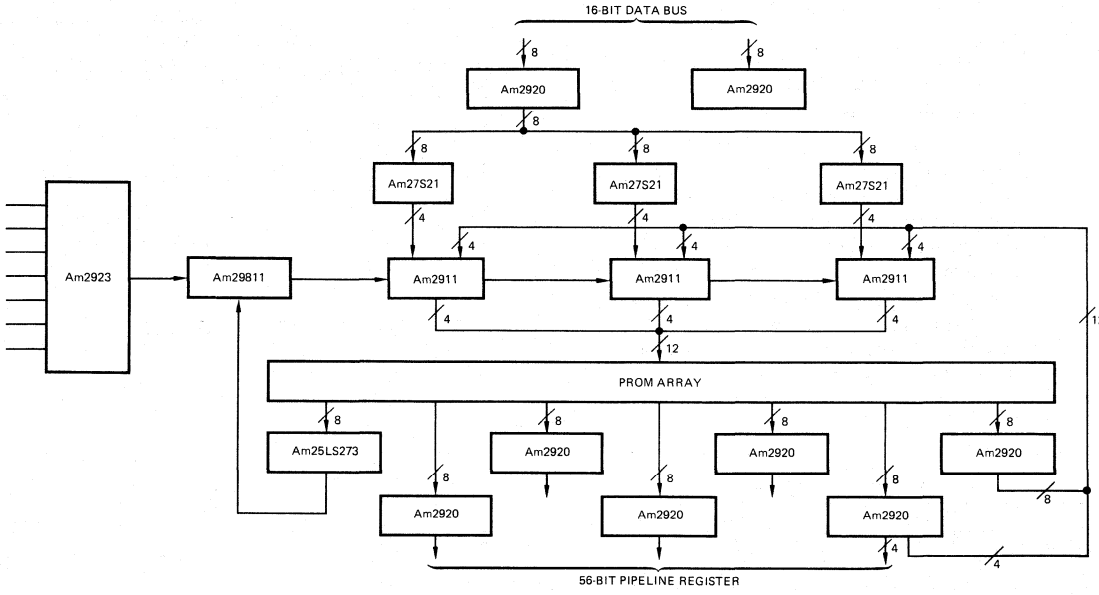
Metallization and Pad Layout



DIE SIZE 0.080" X 0.111"

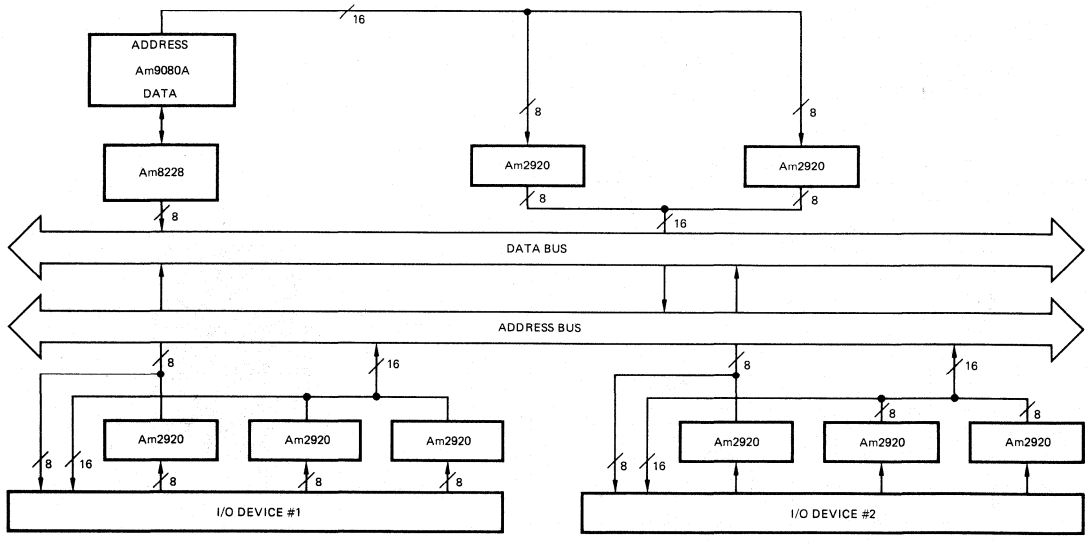
6

APPLICATIONS



A typical Computer Control Unit for a microprogrammed machine.

MPR-205



The Am2920 is a useful device in interfacing with the Am9080A system buses.

MPR-206

Am2921

One-of-Eight Decoder
With Three-State Outputs And Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- AC parameters specified over operating temperature and power supply ranges.
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

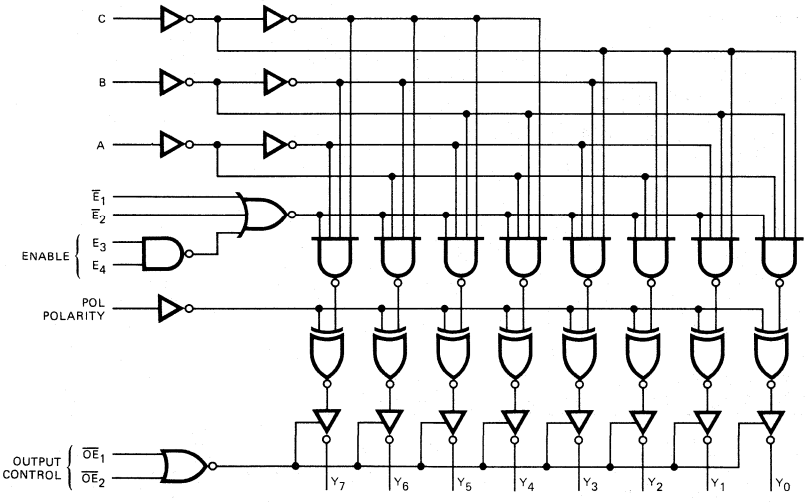
The Am2921 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B, and C, which are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package.

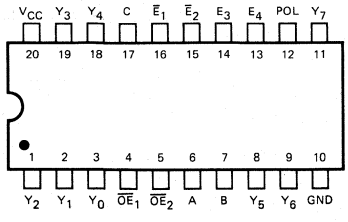
6

LOGIC DIAGRAM
One-of-Eight Decoder



MPR-207

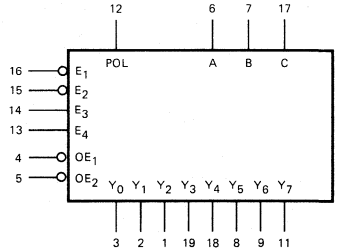
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-208

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-209

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = 1.0mA$ (MIL)	2.4	3.4		Volts
			$I_{OH} = -2.6mA$ (COM'L)	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			21	34	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1 = \overline{E}_2$ = GND : $E_3 = E_4$ = POL = $\overline{OE}_1 = \overline{OE}_2 = 4.5V$.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +7.0
DC Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5.0 m

WITCHING CHARACTERISTICS

A = +25°C, V_{CC} = 5.0V)

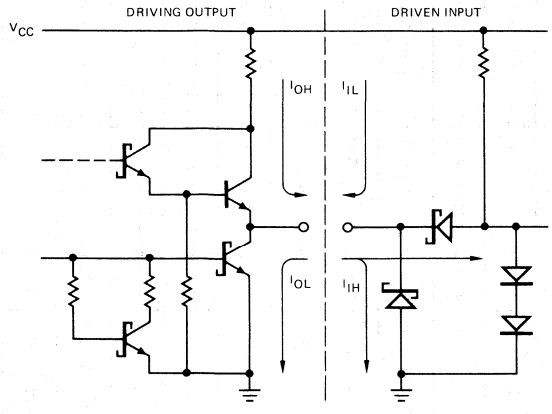
rameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		20	30	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			15	22		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		19	28	ns	
t_{PHL}			20	30		
t_{PLH}	E_3, E_4 to Y_i		21	31	ns	
t_{PHL}			23	34		
t_{PLH}	POL to Y_i		16	24	ns	
t_{PHL}			20	30		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	
t_{ZL}			14	21		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}			20	30		

WITCHING CHARACTERISTICS VER OPERATING RANGE*

		Am2921PC, DC T_A = 0°C to +70°C V_{CC} = 5.0V ± 5%		Am2921DM, FM T_A = –55°C to +125°C V_{CC} = 5.0V ± 10%			
rameters	Description	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		36		42	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			29		37		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		34		39	ns	
t_{PHL}			38		45		
t_{PLH}	E_3, E_4 to Y_i		38		45	ns	
t_{PHL}			43		52		
t_{PLH}	POL to Y_i		29		34	ns	
t_{PHL}			39		49		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		38		45	ns	
t_{ZL}			23		25		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		29		33	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}			33		36		

AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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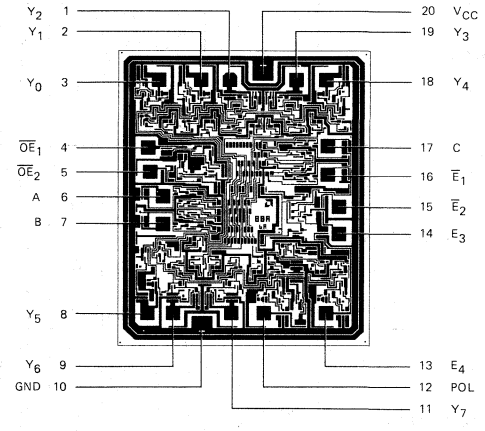
Metallization and Pad Layout



DIE SIZE 0.081" X 0.096"

6

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D — The three select inputs to the decoder/demultiplexer.

$\overline{E}_1$, $\overline{E}_2$ — The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.

E_3, E_4 — The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited.

POL — Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.

$\overline{OE}_1$, $\overline{OE}_2$ — Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high impedance state.

Y_i — The eight outputs for the decoder/demultiplexer.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	Y_2	–	50	130	33	33
2	Y_1	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	$\overline{OE}_1$	1.0	–	–	–	–
5	$\overline{OE}_2$	1.0	–	–	–	–
6	A	1.0	–	–	–	–
7	B	1.0	–	–	–	–
8	Y_5	–	50	130	33	33
9	Y_6	–	50	130	33	33
10	GND	–	–	–	–	–
11	Y_7	–	50	130	33	33
12	POL	1.0	–	–	–	–
13	E_4	1.0	–	–	–	–
14	E_3	1.0	–	–	–	–
15	$\overline{E}_2$	1.0	–	–	–	–
16	$\overline{E}_1$	1.0	–	–	–	–
17	C	1.0	–	–	–	–
18	Y_4	–	50	130	33	33
19	Y_3	–	50	130	33	33
20	V_{CC}	–	–	–	–	–

FUNCTION TABLE

FUNCTION	INPUTS										OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	POL	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High Impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	H	X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	H	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	H	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	L	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	L	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	X	L	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	X	L	H	X	X	X	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	L	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output	L	L	L	L	H	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH L = LOW X = Don't Care Z = High Impedance

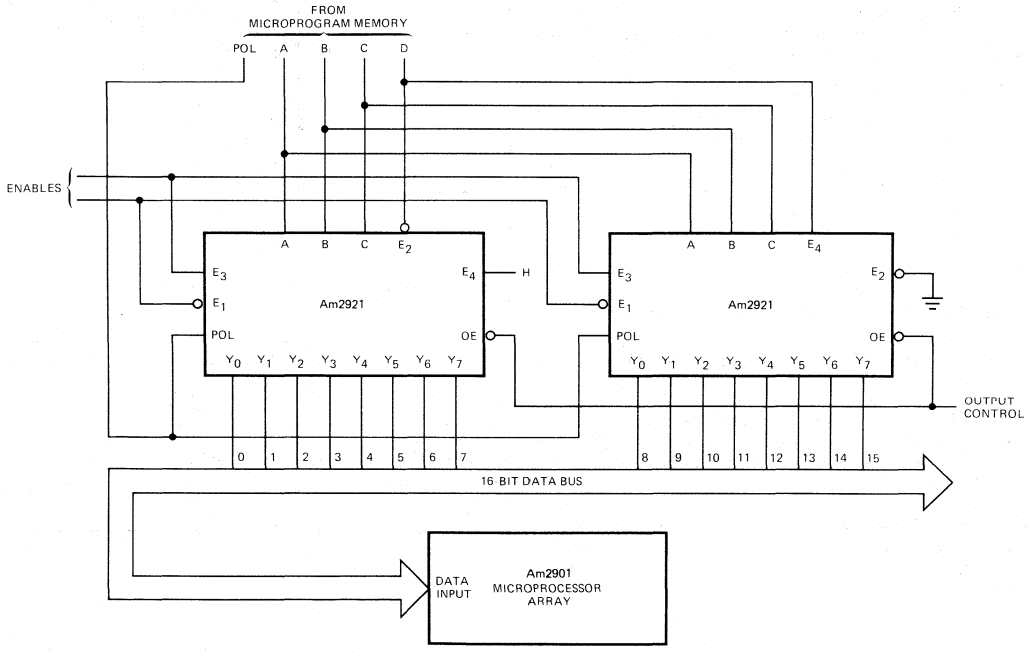
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2921PC	P-20	C	C-1
AM2921DC	D-20	C	C-1
AM2921DC-B	D-20	C	B-1
AM2921DM	D-20	M	C-3
AM2921DM-B	D-20	M	B-3
AM2921FM	F-20	M	C-3
AM2921FM-B	F-20	M	B-3
AM2921XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2921XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



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Two Am2921's can be used to perform a bit set, bit clear, bit toggle or bit test on any of sixteen bits in a microprocessor system. Examples of the operations performed are as follows:

Microprogram Control					16-Bit Field From Am2921															Am2901 ALU Function	Bit Function Performed On Selected Register
D	C	B	A	POL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	OR	BIT SET
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	AND	BIT TEST
0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	AND	BIT CLEAR
1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	EX NOR	BIT TOGGLE
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	EX OR	BIT TOGGLE

Note: Bit test is performed using F = 0 output of Am2901A.

Am2922

Eight Input Multiplexer With Control Register

DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Common register enable
- Asynchronous register clear
- Three-state output for expansion
- AC parameters specified over operating temperature and power supply ranges.
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am2922 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

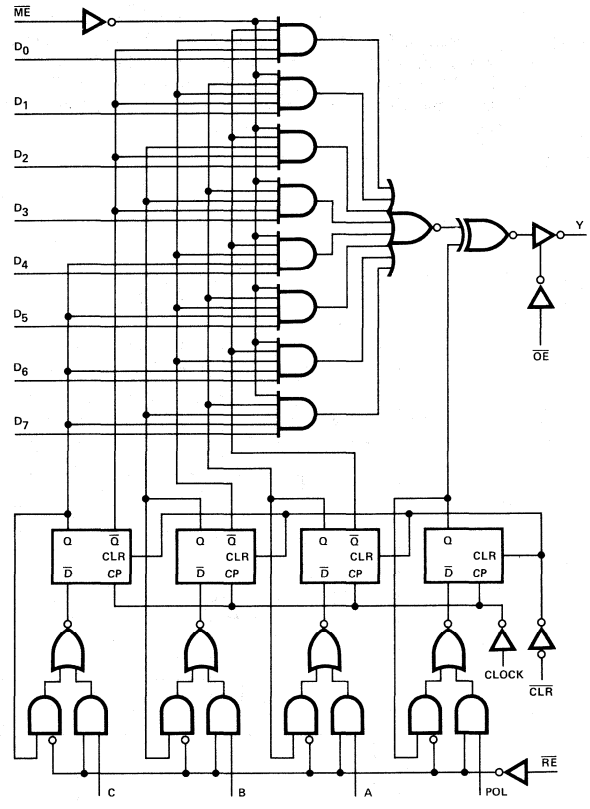
The Am2922 contains an internal register which holds the A, B and C multiplexer select lines as well as the POL (Polarity) control bit. When the Register Enable input ($\overline{RE}$) is LOW, new data is entered into the register on the LOW-to-HIGH, transition of the clock. When $\overline{RE}$ is HIGH, the register retains its current data. An asynchronous clear input ($\overline{CLR}$) is used to reset the register to a logic LOW level.

The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

An active LOW Multiplexer Enable input ($\overline{ME}$) allows the selected multiplexer input to be passed to the output. When $\overline{ME}$ is HIGH, the output is determined only by the Polarity Control bit.

The Am2922 also features a three-state Output Enable control ($\overline{OE}$) for expansion. When $\overline{OE}$ is LOW, the output is enabled. When $\overline{OE}$ is HIGH, the output is in the high impedance state.

LOGIC DIAGRAM



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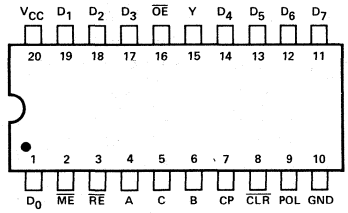
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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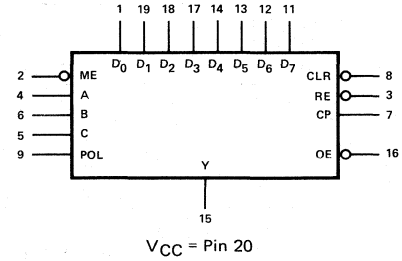
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -2.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -6.5mA$		2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 20mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$				−0.72	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$				−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$				40	μA
			D_N, A, B, C, POL, CP, $\overline{CLR}$				50	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$				0.1	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$				1.0	
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−50	μA
			$V_O = 2.4V$				50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				97	148	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. D_N, A, B, C, POL, $\overline{ME}$ at Gnd. All other inputs and outputs open. Measured after a momentary ground then 4.5V applied to clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

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SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y POL – LOW		21	32	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			19	29		
t_{PLH}	Clock to Y POL – HIGH		16	24	ns	
t_{PHL}			19	29		
t_{PLH}	D_n to Y		10	16	ns	
t_{PHL}			13	19		
t_{PLH}	CLR to Y		22	33	ns	
t_{PHL}			22	33		
t_{PLH}	$\overline{ME}$ to Y		12	18	ns	
t_{PHL}			12	18		
t_{ZL}	$\overline{OE}$ to Y		8	14	ns	
t_{ZH}			8	14		
t_{LZ}			10	17	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			10	17		
t_S	A, B, C, POL	10			ns	C_L = 15pF, R_L = 2.0kΩ
	CE	15				
t_S	CLR Recovery	5			ns	
t_{pw}	Clock	10			ns	
	Clear (LOW)	10				
t_h	A, B, C, POL, CE	0			ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2922PC, DC T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am2922PC, DC Max.	Am2922DM, FM T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am2922DM, FM Max.	Units	Test Conditions
t_{PLH}	Clock to Y, POL-L		40		47	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			34		38		
t_{PLH}	Clock to Y, POL-H		29		33	ns	
t_{PHL}			35		41		
t_{PLH}	D_N to Y		19		21	ns	
t_{PHL}			22		24		
t_{PLH}	CLR to Y		39		45	ns	
t_{PHL}			39		45		
t_{PLH}	$\overline{ME}$ to Y		22		26	ns	
t_{PHL}			19		20		
t_{ZL}	$\overline{OE}$ to Y		19		24	ns	
t_{ZH}			22		29		
t_{LZ}	$\overline{OE}$ to Y		24		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			24		30		
t_S	A, B, C POL	11		12		ns	C_L = 50pF, R_L = 2.0kΩ
	CE	18		20			
t_S	CLR Recovery	6		7		ns	
t_{pw}	Clock	11		12		ns	
	Clear (LOW)	11		12			
t_H	A, B, C, POL, CE	3		3		ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

A, B, C Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.

POL Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.

$\overline{ME}$ Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.

$\overline{RE}$ Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.

$\overline{CLR}$ Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.

D_1-D_8 Data Inputs to the 8-input multiplexer.

CP Clock Pulse. When $\overline{RE}$ is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.

$\overline{OE}$ Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high impedance state.

Y The chip output.

FUNCTION TABLE

MODE	INPUTS							INTERNAL				INPUTS		OUTPUT
	C	B	A	POL	$\overline{RE}$	$\overline{CLR}$	CP	Q_C	Q_B	Q_A	Q_{POL}	$\overline{ME}$	$\overline{OE}$	Y
Clear	X	X	X	X	X	L	X	L	L	L	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	L	L	$\overline{D}_0$
												X	H	Z
Reg. Disable	X	X	X	X	H	H	X	NC	NC	NC	NC	L	L	$\overline{D}_i/D_i$ (Note 1)
Select (Multiplex)	L	L	L	L/H	L	H	↑	L	L	L	L/H	L	L	$\overline{D}_0/D_0$
	L	L	H					L	L	H				$\overline{D}_1/D_1$
	L	H	L					L	H	L				$\overline{D}_2/D_2$
	L	H	H					L	H	H				$\overline{D}_3/D_3$
	H	L	L					H	L	L				$\overline{D}_4/D_4$
	H	L	H					H	L	H				$\overline{D}_5/D_5$
	H	H	L					H	H	L				$\overline{D}_6/D_6$
	H	H	H	↓	↓	↓	↓	H	H	H	↓	↓	↓	$\overline{D}_7/D_7$
Multiplexer Disable	X	X	X	X	X	H	X	X	X	X	L	H	L	H
								X	X	X	H	H	L	L
Tri-state Output Disable	↓	↓	↓	↓	↓	↓	↓	X	X	X	X	X	H	Z

NC = No Change
X = Don't Care

Note 1: The output will follow the selected input, D_i, or its complement depending on the state of the POL flip-flop.

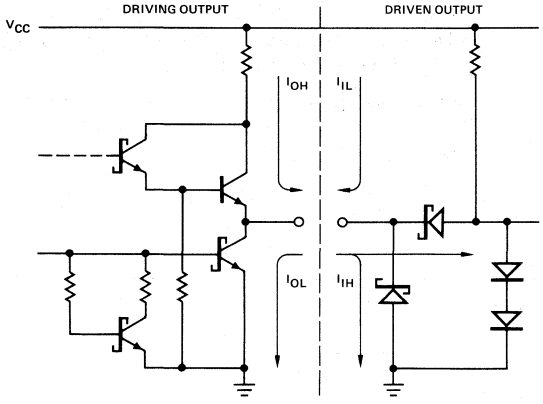
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2922PC	P-20	C	C-1
AM2922DC	D-20	C	C-1
AM2922DC-B	D-20	C	B-1
AM2922DM	D-20	M	C-3
AM2922DM-B	D-20	M	B-3
AM2922FM	F-20	M	C-3
AM2922FM-B	F-20	M	B-3
AM2922XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2922XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

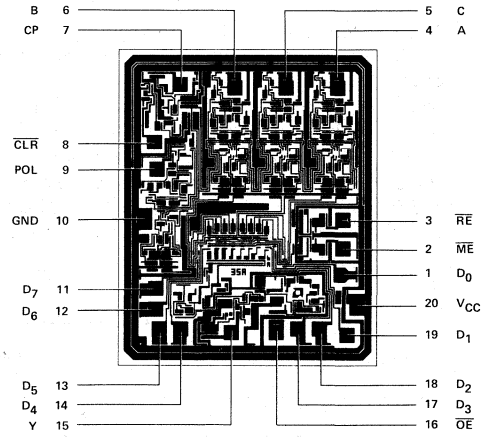
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

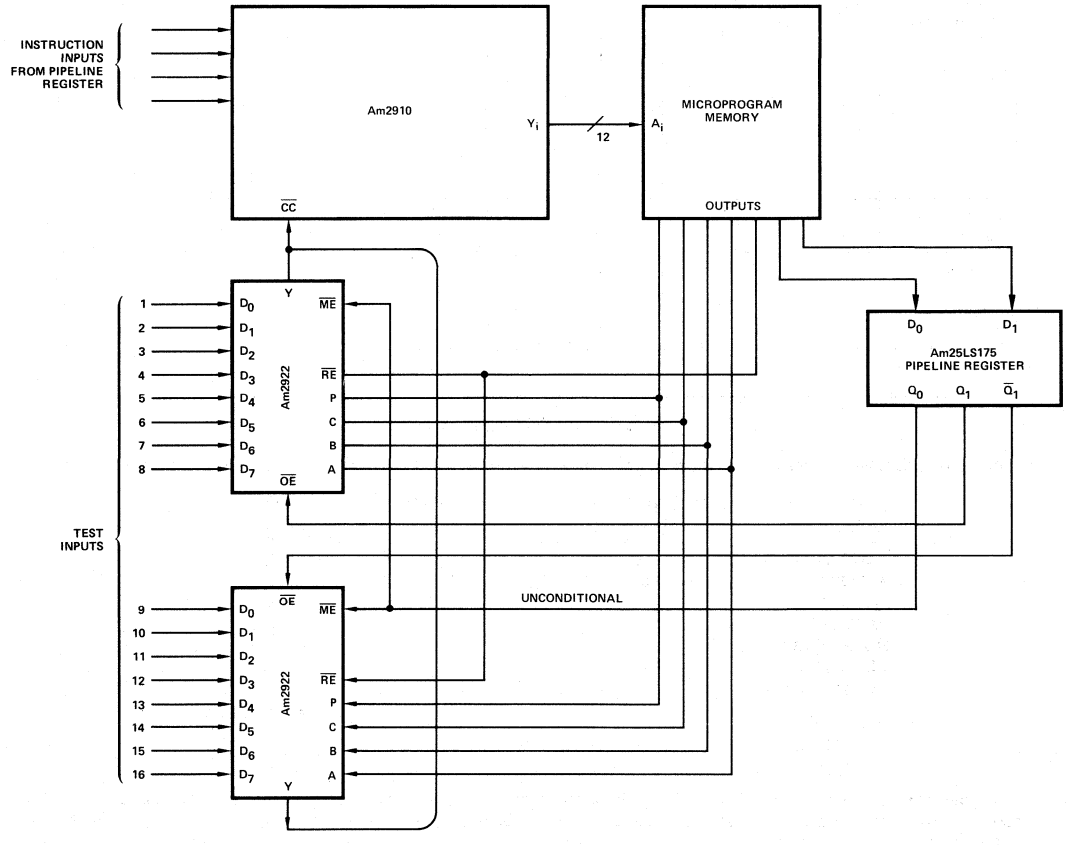
MPR-215

Metallization and Pad Layout



DIE SIZE 0.080" X 0.099"

APPLICATION



A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

MPR-216

Am2923
Eight-Input Multiplexer

Distinctive Characteristics

- Advanced Schottky technology
- Switches one of eight inputs to two complementary outputs
- 3-state output for bus organized systems
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2923 is an 8-input multiplexer that switches one of eight inputs onto the inverting and non-inverting outputs under the control of a 3-bit select code. The inverting output is one gate delay faster than the non-inverting output.

The Am2923 features a 3-state output for data bus organization. The active-LOW strobe, or "output control" applies to both the inverting and non-inverting output. When the output control is HIGH, the outputs are in the high-impedance state. When the output control is LOW, the active pull-up output is enabled.

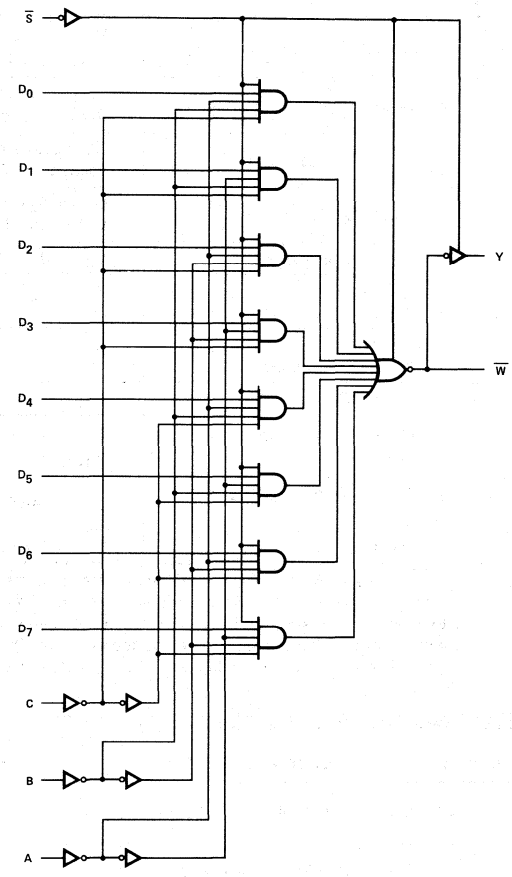
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2923PC	P-16-1	C	C-1
AM2923DC	D-16-1	C	C-1
AM2923DC-B	D-16-1	C	B-1
AM2923DM	D-16-1	M	C-3
AM2923DM-B	D-16-1	M	B-3
AM2923FM	F-16-1	M	C-3
AM2923FM-B	F-16-1	M	B-3
AM2923XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am2923XM	Dice	M	

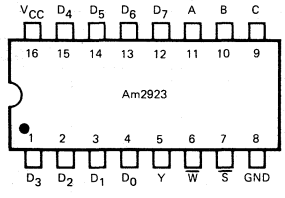
Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

LOGIC DIAGRAM



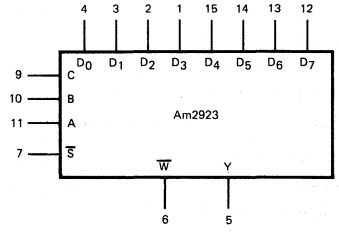
BLI-069

CONNECTION DIAGRAM
Top View



BLI-070

LOGIC SYMBOL



BLI-071

MAXIMUM RATINGS (Above which the useful life may be impaired).

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to + V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Output	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2923PC, DC, XC T_A =0 to 70°C V_{CC} = 5.0V ±5% (COM'L) MIN = 4.75V MAX = 5.25V
Am2923DM, FM, XM T_A = −55.to +125°C V_{CC} = 5.0V ±10% (MIL) MIN = 4.5V MAX = 5.5V

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	MIL	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −2mA	2.4	3.4		Volts
		COM'L		I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage		V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current		V_{CC} = MAX, V_{IN} = 0.5				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7				50	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 5.5V				1	mA
$I_{O(off)}$	Off-State (High-Impedance) Output Current		V_{CC} = MAX, V_{IN} = V_{IH} or V_{IL}	V_O = 2.4V			50	μA
				V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current (Note 4)		V_{CC} = MAX, V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current		V_{CC} = MAX (Note 5)			55	85	mA

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all inputs at 4.5V.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B, or C to Y; 4 Levels of Delay	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15pF		12	18	ns
t_{PHL}				13	19.5	
t_{PLH}	A, B, or C to $\overline{W}$; 3 Levels of Delay			10	15	ns
t_{PHL}				9	13.5	
t_{PLH}	Any D to Y			8	12	ns
t_{PHL}				8	12	
t_{PLH}	Any D to $\overline{W}$			4.5	7	ns
t_{PHL}				4.5	7	
t_{ZH}	Output Enable to Y	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15pF		13	19.5	ns
t_{ZL}				14	21	
t_{ZH}	Output Enable to $\overline{W}$			13	19.5	ns
t_{ZL}				14	21	
t_{HZ}	Output Enable to Y	V_{CC} = 5.0V, R_L = 280Ω, C_L = 5pF		5.5	8.5	ns
t_{LZ}				9	14	
t_{HZ}	Output Enable to $\overline{W}$			5.5	8.5	ns
t_{LZ}				9	14	

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			Output Control		
C	B	A	$\overline{S}$	Y	$\overline{W}$
X	X	X	H	Z	Z
L	L	L	L	D_0	D_0
L	L	H	L	D_1	D_1
L	H	L	L	D_2	D_2
L	H	H	L	D_3	D_3
H	L	L	L	D_4	D_4
H	L	H	L	D_5	D_5
H	H	L	L	D_6	D_6
H	H	H	L	D_7	D_7

H = HIGH X = Don't Care
L = LOW Z = High Impedance

D_0–D_7 = The output will follow the HIGH-level or LOW-level of the selected input.

$\overline{D}_0$–$\overline{D}_7$ = The output will follow the complement of the HIGH-level or LOW-level of the selected input.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_3	1	1	–	–
D_2	2	1	–	–
D_1	3	1	–	–
D_0	4	1	–	–
Y	5	–	20	10
$\overline{W}$	6	–	20	10
$\overline{S}$	7	1	–	–
GND	8	–	–	–
C	9	1	–	–
B	10	1	–	–
A	11	1	–	–
D_7	12	1	–	–
D_6	13	1	–	–
D_5	14	1	–	–
D_4	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS

A, B, C The three select inputs of the multiplexer.

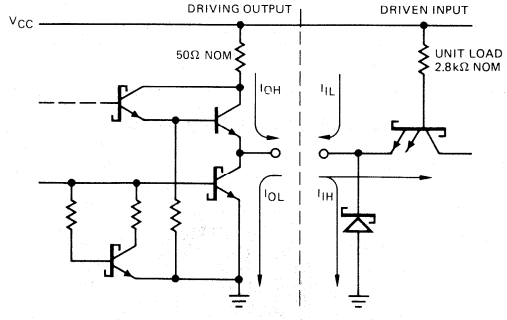
D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7 The eight data inputs of the multiplexer.

Y The true multiplexer output.

$\overline{W}$ The complement multiplexer output.

$\overline{S}$ Output Control. HIGH on the output control (or strobe) forces both the $\overline{W}$ and Y outputs to the high-impedance (off) state.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

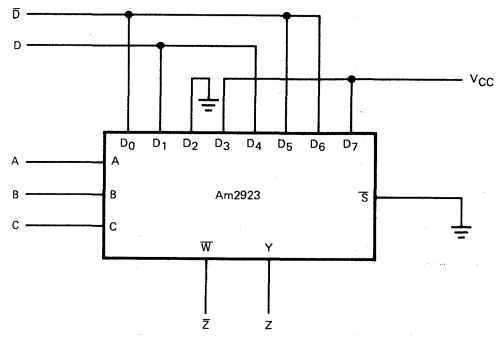


Note: Actual current flow direction shown.

BLI-072

APPLICATIONS

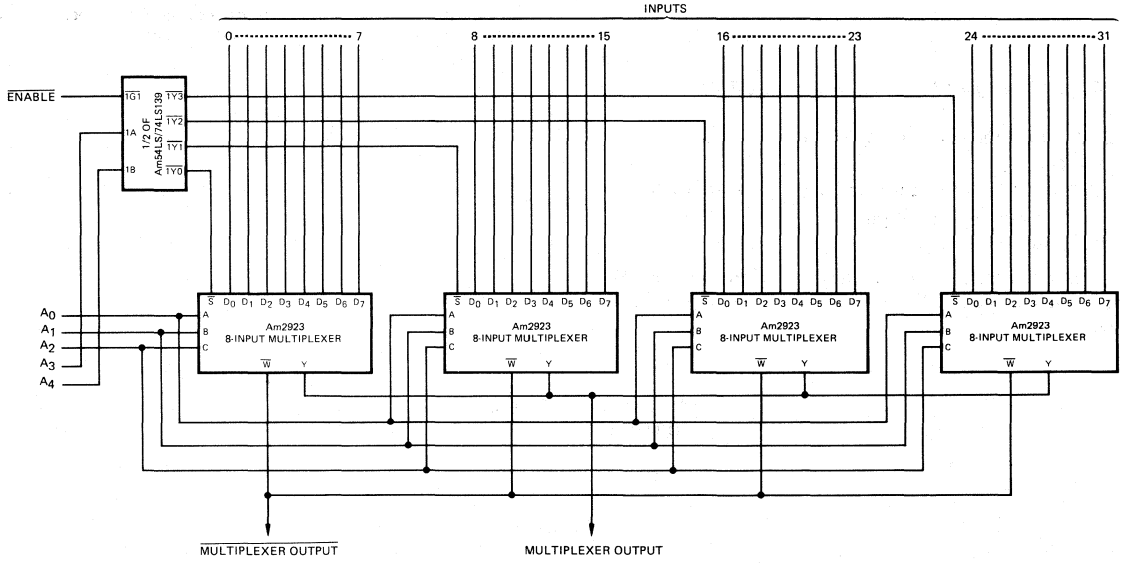
LOGIC FUNCTION GENERATION



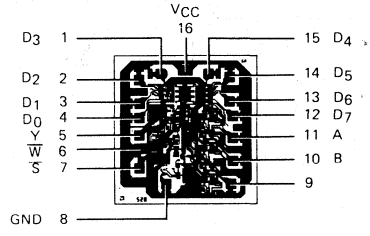
$$Z = \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D} + A\overline{C}D + AB + AC\overline{D} + BC\overline{D}$$

BLI-073

32-INPUT MULTIPLEXER



Metallization and Pad Layout



DIE SIZE: 0.064" X 0.067"

BLI-074

Am2924

3-Line to 8-Line Decoder/Demultiplexer

Distinctive Characteristics

Advanced Schottky technology
Inverting and non-inverting enable inputs

- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2924 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight $\overline{Y}$ outputs.

One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight $\overline{Y}$ outputs are HIGH regardless of the A, B and C select inputs.

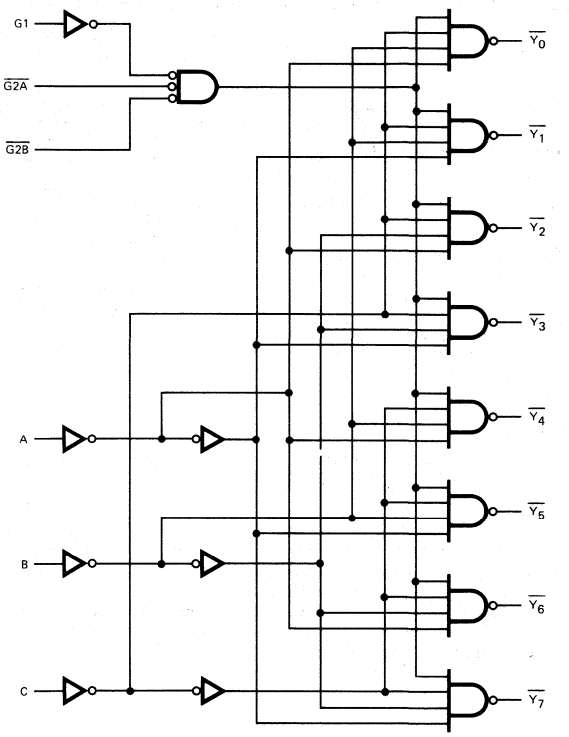
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2924PC	P-16-1	C	C-1
AM2924DC	D-16-1	C	C-1
AM2924DC-B	D-16-1	C	B-1
AM2924DM	D-16-1	M	C-3
AM2924DM-B	D-16-1	M	B-3
AM2924FM	F-16-1	M	C-3
AM2924FM-B	F-16-1	M	B-3
AM2924XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2924XM	Dice	M	

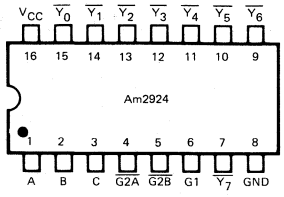
Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883 Class B.

LOGIC DIAGRAM



BLI-075

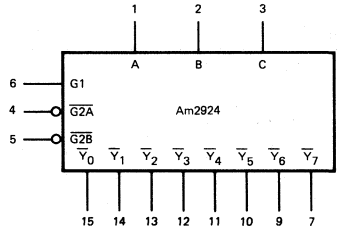
CONNECTION DIAGRAM
Top View



BLI-076

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



BLI-077

V_{CC} = Pin 16
GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +VCC max
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2924PC, DC, XC $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2924DM, FM, XM $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA $V_{IN} = V_{IH}$ or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			49	74	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs enabled and open.

Switching Characteristics ($T_A = +25°C$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Two Level Delay Select to Output	V_{CC} = 5V, C_L = 15pF, R_L = 280Ω		4.5	7	ns
t_{PHL}				7	10.5	
t_{PLH}	Three Level Delay Select to Output			7.5	12	ns
t_{PHL}				8	12	
t_{PLH}	$\overline{G2A}$ or $\overline{G2B}$ to Output			5	8	ns
t_{PHL}				7	11	
t_{PLH}	G1 to Output			7	11	ns
t_{PHL}				7	11	

FUNCTION TABLE

Inputs						Outputs							
Enable			Select										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Unit Load	Fan-out Output HIGH	Fan-out Output LOW
A	1	1	–	–
B	2	1	–	–
C	3	1	–	–
$\overline{G2A}$	4	1	–	–
$\overline{G2B}$	5	1	–	–
G1	6	1	–	–
$\overline{Y_7}$	7	–	20	10
GND	8	–	–	–
$\overline{Y_6}$	9	–	20	10
$\overline{Y_5}$	10	–	20	10
$\overline{Y_4}$	11	–	20	10
$\overline{Y_3}$	12	–	20	10
$\overline{Y_2}$	13	–	20	10
$\overline{Y_1}$	14	–	20	10
$\overline{Y_0}$	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

6

DEFINITION OF FUNCTIONAL TERMS:

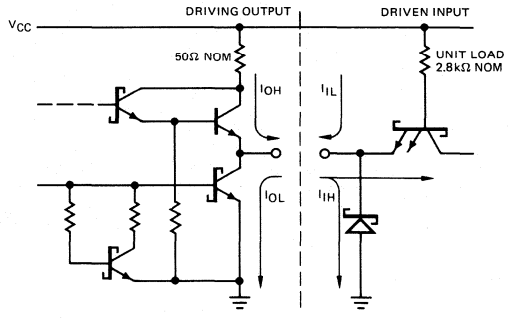
A, B, C Select. The three select inputs to the decoder.

G1 The active-HIGH enable input. A LOW on the G1 input forces all $\overline{Y}$ outputs HIGH regardless of any other inputs.

$\overline{G2A}$, $\overline{G2B}$ The active-LOW enable input. A HIGH on either the $\overline{G2A}$ or $\overline{G2B}$ input forces all $\overline{Y}$ outputs HIGH regardless of any other inputs.

$\overline{Y_0}$, $\overline{Y_1}$, $\overline{Y_2}$, $\overline{Y_3}$, $\overline{Y_4}$, $\overline{Y_5}$, $\overline{Y_6}$, $\overline{Y_7}$ The eight decoder outputs.

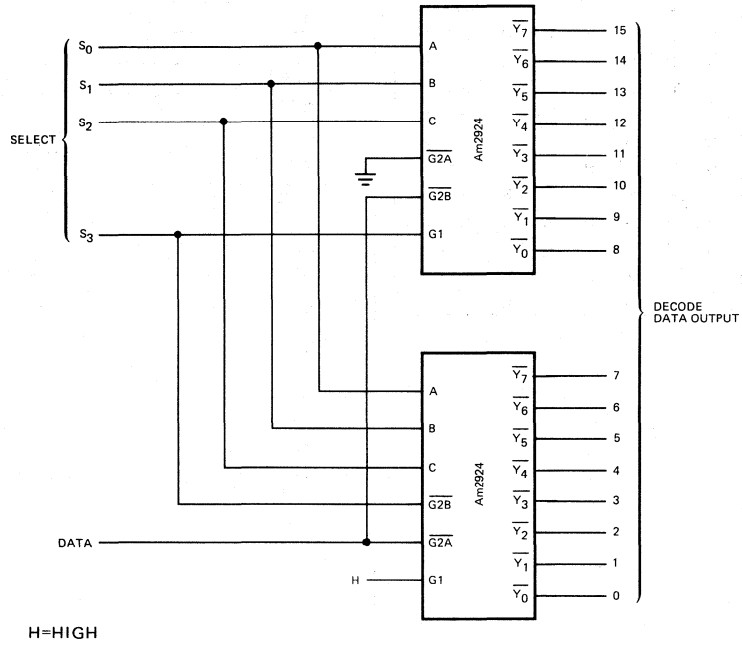
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI-078

APPLICATION

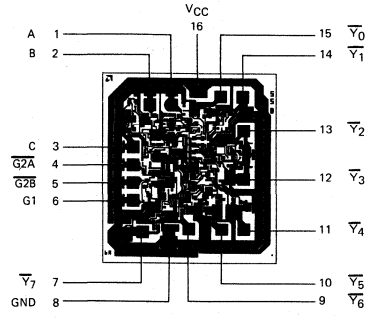


H=HIGH

ONE-OF-SIXTEEN DEMULTIPLEXER

BLI-079

Metallization and Pad Layout



DIE SIZE 0.065"X0.070"

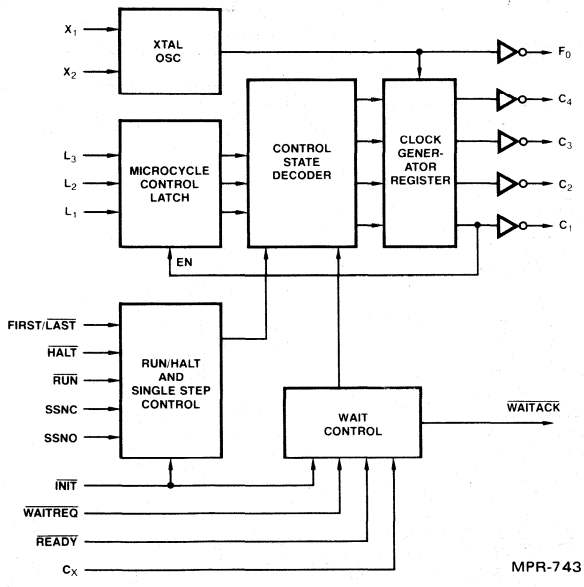
Am2925

Clock Generator and Microcycle Length Controller

DISTINCTIVE CHARACTERISTICS

- **Crystal controlled oscillator**
  Stable operation from 1MHz to over 31MHz
- **Four microcode controlled clock outputs**
  Allows clock cycle length control for 15–30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- **System controls for Run/Halt and Single Step**
  Switch debounced inputs provide flexible halt controls
- **Slim 0.3" 24-pin package**
  LSI complexity in minimum board area

BLOCK DIAGRAM



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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2925DC	D-24-Slim	C	C-1
AM2925DCB	D-24-Slim	C	B-1
AM2925DM	D-24-Slim	M	C-3
AM2925DMB	D-24-Slim	M	B-3
AM2925XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2925XM	Dice	M	

Notes:
1. D = Hermetic DIP. Number following letter is number of leads.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

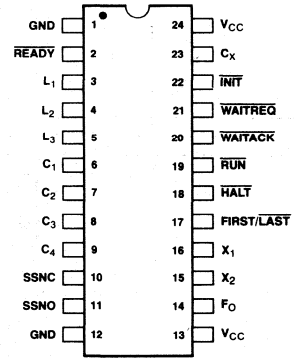
FUNCTIONAL DESCRIPTION

The Am2925 is a single-chip general purpose clock generator/driver. It is crystal controlled, and has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meet a variety of system speed requirements. The Am2925 generates four different simultaneous clock output waveforms tailored to meet the needs of Am2900 and other bipolar and MOS microprocessor based systems. One-of-eight cycle lengths may be generated under microprogram control using the Cycle Length inputs L_1, L_2, and L_3.

The Am2925 oscillator runs at frequencies to over 31MHz. A buffered oscillator output, F_0, is provided for external system timing in addition to the four microcode controlled clock outputs C_1, C_2, C_3 and C_4.

System control functions include Run, Halt, Single-Step, Initialize and Ready/Wait controls. In addition, the FIRST/LAST input determines where a halt occurs and the C_X input determines the end point timing of wait cycles. WAITACK indicates that the Am2925 is in a wait state.

CONNECTION DIAGRAM
Top View



New 24-pin slim (0.3") package

Note: Pin 1 is marked for orientation.

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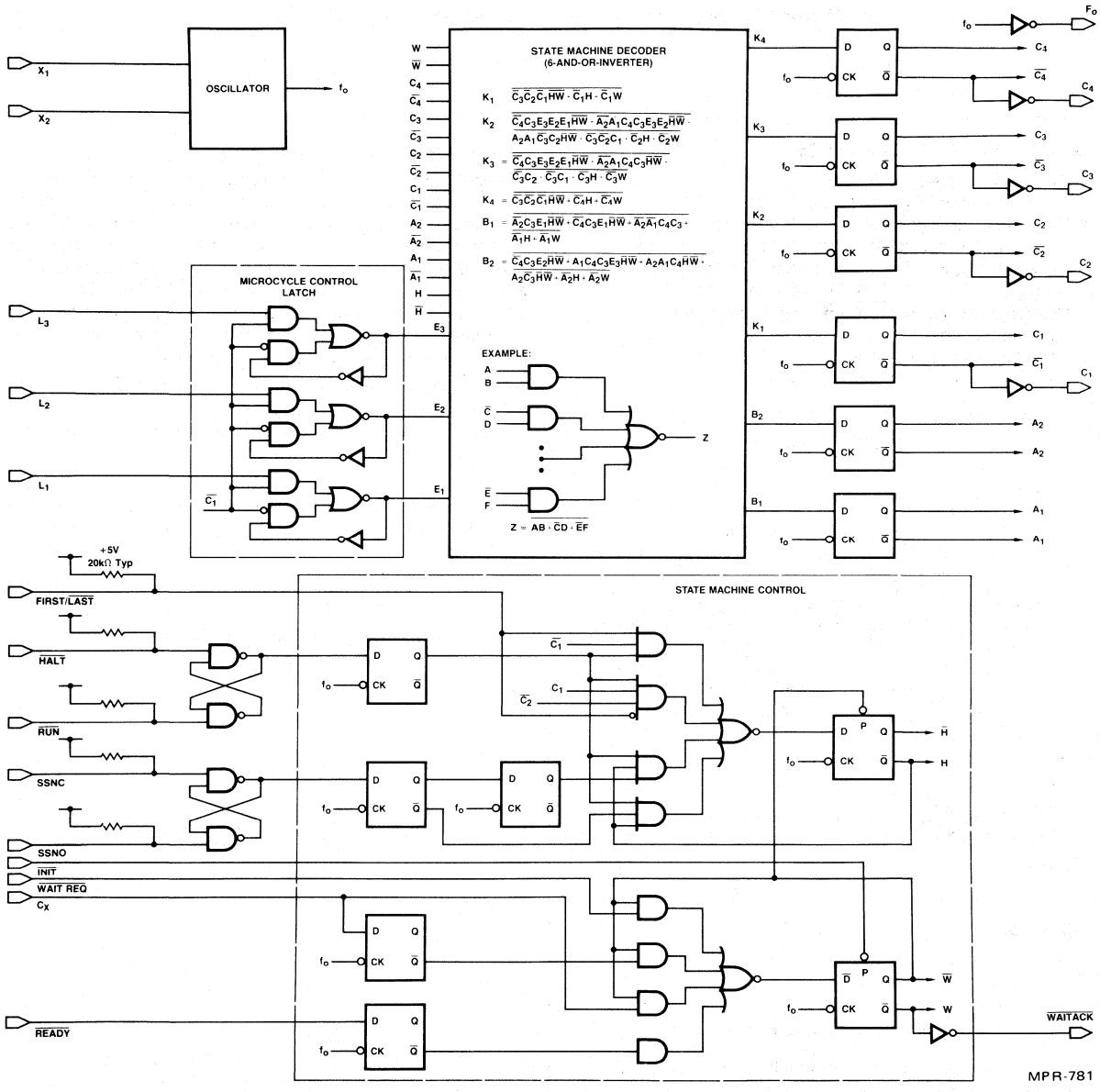
LOGIC DIAGRAM



DEFINITION OF FUNCTIONAL TERMS

C_1, C_2, C_3, C_4 System clock outputs. These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls, L_1, L_2 and L_3.

L_1, L_2, L_3 Clock cycle length control inputs. These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns A through H.

F_0 The buffered oscillator output. F_0 internally generates all of the timing edges for outputs C_1, C_2, C_3, C_4 and $\overline{WAITACK}$. F_0 rises just prior to all of the C_1, C_2, C_3, C_4 transitions.

$\overline{HALT}$ and $\overline{RUN}$ Debounced inputs to provide $\overline{HALT}$ control. These inputs determine whether the output clocks run or not. A LOW input on $\overline{HALT}$ ($\overline{RUN}$ = HIGH) will stop all clock outputs.

FIRST/$\overline{LAST}$ $\overline{HALT}$ time control input. A HIGH input in conjunction with a $\overline{HALT}$ command will cause a halt to occur when C_4 = LOW and $C_1 = C_2 = C_3$ = HIGH (see clock waveforms). A LOW input causes a $\overline{HALT}$ to occur when $C_1 = C_2 = C_3$ = LOW and C_4 = HIGH.

SSNO and SSNC Single Step control inputs. These debounced inputs allow system clock cycle single stepping while $\overline{HALT}$ is activated LOW.

DEFINITION OF FUNCTIONAL TERMS (Cont.)

$\overline{\text{WAITREQ}}$ — The Wait Request active LOW input. When LOW this input will cause the outputs to halt during the next oscillator cycle after the C_X input goes LOW.

C_X — Wait cycle control input. The clock outputs respond to a wait request one oscillator clock cycle after C_X goes LOW. C_X is normally tied to any one of C_1, C_2, C_3 or C_4.

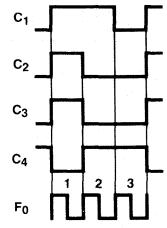
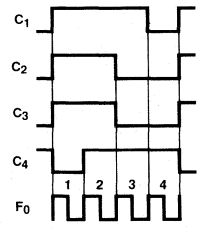
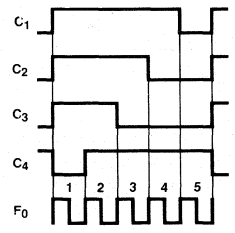
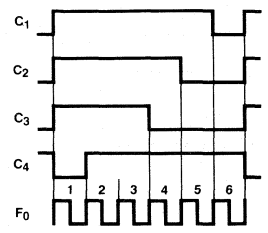
$\overline{\text{WAITACK}}$ — The Wait Acknowledge active LOW output. When LOW, this output indicates that all clock outputs are in the "WAIT" state.

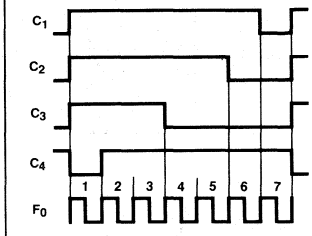
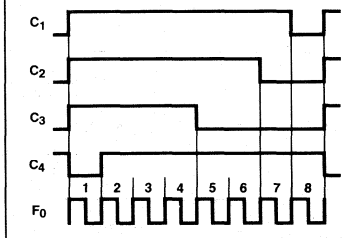
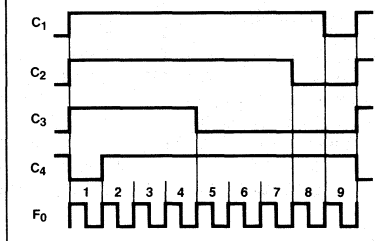
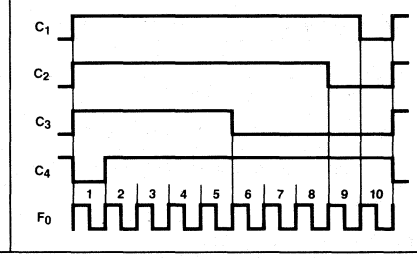
$\overline{\text{READY}}$ — The $\overline{\text{READY}}$ active LOW input is used to continue normal clock output patterns after a wait stage.

$\overline{\text{INIT}}$ — The Initialize active LOW input. This input is intended for use during power up initialization of the system. When LOW all clock outputs free run regardless of the state of the Halt, Single Step, Wait Request and Ready inputs.

X_1, X_2 — External crystal connections. X_1 can also be driven by a TTL frequency source.

Am2925 CLOCK WAVEFORMS

PATTERN INPUT CODE L_3 L_2 L_1	WAVEFORMS AND TIMING
F_3 LLL	
F_4 LLH	
F_5 HLH	
F_6 HHH	

PATTERN INPUT CODE L_3 L_2 L_1	WAVEFORMS AND TIMING
F_7 LHH	
F_8 LHL	
F_9 HHL	
F_{10} HLL	

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0 to 70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V MAX = 5.25V)
MIL	T_C = −55 to 125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA		2.5			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	$\overline{WAITACK}$ C_i	I_{OL} = 4.0mA			0.4	Volts
				I_{OL} = 8.0mA			0.45	
				I_{OL} = 12mA			0.5	
			F_0	I_{OL} = 16mA			0.5	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW level (Note 3)	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Note 3)	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3				−0.4	mA
			$\overline{WAITREQ}$, X_1 (See Figure 1)				−0.8	mA
			SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$				−1.0	mA
			C_X				−1.2	mA
			FIRST/$\overline{LAST}$				−1.5	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3				20	μA
			$\overline{WAITREQ}$				50	μA
			SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$				−500	μA
			C_X				70	μA
			FIRST/$\overline{LAST}$				−750	μA
			X_1 (See Figure 1)				500	μA
I_I	Input HIGH Current	V_{CC} = MAX	V_{IN} = 5.5V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3			100	μA
			V_{IN} = V_{CC}	SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$			100	μA
			V_{IN} = 5.5V	$\overline{WAITREQ}$, C_X			1.0	mA
			V_{IN} = V_{CC}	FIRST/$\overline{LAST}$			1.0	mA
			V_{IN} = 4.0V	X_1 (See Figure 1)			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX				85	120	mA

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Does not apply to X_1 and X_2.
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} varies with temperature and oscillation frequency as shown in Figure 2. The parameters specified (worst case) applies to f_0 = 0, +25°C, C_1 = C_2 = C_3 = LOW, C_4 = HIGH, X_1 = 2.4V, X_2 = open and F_0 = LOW. The variations shown in Figure 2 apply to typical values.

MAXIMUM RATINGS (Above which the useful life may be impaired)

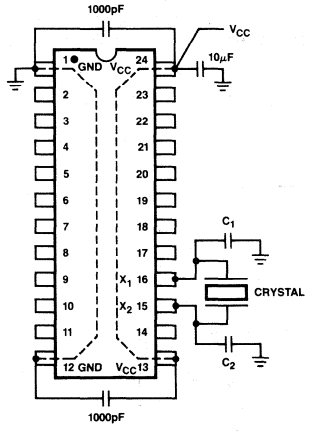
Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

	Parameters	Description	Min	Typ	Max	Units	Test Conditions
1	f_{MAX1}	F_0 Frequency (C_X Connected) (Note 6)	31			MHz	C_L = 15pF, R_L = 280Ω
2	f_{MAX2}	F_0 Frequency (C_X = HIGH)		42			
3	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)	0	3	5	ns	
4	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↑)	3	8	12	ns	
5	t_{SKEW}	C_1 (↓) to C_2 (↓)	0	0.5	2	ns	
6	t_{SKEW}	C_1 (↓) to C_3 (↓)	0	0.5	2	ns	
7	t_{SKEW}	C_1 (↓) to C_4 (↑) Opposite Transition	4	7	10	ns	
8	t_S	L_1, L_2, L_3 to C_1 (↓)	5			ns	
9	t_H	L_1, L_2, L_3 to C_1 (↓)	9			ns	
10	t_S	C_X to F_0 (↓) (Note 7)	20	17		ns	
11	t_H	C_X to F_0 (↓) (Note 7)	0	−10		ns	C_L = 50pF, R_L = 2.0kΩ
12	t_S	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)	20	17		ns	
13	t_H	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)	0	−10		ns	
14	t_S	$\overline{READY}$ to F_0 (↓) (Note 8)	20	17		ns	
15	t_H	$\overline{READY}$ to F_0 (↓) (Note 8)	0	−10		ns	
16	t_S	$\overline{RUN}$, $\overline{HALT}$ (↑) to F_0 (↓) (Notes 8, 9)	20	14		ns	
17	t_S	SSNC, SSNO to F_0 (↓) (Notes 8, 9)	20	14		ns	
18	t_S	FIRST/$\overline{LAST}$ to F_0 (↓) (Note 10)	25	17		ns	
19	t_{PWL}	$\overline{INIT}$ LOW Pulse Width	15	10		ns	
20	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$		16	23	ns	
21	t_{PLH}	Propagation Delay X_1 to F_0		16	20	ns	C_L = 15pF, R_L = 280Ω
22	t_{PHL}			15	19	ns	

TYPICAL EXTERNAL CONNECTIONS



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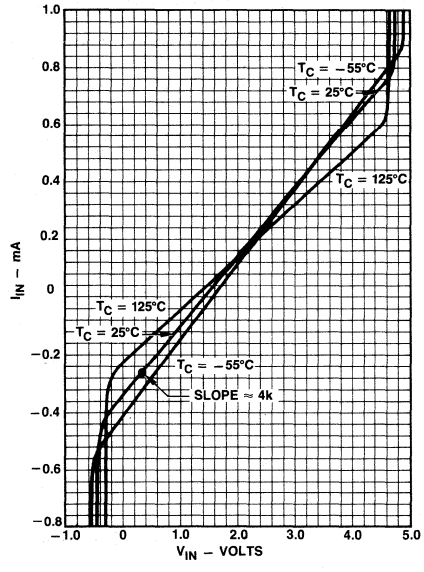
DESIGN CONSIDERATIONS

1. Oscillator external connections should be less than 1″ long – wirewrap is not recommended.
2. V_{CC} and GND connections should be less than ½″ long to power plane.
3. Supply decoupling includes both high frequency and bulk storage elements.
4. The same considerations apply for 3rd overtone configurations.



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X_1 is not a TTL input. It is a crystal connection to an inverting linear oscillator amplifier, and is specified primarily for test convenience.

Figure 1. Am2925 X_1 Input Characteristics (Typical, V_{CC} = 5.0V)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

	Parameters	Description	Am2925 COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% Min	Am2925 COM'L Max	Am2925 MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% Min	Am2925 MIL Max	Units	Test Conditions
1	f_{MAX1}	F_0 Frequency (C_X Corrected) (Note 6)	31		31		MHz	C_L = 15pF R_L = 280Ω
2	f_{MAX2}	F_0 Frequency (C_X = HIGH)						
3	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)		6		6	ns	
4	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↑)		13		14	ns	
5	t_{SKEW}	C_1 (↓) to C_2 (↓)		2		2	ns	
6	t_{SKEW}	C_1 (↓) to C_3 (↓)		2		2	ns	
7	t_{SKEW}	C_1 (↓) to C_4 (↑).Opposite Transition		11		11	ns	
8	t_S	L_1, L_2, L_3 to C_1 (↓)	6		7		ns	
9	t_H	L_1, L_2, L_3 to C_1 (↓)	11		11		ns	
10	t_S	C_X to F_0 (↓) (Note 7)	25		25		ns	
11	t_H	C_X to F_0 (↓) (Note 7)	0		0		ns	C_L = 50pF R_L = 2.0kΩ
12	t_S	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)	25		25		ns	
13	t_H	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)	0		0		ns	
14	t_S	$\overline{READY}$ to F_0 (↓) (Note 8)	25		25		ns	
15	t_H	$\overline{READY}$ to F_0 (↓) (Note 8)	0		0		ns	
16	t_S	$\overline{RUN}$, $\overline{HALT}$ (↑) to F_0 (↓) (Notes 8, 9)	25		25		ns	
17	t_S	SSNC, SSNO to F_0 (↓) (Notes 8, 9)	25		25		ns	
18	t_S	FIRST/$\overline{LAST}$ to F_0 (↓) (Note 10)	30		35		ns	
19	t_{PWL}	$\overline{INIT}$ LOW Pause Width	20		25		ns	
20	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$		25		27	ns	
21	t_{PLH}	Propagation Delay X_1 to F_0		27		30	ns	C_L = 15pF R_L = 280Ω
22	t_{PHL}			23		25	ns	

Notes:
6. The frequency guarantees apply with C_X connected to C_1, C_2, C_3, C_4 or HIGH. The C_X input load must be considered part of the 50pF/2.0kΩ clock output loading.
7. These set-up and hold times apply to the F_0 LOW-to-HIGH transition of the period in which C_X goes LOW.
8. These inputs are synchronized internally. Failure to meet t_s may cause a $1/F_0$ delay but will not cause incorrect operation.
9. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
10. FIRST/LAST is normally wired HIGH or LOW.

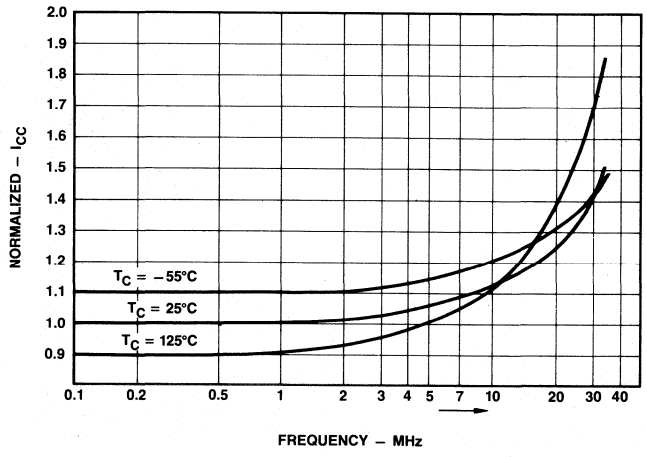

Figure 2. Am2925 I_{CC} Normalized vs Frequency (V_{CC} = 5.5V)

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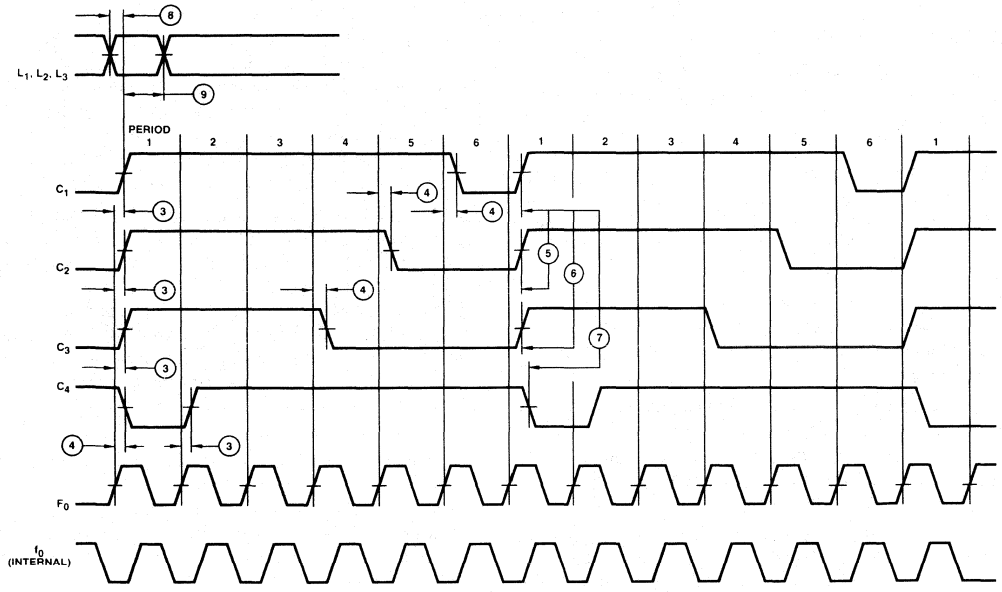
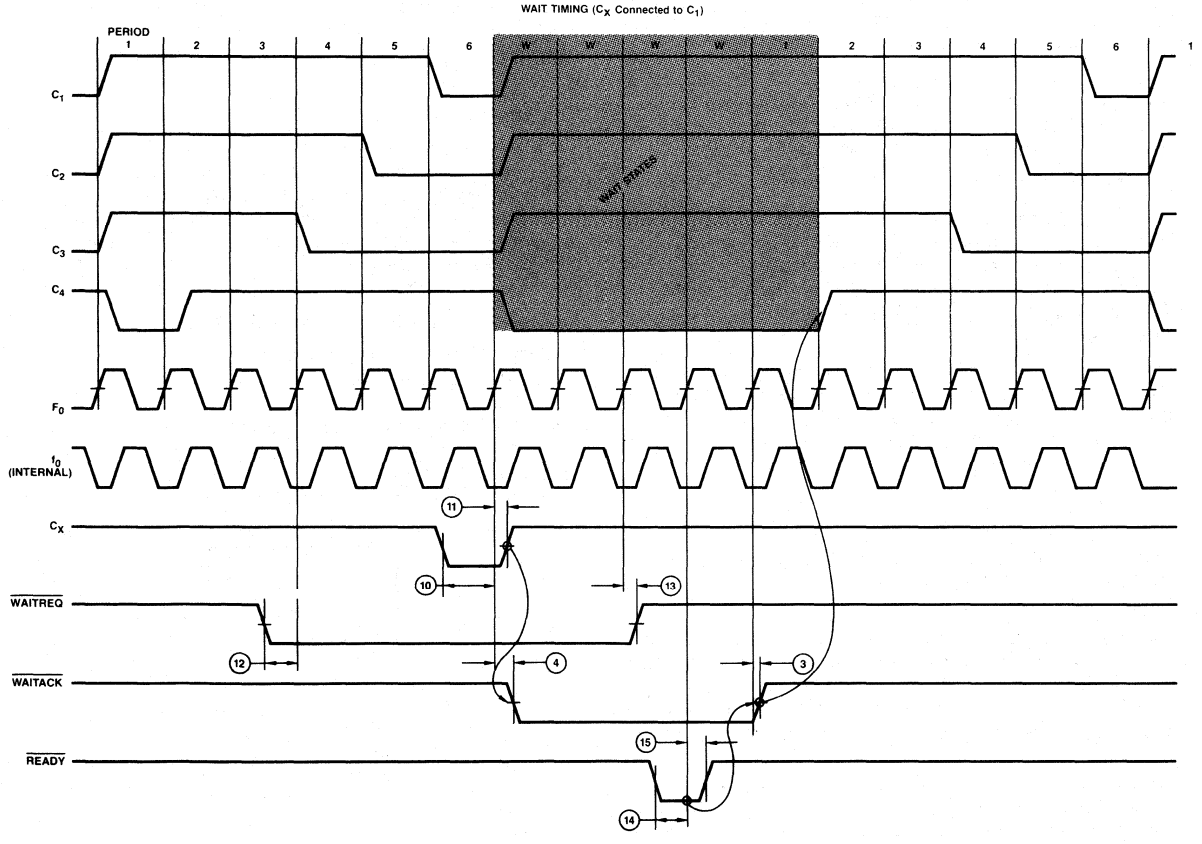
SWITCHING CHARACTERISTICS



NORMAL CYCLE WITHOUT WAIT STATES (Pattern F_6 Shown) MPR-786



WAIT TIMING (C_X Connected to C_1) MPR-787

Am2925 APPLICATIONS

DETAILED FUNCTIONAL DESCRIPTION

The Am2925 is a dynamically programmable general-purpose clock generator/driver. It can be logically separated into three parts. There is an oscillator, a state machine decoder and a state machine control section.

The oscillator is a linear inverting amplifier which with a minimum of external parts may be configured as a 1st harmonic* crystal oscillator, 3rd harmonic* crystal oscillator, L-C oscillator or used to buffer an external clock. the buffered, inverted output of this oscillator is availavble as F_0.

The state machine takes microcode information from the Microcycle Length "L" inputs L_1, L_2 and L_3 and counts the fundamental frequency of the internal oscillator, F_0, to create the clock outputs, C_1, C_2, C_3 and C_4.

The clock outputs have a characteristic wave shape relationship for each microcycle length. For example, C_1 is always LOW only on the last F_0 clock period of a microcycle and C_4 is always LOW on the first. C_3 has an approximately 50% duty cycle, and C_2 is HIGH for all but the last two periods.

The current state of the machine is contained in a register, part of which is the Clock Generator Register. C_1, C_2, C_3 and C_4 are the outputs of this register. These outputs and the outputs of the Microcycle Control Latch are fed into a set of combinatorial logic to generate the next state. On each falling edge of the internal clock the next state is entered into the current state register. The Microcycle Control Latch is latched when C_1 is HIGH. This means that it will be loaded during the last state of each microcycle, ($C_1 = C_2 = C_3$ = LOW, C_4 = HIGH). This internal latch selects one of eight possible microcycle lengths, F_3 to F_{10}.

The state machine control logic, which determines the mode of operation of the state machine, is intended to be connected to a front panel. There are four basic modes of operation of the Am2925 comprised of Run, Halt, Wait and Single Step.

SYSTEM TIMING

In the typical computer, the time required to execute different instructions varies. However, the time allotted to each instruction is the time that it takes to execute the longest instruction. The Am2925 allows the user to dynamically vary the time allotted for each instruction, thereby allowing the user to realize a higher throughput.

This application note will cover several aspects of the Am2925. The first topic to be covered is the oscillator section which is responsible for providing the basis of all system timing. Second will be how to operate the Am2925; last will be an example of an Am2925 in a 16-bit microprogrammed machine.

OSCILLATOR

The Am2925 contains an inverting, linear amplifier which is intended to form the basis of a crystal oscillator. In designing this oscillator it is necessary to consider several factors related to the application.

The first consideration is the desired frequency accuracy. This may be subdivided into several areas. An oscillator is considered stable if it is insensitive to variations in temperature and supply voltage, and if it is unaffected by individual component changes and aging. The design of the Am2925 is such that the degree to which these goals are met is determined primarily by the choice of external components. Various types of crystals are available and the manufacturers' literature should be consulted to determine the appropriate type. For good temperature stability, zero temperature coefficient capacitors should be used (Type NPO). For extreme temperature stability, an oven must be used or some other form of temperature compensation applied.

Absolute frequency accuracy must also be considered. The resonant frequency varies with load capacitance. It is therefore important to match the load specified by the crystal manufacturer for a standard crystal (usually 32pF), or to specify the load when ordering a special crystal. It should then be possible to determine from the crystal characteristics the load tolerance to maintain a given accuracy. If the "set-on" error due to load tolerance is unacceptable, a trimmer capacitor should be incorporated for fine adjustment.

The mechanism by which a crystal resonates is electromechanical. This resonance occurs at a fundamental frequency (1st harmonic) and at all odd harmonics of this frequency (even harmonic resonance is not mechanically possible). Unless otherwise constrained crystal oscillators operate at their fundamental frequency. However, crystals are not generally available with fundamental frequencies above 20-25MHz. At higher frequencies, an overtone oscillator must be used. In this case, the crystal is designed to oscillate efficiently at one of its odd harmonic frequencies and additional components are included in the oscillator circuit to prevent it oscillating at lower harmonics.

Where a high degree of accuracy or stability is not required, the amplifier may be configured as an L-C oscillator. It may also be driven from an external clock source if operation is required in synchronism with that source.

1st Harmonic (Fundamental) Oscillator

The circuit of a typical 1st harmonic oscillator is shown in Figure 1. The crystal load is comprised of the two 68pF capacitors in series. This 34pF approximates the standard 32pF crystal load. If a closer match is required then one of the capacitors should be replaced with a parallel combination of a fixed capacitor and a trimmer. The nominal value of the combination should be 60pF to provide proper crystal loading.

A typical crystal specification for use in this circuit is:

Frequency Range: 5–20MHz
Resonance: Parallel Mode
Load: 32pF
Stability: .01% or to match systems requirements
Case: H-17 – for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change over temp

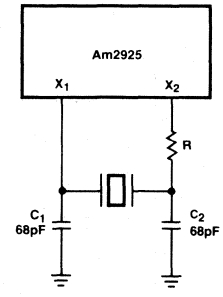


Figure 1. Connections for 5-20 MHz MPR-792

*It is understood that the terms "fundamental mode" and "3rd overtone" are generally regarded as more technically correct, but "1st harmonic" and "3rd harmonic" are used here because of their more generally accepted usage

It is good practice to ground the case of the crystal to eliminate stray pick-up and keep all connections as short as possible.

Note: At fundamental frequencies below 5MHz it is possible for the oscillator to operate at the 3rd harmonic. To prevent this a resistor should be added in series with the X_2 pin as shown in the circuit diagram.

The resistor value should match the impedance of C_1:

$$R = X_{C_2} = \frac{1}{2\pi f C_2}$$

3rd Harmonic Oscillator

At frequencies greater than 20MHz the crystal must be operated at its 3rd harmonic. A typical circuit is shown in Figure 2. Two additional components are included; an inductor, L_1, and a capacitor, C_3. The purpose of the capacitor is to block the d.c. path through the inductor and thereby maintain the correct amplifier bias. C_3 should be large ($\geq$1000pF).

The inductor forms a parallel tuned circuit with C_1. This circuit has its resonance set between the 1st and 3rd harmonics of the crystal and is used to prevent the oscillator operating at the 1st harmonic. In the 1st harmonic oscillator (Figure 1), the crystal appears as an inductor and forms a π-network with the two capacitors, thus providing the necessary phase shift for oscillation. In the 3rd harmonic oscillator, L_1 and C_1 are chosen such that at the 3rd harmonic the impedance of circuit is equivalent to that of the capacitor C_1 in the 1st harmonic oscillator, (Figure 3b). Thus, the same π-network is formed (Figure 3c) and oscillation is possible. At the 1st harmonic the tuned circuit appears as an inductor (Figure 3a), the π-network is not formed and oscillation is not possible.

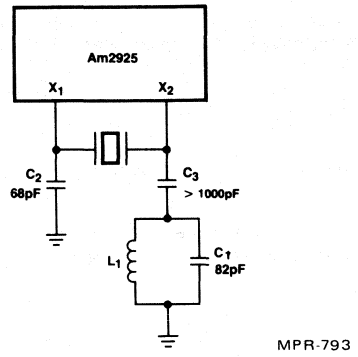
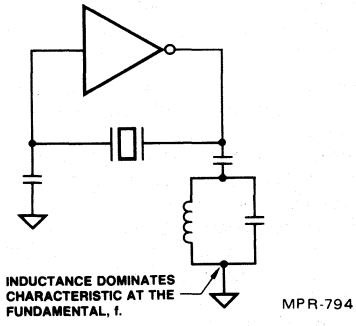


Figure 2. Connections for 20 MHz and Above

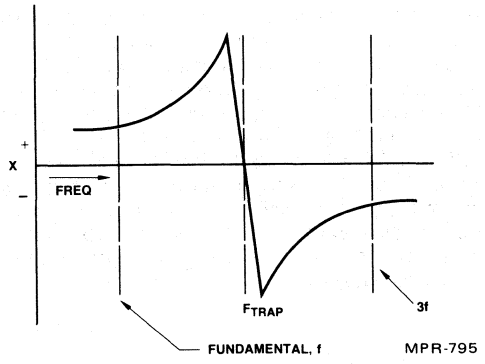
The following specification is typical for a crystal to be used in a 3rd harmonic oscillator.

Frequency Range: 20MHz and above
Resonance: Parallel Mode
Load: 32pF
Stability: .01% or to match systems requirements
Case: H-17 – for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change temp

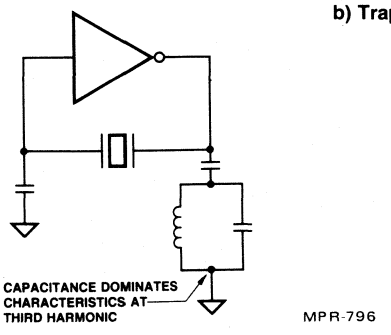
Again it is good practice to ground the crystal case and keep connections short.



a) Fundamental Equivalent



b) Trap Impedance



c) 3rd Harmonic Equivalent

Figure 3. Forcing Third Harmonic Oscillation

Design Procedure

(1) Assume C_1 = 82pF and C_2 = 68pF (this gives a sensible inductor value). L_1 is calculated according to the formula

$$L_1 = \frac{1151}{f_o^2}$$

f_o = Operating frequency in MHz
L_1 in μH

This sets the resonant frequency of the L-C combination at 0.52 f_o.

(2) Select the closest standard value inductor for L_1. Using this value calculate C_1 such that the resulting crystal load at the 3rd harmonic is 32pF.

$$C_1 = 60 + \frac{25330}{L_1 \cdot f_o^2} \qquad C_1 \text{ in pF.}$$

Choose the closest standard capacitor value to this.

Using standard values both the resonant frequency of the L-C circuit (f_r) and the crystal load are non-optimal. This will cause a slight error in the oscillating frequency. If this is not permissible C_1 may be a fixed capacitor in parallel with a trimmer such that the range of adjustment includes the calculated value for C_1. This is then set to give the desired frequency. In either case the approximate inductor value will cause the resonant frequency to the L-C circuit to change. This frequency, f_r, may be computed and should remain approximately midway between the 1st and 3rd harmonic.

$$f_r = \frac{159}{\sqrt{L_1 \cdot C_1}}$$

f_r in MHz
L_1 in μH
C_1 in pF

L-C Oscillator

The Am2925 can be operated as an L-C tuned oscillator (Figure 4) and will perform as a stable oscillator within the restrictions of the chosen frequency determining components, i.e., (inductor and capacitors). The circuit chosen is a classical π-network with DC loop isolation. The Am2925 oscillator is a DC biased linear amplifier. This DC bias is necessary and therefore C_3 is included to block the DC path through the inductor. If a variable slug tuned inductor is used a moderate range of frequency adjustment tuneability (approximately 2:1) can be achieved. The range can be enhanced by switching the two resonant capacitors (C_1, C_2) to larger or smaller values. The specific frequency of operation can be determined by the formula

$$f = \frac{1}{2\pi\sqrt{L\,C}}$$

(where C is C_1 and C_2 in series).

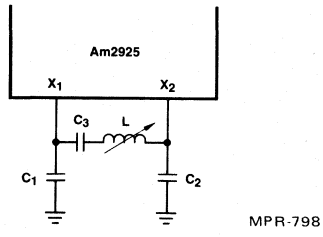


Figure 4. L-C Tuned Oscillator

External Clock Drive

The Am2925 can be driven from an external clock source at a signal level of 1.0V P-P or greater. This is accomplished by reducing the gain of the amplifier, and AC coupling the input signal (Figure 5). The gain is reduced by feeding the amplifier output back to the input through a 4.7kΩ resistor. AC coupling is provided by a 0.01μF capacitor. The controlled gain minimizes ringing caused by the fast rising edges of the driver.

The AC coupling maintains oscillator output symmetry by preserving oscillator DC bias levels. X_1 can be driven directly by TTL levels meeting the DC input requirements.

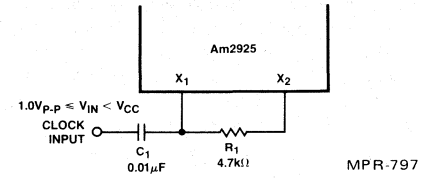


Figure 5. External Clock Drive

Am2925 Control Inputs

The control inputs fall into two categories, microcycle length control and clock control. Microcycle length control is provided via the "L" inputs which is intended to be connected to the microprogram memory. The "L" inputs are used to select one of eight cycle lengths ranging from three oscillator cycles for pattern F_3 to ten oscillator cycles for pattern F_{10}. This information is always loaded at the end of the microcycle into the Microcycle Control Latch. The microcycle latch performs the function of a pipeline register for the microcycle length microcode bits. Therefore, the cycle length goes in the same microword as the instruction that it is associated with.

The clock control inputs are used to synchronize the microprogram machine with the external world and I/O devices. Inputs like $\overline{\text{RUN}}$, $\overline{\text{HALT}}$, SSNO and SSNC, which start and stop execution, are meant to be connected to switches on the front panel of the microprogrammed machine (see Figure 6). These inputs have internal pull-up resistors and are connected to an R-S flip-flop in order to provide switch debouncing. The FIRST/$\overline{\text{LAST}}$ input is used to determine at what point of the microcycle the Am2925 will halt when $\overline{\text{HALT}}$ or a SINGLE STEP is initiated. In most applications the user wires this input HIGH or LOW depending on his design.

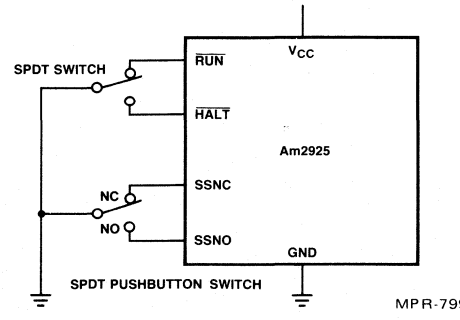


Figure 6. Switch Connection for $\overline{\text{RUN}}$/$\overline{\text{HALT}}$ and Single Step

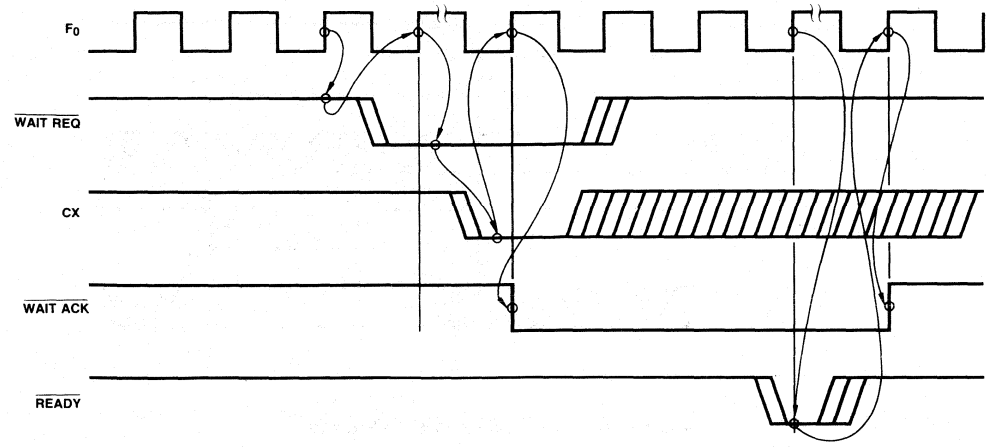


Figure 7. Am2925 $\overline{\text{WAIT/READY}}$ Timing MPR-800

When $\overline{\text{HALT}}$ is held low ($\overline{\text{RUN}}$ = HIGH) the state machine will start the halt mode on the last (C_1 = LOW) or the first (C_4 = LOW) state of the microcycle as determined by the FIRST/$\overline{\text{LAST}}$ input. When $\overline{\text{RUN}}$ goes low ($\overline{\text{HALT}}$ = HIGH) the state machine will resume the run mode.

The $\overline{\text{WAITREQ}}$, C_X, $\overline{\text{READY}}$ and $\overline{\text{WAITACK}}$ signals are used to synchronize other parts of a computer system (memory, I/O devices) to the CPU by dynamically stretching the microcycle. For example, the CPU may access a slow peripheral that requires the data remain on the data bus for several microseconds in which case the peripheral pulls the $\overline{\text{WAITREQ}}$ line LOW. The C_X input lets the designer specify when the $\overline{\text{WAITREQ}}$ line is sampled in the microcycle. This has a direct impact on how much time the peripheral has to respond in order to request a wait cycle (see Figure 7). The $\overline{\text{READY}}$ line is used by the peripheral to signal when it is ready to resume execution of the rest of the microcycle. The $\overline{\text{WAITACK}}$ line goes LOW on the next oscillator cycle after the C_X input goes LOW and remains LOW until the second oscillator cycle after $\overline{\text{READY}}$ goes LOW.

The SSNO and SSNC inputs are used to initiate the SINGLE STEP mode. These debounced inputs allow a single microcycle to occur while in the halt mode. SSNO (normally open) and SSNC (normally closed) are intended to be connected to a momentary SPDT switch. After SSNO has been low for one clock edge, the state machine will change to the run mode. The microcycle will end on the first or last state of the microcycle depending on the state of the FIRST/$\overline{\text{LAST}}$.

AC Timing Signal References

Set-up and hold times in registers and latches are measured relative to the clock signals that drives them. In the Am2925, the crystal oscillator provides a free running clock signal that drives all the registers on the devices. This clock is provided for the user through the buffered output of F_0. Therefore, F_0 is used as the reference for set-up, hold and clock to output times. However for the Microcontrol Latch, the set-up and hold times are referenced to the C_1 output which is the buffered version of the latch enable. This reference is appropriate for the Microcontrol Latch because in a typical application this latch is considered part of the pipeline register which is also driven by one of the "C" outputs.

Clock Outputs

There are four clock outputs provided for the user which have different duty cycles. The user must make a decision as to which one best fits his purposes. For example, in a three address architecture, with the Am2903 (Figure 8), the C_3 clock (approximately 50% duty cycle) could be used to drive the clock input while C_2 (always low last two oscillator cycles) drives Instruction Enable. This guarantees, for microcycle lengths greater than four, that the internal RAM data latches of the Am2903 are closed and the destination address is multiplexed onto the B address bus before the RAM begins the Write cycle (Figure 9).

16-BIT MACHINE WITH Am2925

The block diagram in Figure 10 shows a 16-bit microprogrammed machine which uses an Am2925 to generate system timing. The design decisions include oscillator frequency and clock pattern selections.

Selecting the Crystal

In order to pick the oscillator frequency, a detailed timing analysis of the machine must be done in order to determine the execution length of every operation to be performed. For each operation there will be several delay paths, which usually include the ALU and the microprogram control.

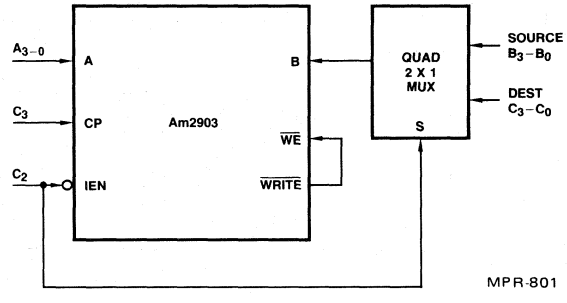


Figure 8. Am2903 Three Address Architecture

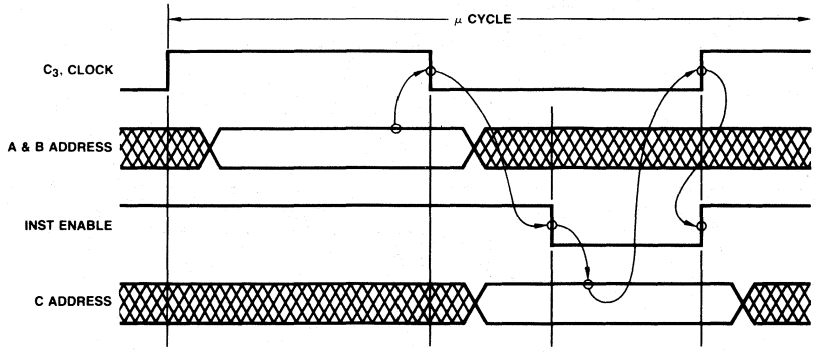


Figure 9. Am2903 Three Address Operation MPR-802

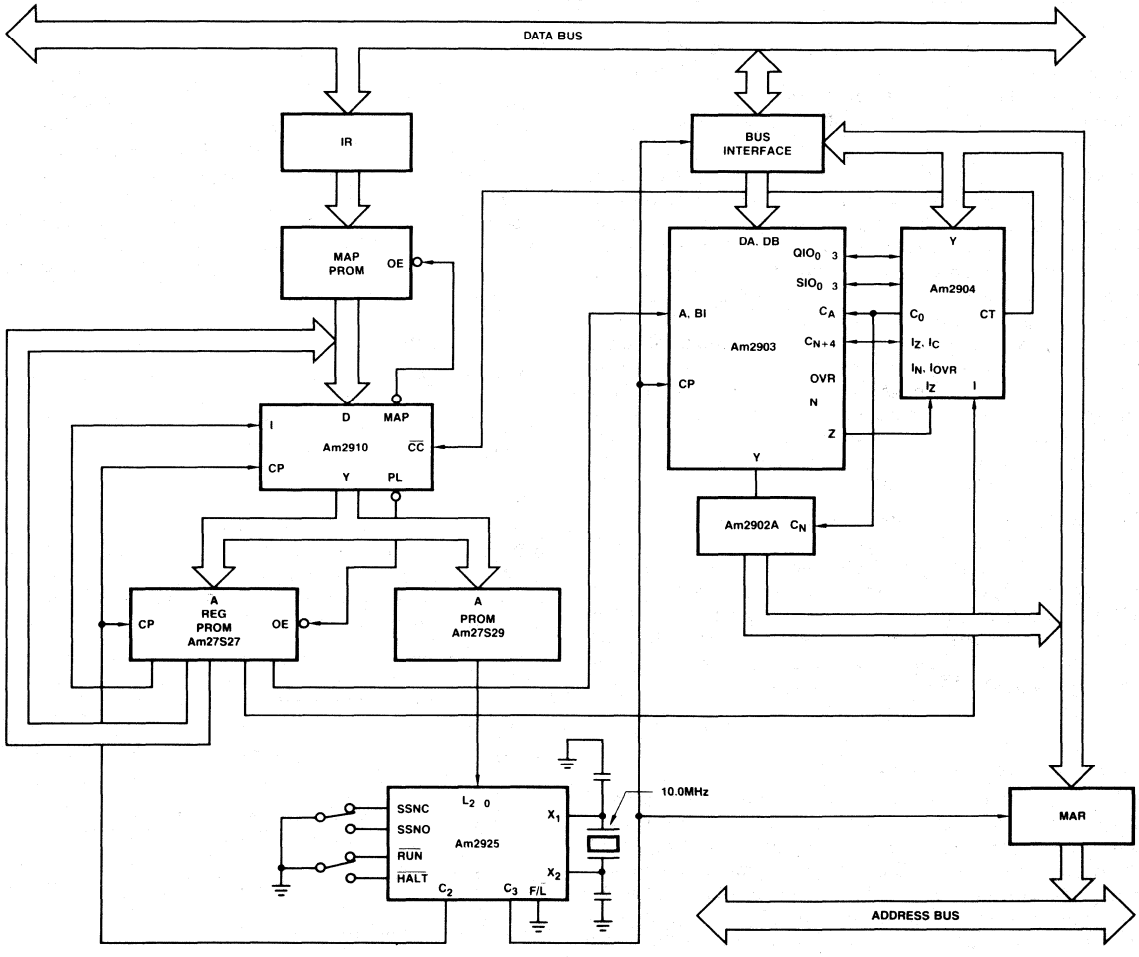


Figure 10. 16-Bit Microprogrammed Machine MPR-803

Figure 11 is an example of two of these paths. PATH 1 is a path through the Am2910 (Figure 10) for a microprogram Conditional Jump Subroutine. PATH 2 is a data flow path through the Am2903 for an Add instruction. Therefore, if the operation were an Add with a Conditional Jump Subroutine the maximum delay would be 196ns. If there were a Program Control Unit also, then delays through it would have to be considered.

After the execution times all of the instruction types have been calculated, the oscillator frequency can be selected. It is desirable to minimize the difference between the most commonly used instructions and multiples of the oscillator period. In this way the most efficient use can be made of the variable microcycle scheme.

For example, in the hypothetical machine in Figure 10 there are five instruction types (most machines will have more). Figure 12 is a table which lists each instruction type, corresponding execution time, and anticipated percentage of the typical instruction stream for each instruction. Several possible frequencies are shown which contain the next highest multiple of the corresponding oscillator period for each instruction. 20MHz is the best choice because it comes closest to matching instructions A and C which compose 90% of the typical instruction stream.

In this example, 20MHz was chosen. At 20MHz there is a choice between fundamental or overtone crystals. Fundamental frequency crystals are commonly available up to 25MHz and 3rd harmonic crystals are available above 17MHz. A fundamental crystal was selected for the example machine because the component count for the oscillator design is lower than for the overtone design. However, if it had turned out that 30MHz was a better choice then overtone operation would be chosen since fundamental crystals above 25MHz are not generally available.

Fixed Bandwidth Buses

For those designs that require a data bus with fixed bandwidth and fixed time slots for each memory access, the designer should consider using cycle lengths which are a multiple of the shortest cycle length, i.e., cycle lengths 3, 6 and 9 or cycle lengths 4 and 8. The design could further require that the bus be accessed only during the shortest cycle length. Therefore, by using multiple cycle lengths it can be predicted when the CPU will access the bus and for how long, thereby maintaining the fixed bandwidth.

Performance Comparison

Estimated performance can be calculated directly from Figure 12. For a fixed microcycle machine the longest instruction execution time would have to be used for all instructions, yielding an average instruction time of 228ns. With a variable microcycle machine the average instruction time is the sum of the products for each instruction, of the percentage of the instruction stream and the next highest multiple. The average instruction for the example machine with a 20MHz crystal is:

$$(0.6 \times 150 + .08 \times 200 + .3 + 200 + .01 \times 200 + .01 + 250) = 170.5\text{ns}$$

This represents a 25% increase in system performance without requiring any other system speed-ups and without requiring faster devices.

Device No.	Device Path	Path 1	Path 2
Am27S27	CP – Q	27	27
Am2904	INST – CT	58	–
Am2903	I/AB – GP	–	81
Am2910	CC – Y	43	–
Am2902A	GP – CN + Z	–	7
Am27S27	TS	55	–
Am2903	CN – Z	–	64
Am2904	TSZ	–	17
Total	ns	183	196

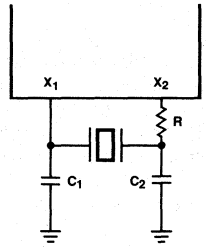
Figure 11. Delay Path Totals for an Add and a Conditional Jump Subroutine

Instruction Type	A	B	C	D	E	Unit
Execution Time	143	180	184	200	228	ns
Percentage of Instruction Stream	60%	8%	30%	1%	1%	%
Closest Multiple Oscillator Period						
20MHz P = 50	150 (3P)	200 (4P)	200 (4P)	200 (4P)	250 (5P)	ns
25MHz P = 40	160 (4P)	200 (5P)	200 (5P)	200 (5P)	240 (6P)	ns
30MHz P = 33	167 (5P)	200 (6P)	200 (6P)	200 (6P)	233 (7P)	ns
33MHz P = 30	150 (5P)	180 (6P)	210 (7P)	210 (7P)	240 (8P)	ns

Figure 12. Instruction Time Analysis

Am2925 OSCILLATOR APPLICATIONS

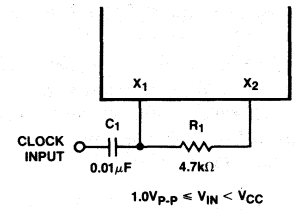
EXTERNAL COMPONENT CALCULATIONS SUMMARY



R = 0Ω for 6-20 MHz

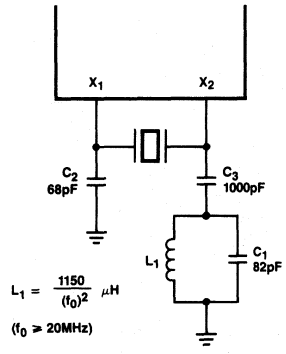
$R = X_{C_2} = \frac{1}{2\pi f C_2}$ for 1-6 MHz

FUNDAMENTAL OSCILLATOR MPR-788



$1.0V_{P-P} \leq V_{IN} < V_{CC}$

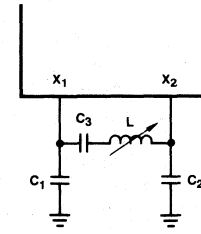
EXTERNAL CLOCK DRIVE MPR-789



$L_1 = \frac{1150}{(f_0)^2}\ \mu H$

($f_0 \geq 20MHz$)

3rd HARMONIC OSCILLATOR MPR-790



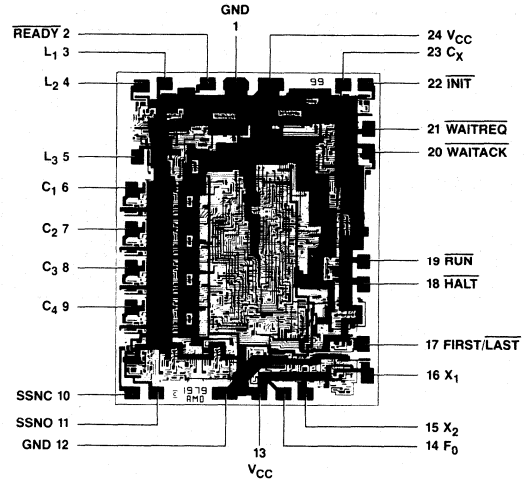
$f_0 = \frac{1}{2\pi\sqrt{2LC}}$

$C_1 = C_2 = C$

$X_{C_3} \ll X_L$

L-C OSCILLATOR MPR-791

METALLIZATION AND PAD LAYOUT



DIE SIZE .097" X .122"

Am2926 • Am2929

Schottky Three-State Quad Bus Driver/Receiver

Distinctive Characteristics

- Advanced Schottky technology
- 48mA driver sink current
- 3-state outputs on driver and receiver
- PNP inputs
- Am2926 has inverting outputs
- Am2929 has non-inverting outputs
- Driver propagation delay – 14ns max for Am2926; 17ns max for Am2929
- Receiver propagation delay – 14ns max for Am2926; 17ns max for Am2929
- 100% reliability assurance testing in compliance with MIL-STD-883

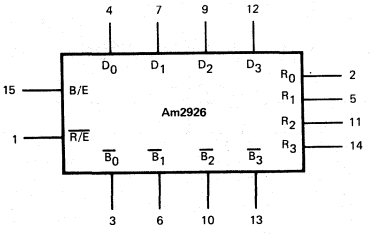
FUNCTIONAL DESCRIPTION

The Am2926 and Am2929 are high speed bus transceivers consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

A HIGH on the receiver enable ($\overline{R/E}$) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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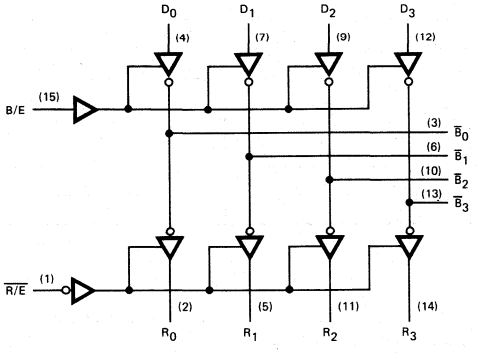
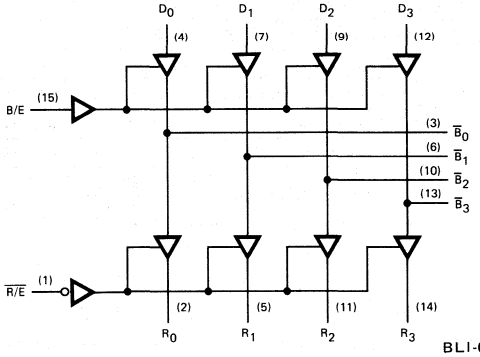
LOGIC DIAGRAMS

Am2926
Inverting Output (3-State)

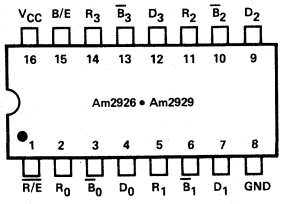


Am2929
Non-Inverting Output (3-State)



BLI-080

CONNECTION DIAGRAM
Top View



BLI-081

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5
DC Output Current, Into Outputs (Receiver)	30mA
DC Output Current, Into Outputs (BUS)	80mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am2926PC, DC, XC Am2929PC, DC, XC T_A = 0°C to +75°C (COM'L) MIN. = 4.75 V MAX. = 5.25 V

Am2929DM, XM Am2926DM, XM T_A = −55°C to +125°C (MIL) MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
Driver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			−200	μA
I_{IL}	Low Level Input Current (Disabled)	V_{IN} = 0.4 V			−25	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)	V_{IN} = V_{CC} MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 48mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = −10mA, V_{CC} = V_{CC} MIN. (Note 6)	2.4			Volts
I_{OS}	Short Circuit Output Current	V_{OUT} = 0V, V_{CC} = V_{CC} MAX. (Note 4)	−50		−150	mA
Receiver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			−200	μA
I_{IH}	High Level Input Current (R_E)	V_{IN} = V_{CC} MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 20mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = −100μA, V_{CC} = 5.0 V	3.5			Volts
		I_{OUT} = −2.0mA (Note 6)	2.4			
I_{OS}	Short Circuit Output Current	V_{OUT} = 0V, V_{CC} = V_{CC} MAX.	−30		−75	mA
Both Driver and Receiver						
V_{TL}	Low Level Input Threshold Voltage		0.85			Volts
V_{TH}	High Level Input Threshold Voltage				2.0	Volts
I_O	Low Level Output Off Leakage Current	V_{OUT} = 0.5 V			−100	μA
	High Level Output Off Leakage Current	V_{OUT} = 2.4 V			100	μA
V_I	Input Clamp Voltage	I_{IN} = −12mA			−1.0	Volts
P_{WR}/ I_{CC}	Power/Current Consumption — Am2926	V_{CC} = V_{CC} MAX.			457/87	mW/mA
	Power/Current Consumption — Am2929	V_{CC} = V_{CC} MAX.			578/110	

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Test Conditions	Am2926 Min.	Am2926 Typ.	Am2926 Max.	Am2929 Min.	Am2929 Typ.	Am2929 Max.	Units
t_{PLH}	Driver Input to Bus	Figure 1		10	14		13	17	ns
t_{PHL}				10	14		13	17	
t_{PLH}	Bus to Receiver Output	Figure 2		9.0	14		12	17	ns
t_{PHL}				6.0	14		9.0	17	
t_{ZL}	Driver Enable to Bus	Figure 3		19	25		21	28	ns
t_{LZ}				15	20		18	23	
t_{ZL}	Receiver Enable to Receiver Output	Figure 4		15	20		18	23	ns
t_{LZ}				10	15		13	18	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Output sink current is supplied through a resistor to V_{CC}.
6. Measurements apply to each output and the associated data input independently.

DEFINITION OF FUNCTIONAL TERMS

D_0, D_1, D_2, D_3 The four driver inputs.

$\overline{B_0}, \overline{B_1}, \overline{B_2}, \overline{B_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

B/E Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

$\overline{R/E}$ Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	LOW Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{R/E}$	1	1/8	–	–
R_0	2	–	50	10
$\overline{B_0}$	3	1/16	250	25
D_0	4	1/8	–	–
R_1	5	–	50	10
$\overline{B_1}$	6	1/16	250	25
D_1	7	1/8	–	–
GND	8	–	–	–
D_2	9	1/8	–	–
$\overline{B_2}$	10	1/16	250	25
R_2	11	–	50	10
D_3	12	1/8	–	–
$\overline{B_3}$	13	1/16	250	25
R_3	14	–	50	10
B/E	15	1/8	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as −1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

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DRIVER FUNCTION TABLE

INPUTS		Am2926 OUTPUT	Am2929 OUTPUT
B/E	D_i	$\overline{B_i}$	$\overline{B_i}$
L	X	Z	Z
H	L	H	L
H	H	L	H

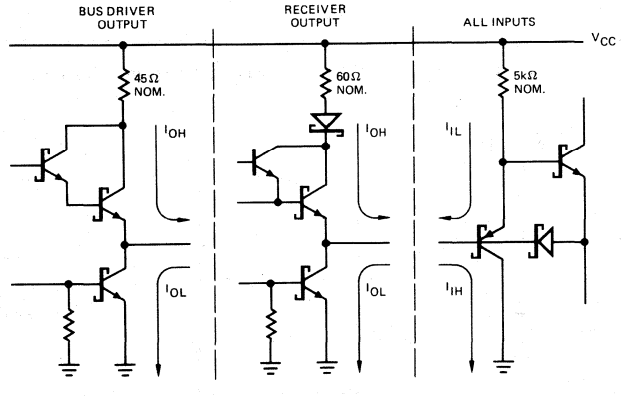
L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

RECEIVER FUNCTION TABLE

INPUTS		Am2926 OUTPUT	Am2929 OUTPUT
$\overline{R/E}$	$\overline{B_i}$	R_i	R_i
H	X	Z	Z
L	L	H	L
L	H	L	H

L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (Data In to Bus)

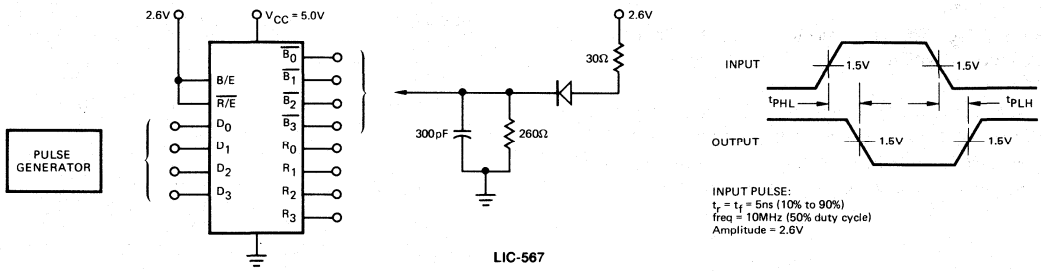

Figure 1

BLI-083

PROPAGATION DELAY (Bus to Receiver Out)

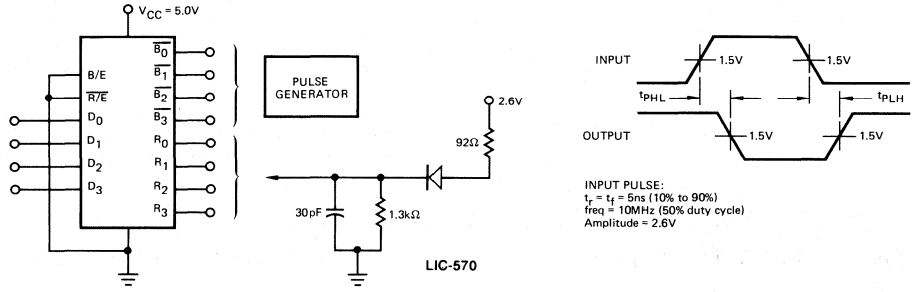

Figure 2

BLI-084

PROPAGATION DELAY (Bus Enable to Bus Output)

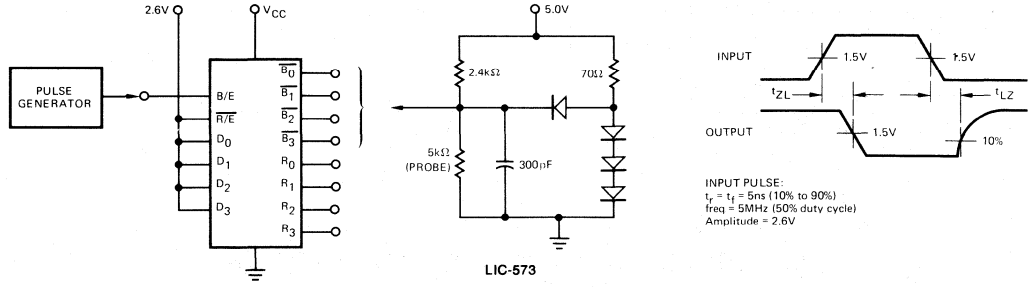

Figure 3

BLI-085

PROPAGATION DELAY (Receive Enable to Receive Output)

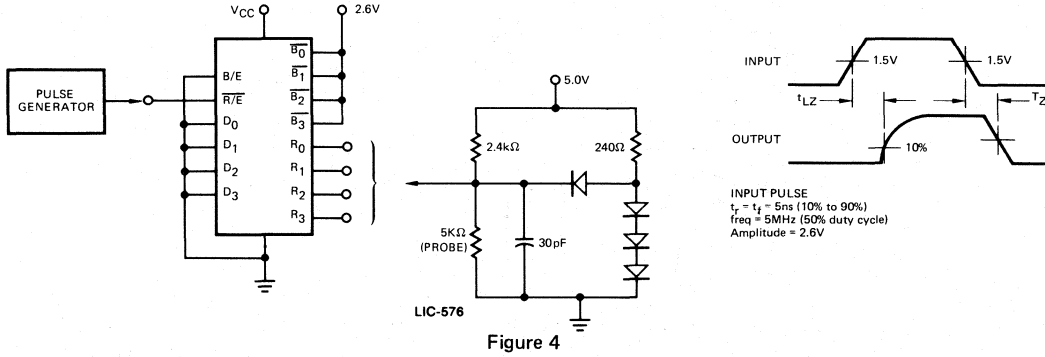

Figure 4

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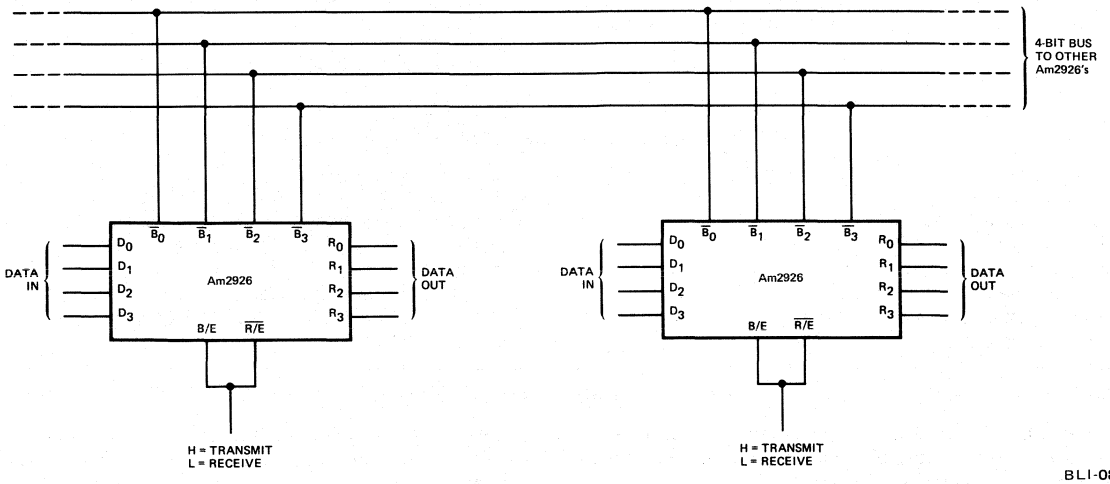
APPLICATION



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ORDERING INFORMATION

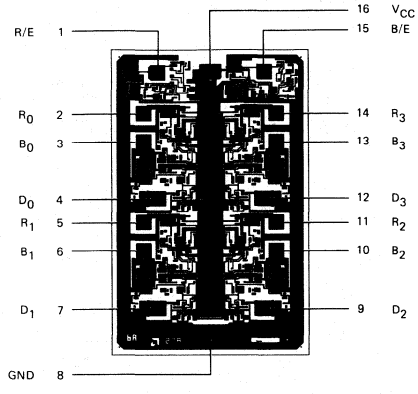
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2926 Order Number	Am2929 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2929PC	AM2929PC	P-16-1	C	C-1
AM2929DC	AM2929DC	D-16-1	C	C-1
AM2929DC-B	AM2929DC-B	D-16-1	C	B-1
AM2926DM		D-16-1	M	C-3
AM2926DM-B		D-16-1	M	B-3
AM2926XC	AM2929XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010 B.
AM2926XM		Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

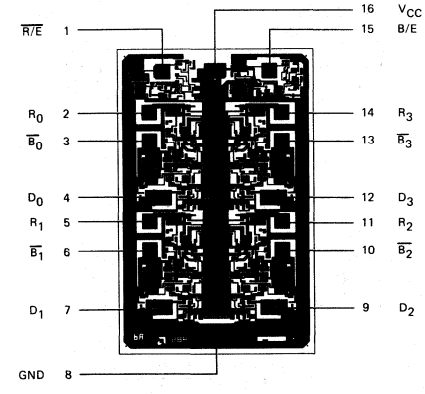
Metallization and Pad Layouts

Am2926



DIE SIZE 0.058" X 0.091"

Am2929



DIE SIZE 0.058" X 0.091"

Am2927 • Am2928

Quad Three-State Bus Transceivers With Clock Enable

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceivers
- Three-state bus driver and receiver outputs
- D-type register on drivers
- Latch output on Am2927
- Registered output on Am2928
- Output data to input wrap around gating
- Input register to output transfer gating with or without driving data bus
- Clock enabled registers
- Bus driver outputs can sink 48mA at 0.5V max.
- Three-state receiver outputs sink 24mA at 0.5V max.
- 3.0V minimum V_{OH} for direct interface to MOS microprocessors
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2927 and Am2928 are high-performance, low-power Schottky, quad bus transceivers intended for use in bipolar or MOS microprocessor system applications.

Both devices feature register enable lines which function as clock enables without introducing gate delay in the clock inputs. The four transceivers share common enables, clock, select and three-state control lines.

The Am2927 consists of four D-type edge-triggered flip-flops. Each flip-flop output is connected to a three-state data bus driver and separately to the input of a corresponding receiver latch input. The receiver latch can select input from the driver or the data bus. The select line determines the source of input data for the bus driver choosing between input data or data recirculated from the receiver output. The receiver output also has a three-state output buffer.

The combination of the select input, S, the driver input enable, $\overline{ENDR}$, and the receiver latch enable, $\overline{RLE}$, provide seven different data path operating modes not available in other transceivers. For example, transmitted data can be stored in the receiver for subsequent retransmission. Also, received data can be output to the system and simultaneously fed back to the driver input.

The Am2928 is similar to the Am2927, but with a D-type edge-triggered register in the receiver and a receiver enable, $\overline{ENREC}$, which functions as a common clock enable.

Data from each D input is inverted at the bus output. Likewise, data at the bus input is inverted at the receiver output.

All three-state controls and enable lines are active low (the Am2927 receiver latch is transparent when $\overline{RLE}$ is LOW). The select input, S, determines whether the enabled driver input accepts data from the data input, D, or from the corresponding receiver output, Y. Similarly, the select line determines whether the receiver accepts input data from the data bus, or the driver output.

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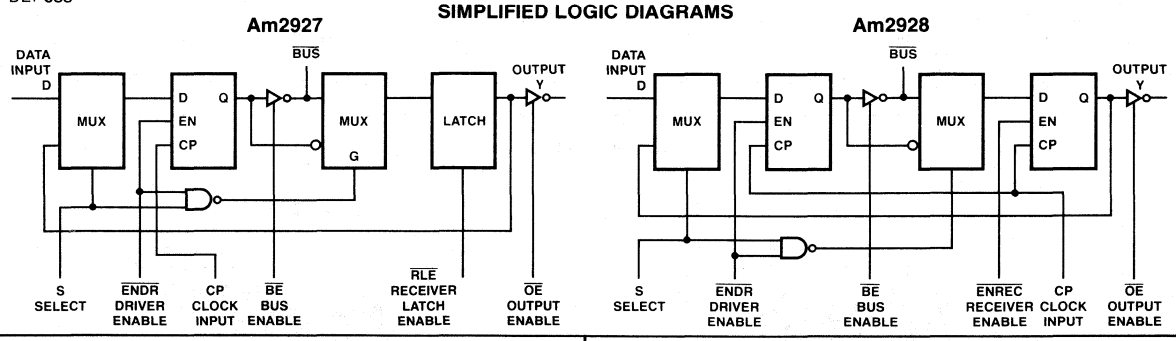
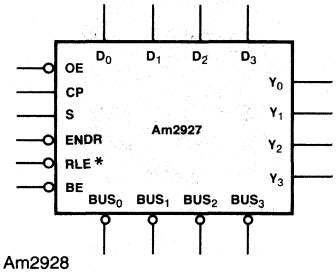
SIMPLIFIED LOGIC DIAGRAMS



LOGIC SYMBOL



*ENREC for Am2928

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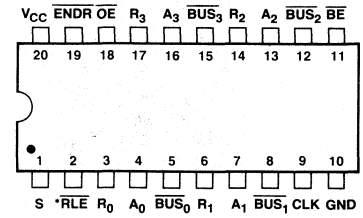
Am2927 CONNECTION DIAGRAM — Top View



*ENREC for Am2928 Note: Pin 1 is marked for orientation.

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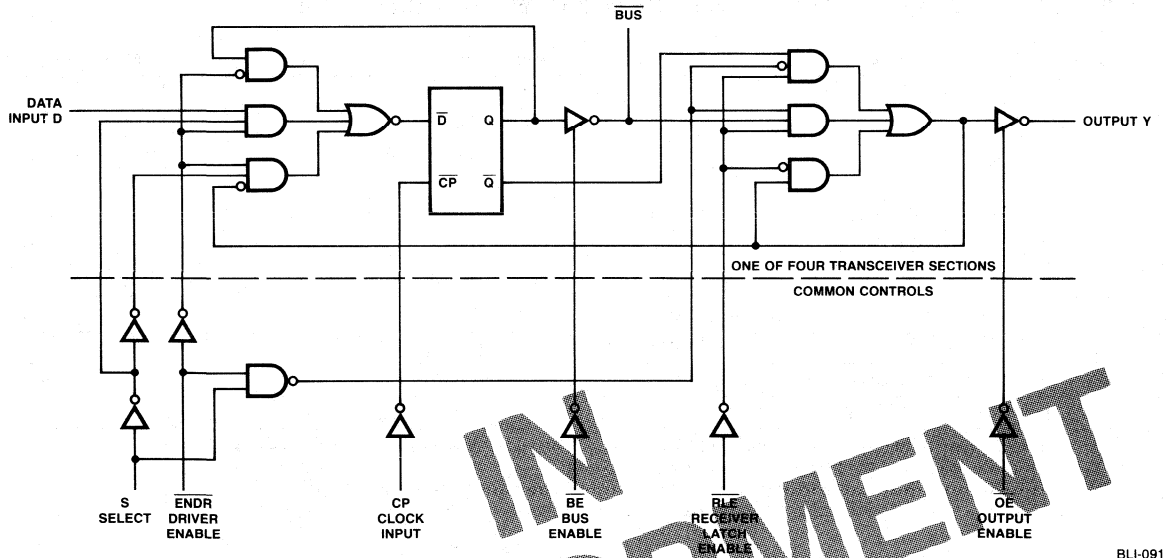
DETAILED LOGIC DIAGRAMS

Am2927



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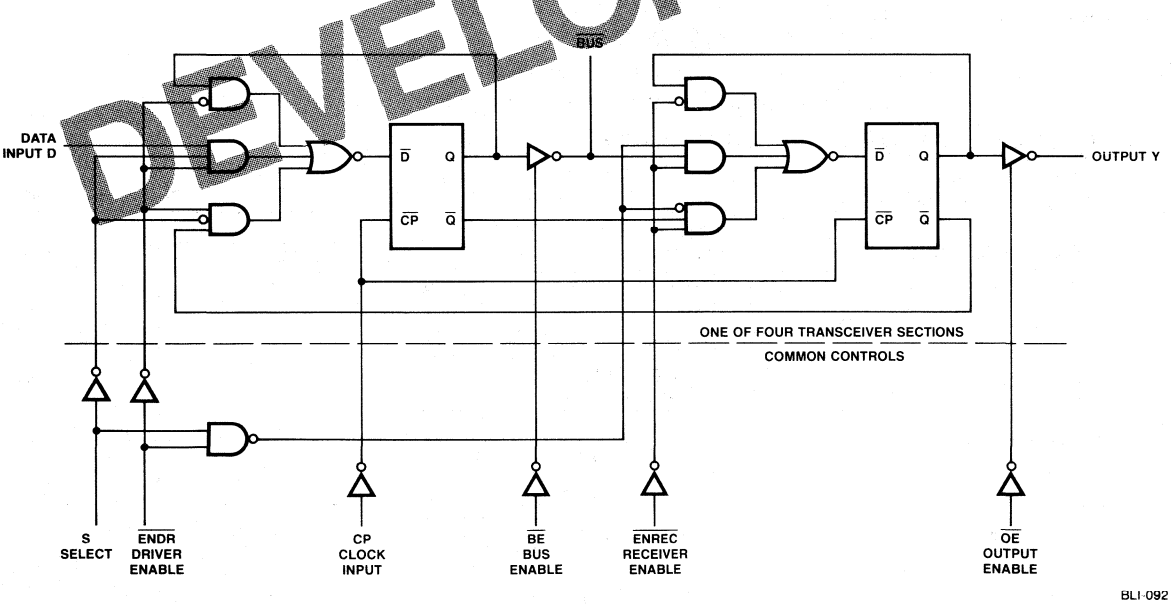
Am2928



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6

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V MAX = 5.25V)
MIL	T_A = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA	2.4			
V_{IH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus Enable = 2.4V				0.8	Volts
I_{OFF}	Bus Leakage Current (Power Off)	V_{CC} = 0V, V_O = 4.5V				100	μA
I_{OZL}	Bus Leakage Current (HIGH Impedance)	V_{CC} = MAX Bus Enable = 2.4V	V_O = 0.4V			−1.4	mA
I_{OZH}			V_O = 2.5V			100	μA
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX, V_O = 0V		−50		−255	mA
C_B	Bus Capacitance (Note 4)	V_{CC} = 0V			8		pF

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. This parameter is typical of device characterization data and is not tested in production.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V MAX = 5.25V)
MIL	T_A = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE (Except Bus Ports)

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.4		
		V_{CC} = 5.0V	I_{OH} = −100μA	3.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 24mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.8	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	S, $\overline{ENDR}$			−2.8	mA
			All other inputs			−1.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	S, $\overline{ENDR}$			100	μA
			All other inputs			50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZH}	Off-State Output Current (Receiver Output)	V_{CC} = MAX	V_O = 2.4V			100	μA
I_{OZL}			V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX	Receiver	−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX	Am2927		150	185	mA
			Am2928		153	190	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2927XM			Am2927XC			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Driver Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		18	26		18	23	ns
t_{PHL}				18	26		18	23	
t_{ZH} • t_{ZL}	Bus Enable, $\overline{BE}$, to $\overline{BUS}$			14	26		14	23	ns
t_{HZ} / t_{LZ}		R_L = 130Ω, C_L = 5pF		12	18/30		12	16/23	
t_{PW}	Min Clock Pulse Width (HIGH or LOW)		18			15			ns
t_{PLH}	$\overline{BUS}$ to Receiver Output (Latch Enabled)	C_L = 50pF, R_L = 270Ω			23		16	20	ns
t_{PHL}					23		16	20	
t_{PLH}	Latch Enable, $\overline{RLE}$, to Receiver Output				26		18	23	ns
t_{PHL}					26		18	23	
t_{ZH} • t_{ZL}	Output Enable, $\overline{OE}$, to Receiver Output				23			21	ns
t_{HZ} • t_{LZ}		C_L = 5pF, R_L = 270Ω			21		14	18	
t_s	Driver Enable, $\overline{ENDR}$, to Clock		10			9			ns
t_h			3			3			
t_s	Select, S, to Clock ($\overline{RLE}$ = HIGH)		18			15			ns
t_h			3			2			
t_{PLH}	Select, S, to Receiver Output	C_L = 50pF, R_L = 270Ω			26			23	ns
t_{PHL}					35			30	
t_s	Data Inputs, D, to Clock		9			7			ns
t_h			5			4			
t_s	$\overline{BUS}$ to Latch Enable, $\overline{RLE}$		11			10			ns
t_h			4			3			

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2928
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2928XM			Am2928XC			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF, R_L (BUS) = 130Ω			26		18	23	ns
t_{PHL}					26		18	23	
t_{ZH} • t_{ZL}	Bus Enable, $\overline{BE}$, to $\overline{BUS}$				26		14	23	ns
t_{HZ} / t_{LZ}		R_L = 130Ω, C_L = 5pF			18/30		12	16/23	
t_{PLH}	Clock, CP, to Receiver Output	C_L = 50pF, R_L = 270Ω			26		18	23	ns
t_{PHL}					26		18	23	
t_{PW}	Min Clock Pulse Width (HIGH or LOW)		18			15			ns
t_{ZH} • t_{ZL}	Output Enable, $\overline{OE}$, to Receiver Output				23		14	21	ns
t_{HZ} • t_{LZ}		C_L = 5pF, R_L = 270Ω			21		14	18	
t_s	Driver Enable, $\overline{ENDR}$, to Clock		10			9			ns
t_h			3			3			
t_s	$\overline{BUS}$ to Clock (Receiver Register)		8			7			ns
t_h			5			4			
t_s	Receiver Enable, $\overline{ENREC}$, to Clock		10			8			ns
t_h			5			4			
t_s	S to Clock		12			10			ns
t_h			5			4			
t_s	Data Inputs, D, to Clock (Driver Register)		9			7			ns
t_h			5			4			

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

DEFINITION OF FUNCTIONAL TERMS

CP — Clock Pulse to internal registers enters data on the LOW-to-HIGH transition.

$\overline{BE}$ — Bus Enable. When Bus Enable is LOW the four drivers drive the $\overline{BUS}$ outputs.

$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ — The four driver outputs and receiver inputs.

D_0, D_1, D_2, D_3 — The four driver data inputs inverting from D to $\overline{BUS}$.

Y_0, Y_1, Y_2, Y_3 — The four receiver data outputs inverting from $\overline{BUS}$ to Y.

S — Select input controls data path modes in conjunction with $\overline{ENDR}$ and $\overline{RLE}$ (or $\overline{ENREC}$).

$\overline{OE}$ — Output Enable. When Output Enable is LOW the four receiver outputs Y are active.

$\overline{ENDR}$ — Driver Enable. Common clock enable for the input register. Allows the data on the D inputs to be loaded into the driver register on the clock LOW-to-HIGH transition.

$\overline{RLE}$ — Receiver Latch Enable (Am2927 only). When Receiver Latch Enable is LOW, the four receiver latches are transparent. The latches hold received data when $\overline{RLE}$ is HIGH.

$\overline{ENREC}$ — Receiver Enable (Am2928 only). Common clock enable for the receiver register. Allows the $\overline{BUS}$ driver or previous receiver data to enter the receiver register on the rising edge of the clock.

Am2927 FUNCTION TABLES

Driver Register Control

$\overline{ENDR}$	S	$\overline{RLE}$	Driver Register
H	X	X	Hold Previous Data
L	L	X	Load from D Input
L	H	L	Load from $\overline{BUS}$
L	H	H	Load Latched Receiver Data

Receiver Latch Control

$\overline{ENDR}$	S	$\overline{RLE}$	Receiver Output
X	X	H	Data Latched
H	H	L	Driver Register Output at Y Output (Latch Transparent)
X	L	L	Bus Data at Y Output (Latch Transparent)
L	X	L	

Am2928 FUNCTION TABLES

Driver Register Control

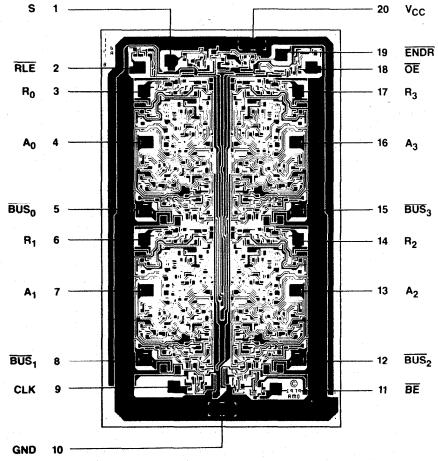
$\overline{ENDR}$	S	Driver Register
H	X	Hold Previous Data
L	L	Load from D Input
L	H	Load from Receiver Register

Receiver Register Control

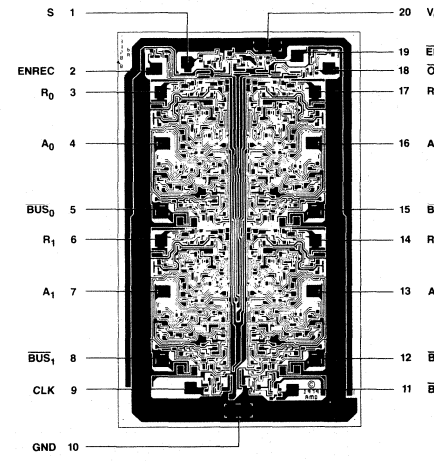
$\overline{ENDR}$	S	$\overline{ENREC}$	Receiver Output
X	X	H	Hold Previous Data
H	H	L	Load from Driver Register
X	L	L	Load from $\overline{BUS}$
L	X	L	

METALLIZATION AND PAD LAYOUTS

Am2927

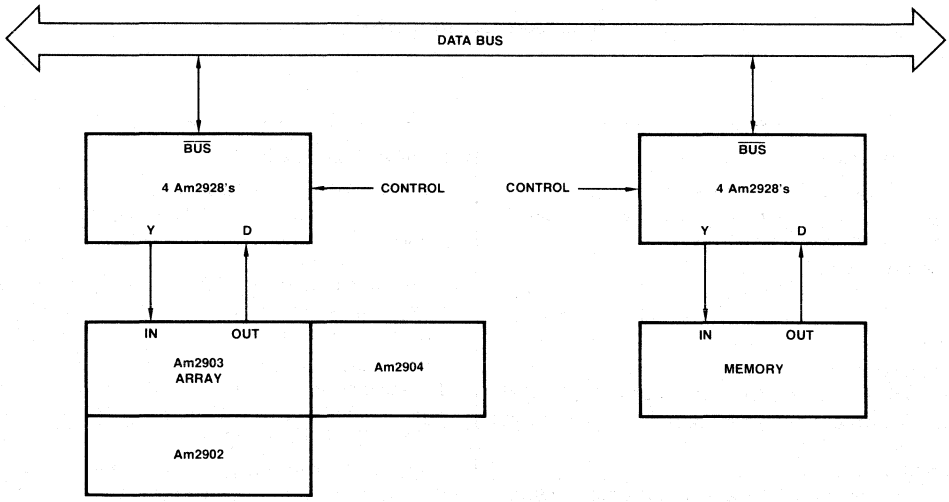


Am2928



DIE SIZE 0.087" X 0.144"

APPLICATION



The Am2927 and Am2928 can be used to provide Data Bus, Address Bus and Control Bus Interface in a high-speed bipolar microprocessor system.

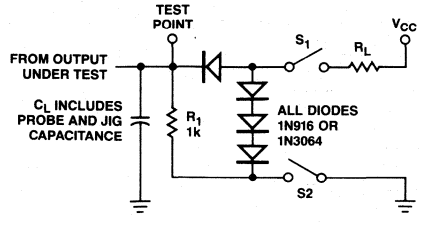
BLI-093

Am2927 AND Am2928 FUNCTION TABLE

Driver Input From	Receiver Input From	Control Input Condition S	Control Input Condition $\overline{ENDR}$	Control Input Condition *	Signal Flow	$\overline{BE}$
D Input	BUS	L	L	L	$\overline{BUS}$ D R	H
	(No Load)	L	L	H	D R	L
Receiver	BUS	H	L	L	D R	H
	(No Load)	H	L	H	D R	L
(No Load)	BUS	L	H	L	D R	H
	Driver	H	H	L	D R	X
	(No Load)	X	H	H	D R	L

*$\overline{RLE}$ for Am2927 (asynchronous) or $\overline{ENREC}$ for Am2928 (⊥).

LOAD TEST CIRCUIT



Note: For standard totem-pole outputs, remove R_1; S_1 and S_2 closed.

ORDERING INFORMATION

Am2927 Order Number	Am2928 Order Number	Package Type	Temperature Range
AM2927DC	AM2928DC	Hermetic DIP	0 to +70°C
AM2927XC	AM2928XC	Dice	0 to +70°C
AM2927DM	AM2928DM	Hermetic DIP	−55 to +125°C
AM2927XM	AM2928XM	Dice	−55 to +125°C

Am2930

Program Control Unit

DISTINCTIVE CHARACTERISTICS

- Powerful, 4-bit slice address controller for memories
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- Executes 32 instructions
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- Contains cascadable full adder
  Twelve different relative address instructions are provided, including jump-to-subroutine relative and return-from-subroutine relative
- Built-in condition code input
  Sixteen instructions are dependent on external condition control
- Seventeen-level push/pop stack
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- Separate incrementer for program counter
  A relative address may be computed and PC may be incremented by one on a single cycle

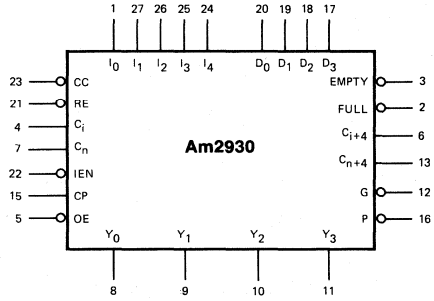
GENERAL DESCRIPTION

The Am2930 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2930's may be interconnected to generate a 16-bit address (64K words). The Am2930 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2930 performs five types of instructions. These are: 1) Unconditional Fetch; 2) Conditional Jump; 3) Conditional Jump-to-Subroutine; 4) Conditional Return-from-Subroutine; and 5) miscellaneous instructions.

There are four sources of data for the adder which generates the Address outputs (Y_0-Y_3). These are: 1) the Program Counter (PC); 2) the Stack (S); 3) the auxiliary Register(R); and 4) the Direct inputs (D). Under control of the Instruction inputs (I_0-I_4), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register. A condition code input is provided for conditional instructions.

LOGIC SYMBOL

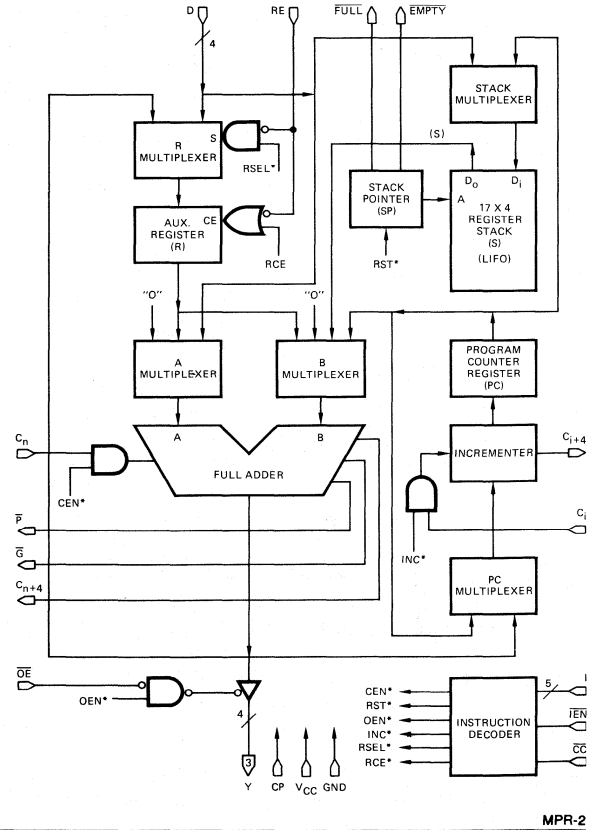


V_{CC} = Pin 28
GND = Pin 14

MPR-220

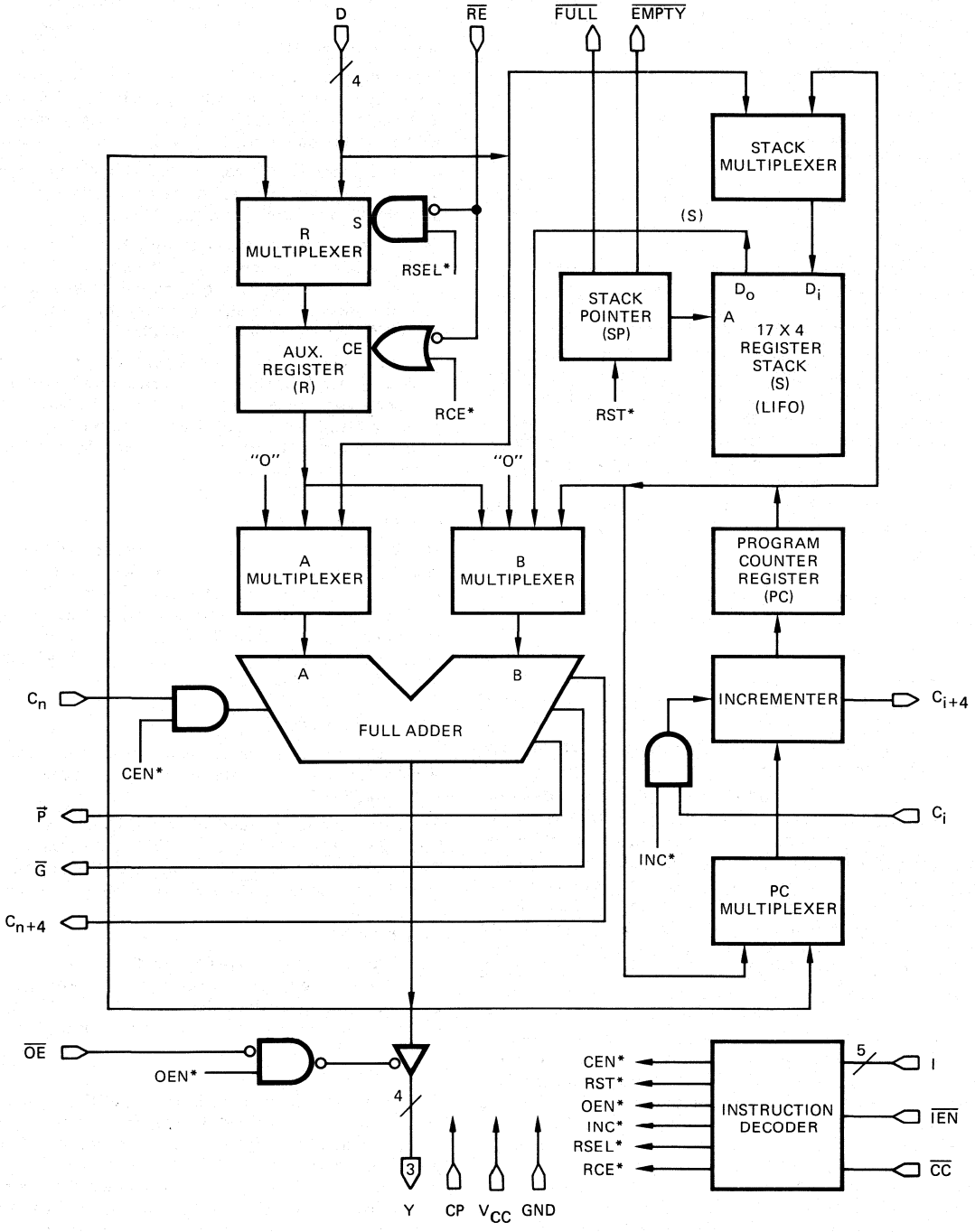
For applications information, see Chapter V of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

BLOCK DIAGRAM



MPR-2

BLOCK DIAGRAM



*INTERNAL

MPR-221

ARCHITECTURE OF THE Am2930

The Am2930 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1) A full adder with input multiplexers
2) A Program Counter Register with an incrementer and an input multiplexer
3) A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4) An auxiliary register with an input multiplexer
5) An instruction decoder
6) Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition and provision is made for further lookahead by including both carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. In slower systems, the carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceeded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During three instructions (unconditional Hold and conditional Hold and Suspend when the $\overline{CC}$ input is LOW), the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer if the $\overline{CC}$ input is LOW. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP+1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Empty output ($\overline{EMPTY}$) is LOW when the stack is empty (after the Reset instruction and after the last word has been Popped from the stack); the active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Register Enable input ($\overline{RE}$) is LOW or if the Instruction inputs call for it to be loaded. When $\overline{RE}$ is LOW, R is loaded from the D inputs unless the Instruction dictates that R be loaded from the output of the Full Adder.

Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

For unconditional instructions, the $\overline{CC}$ input is not utilized; it may be either HIGH or LOW. For conditional instructions, if $\overline{CC}$ is LOW, the condition is met and the conditional operation is performed; if $\overline{CC}$ is HIGH, a Fetch PC is performed.

Output Buffers

The Address outputs (Y_0-Y_3) are three-state drivers which may be disabled either under Instruction control or by a HIGH on the Output Enable input ($\overline{OE}$). Disabling the Y outputs does not affect the execution of instructions inside the Am2930.

Instruction Enable

When HIGH, the Instruction Enable input ($\overline{IEN}$) forces PC and SP into the hold mode and disables the write circuitry to the RAM. The auxiliary register (R) is under control of the $\overline{RE}$ input when $\overline{IEN}$ is HIGH, independent of the state of the Instruction inputs. The $\overline{IEN}$ input does not affect the combinatorial data paths or Y outputs in the Am2930. The data paths are selected by the Instruction and $\overline{CC}$ inputs and are not affected by $\overline{IEN}$.

Am2930 INSTRUCTION SET

The Am2930 Instruction set can be divided into five types of instructions. These are:

- Unconditional Fetches
- Conditional Jumps
- Conditional Jumps-to-Subroutine
- Conditional Returns-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Unconditional Fetches

As can be seen from Table 1, there are nine unconditional Fetch instructions (Instructions 1-9). Under control of the Instruction inputs, the desired function is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instructions 1 through 7, the auxiliary register is under control of the RE input. For Instructions 8 and 9, R is loaded with PC and R + D, respectively. The RAM and Stack Pointer are not changed during a Fetch instruction.

Conditional Jumps

There are six conditional Jump instructions (Instructions 16 through 21). Under control of the Instruction inputs, the desired function is placed at the Y outputs. Additionally, the desired function is incremented if C_i of the least significant device is HIGH and loaded into PC. During these instructions, R is controlled by $\overline{RE}$. The RAM and Stack Pointer are not changed during these instructions. The above operations are performed if the $\overline{CC}$ input is LOW; if $\overline{CC}$ is HIGH, a Fetch PC operation is performed.

Conditional Jumps-to-Subroutine

There are six conditional Jump-to-Subroutine instructions (Instructions 22 through 27). Under control of the Instruction inputs, the desired function is placed on the Y outputs. On the rising edge of the clock the data on the Y outputs is incremented and loaded into PC, PC is loaded into the RAM at location SP+1; and SP is incremented.

As with Conditional Jump Instructions, R is controlled by $\overline{RE}$ and whether the Jump-to-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Conditional Returns-from-Subroutine

There are two conditional Return-from-Subroutine instructions (Instructions 28 and 29). Under control of the instruction inputs, either S or S+D is placed at the Y outputs. Additionally, the selected function is incremented and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock).

As with the Condition Jump and Jump-to-Subroutine Instructions, R is controlled by $\overline{RE}$ and whether the Return-from-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM is unchanged and R is controlled by $\overline{RE}$.

Load R (Instruction 10)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 11)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 12)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 13)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is controlled by $\overline{RE}$.

Pop PC (Instruction 14)

This instruction is the same as Fetch PC except SP is decremented at the end of the cycle, causing the data at the top of the stack to be lost.

Hold (Instruction 15)

This instruction places PC at the Y outputs and inhibits any change in PC, SP, and RAM. R is controlled by $\overline{RE}$.

Conditional Hold (Instruction 30)

This instruction is the same as Hold except $\overline{CC}$ must be LOW. If $\overline{CC}$ is HIGH, the Fetch PC instruction is performed.

Suspend (Instruction 31)

The Suspend instruction is the same as th Conditional Hold instruction except the Y outputs are forced into the high-impedance state if $\overline{CC}$ is LOW.

TABLE I — Am2930 INSTRUCTION SET

Mnemonic	Instruction Number	I_4	I_3	I_2	I_1	I_0	$\overline{CC}$	$\overline{IEN}$	Instruction	Y_0-Y_3	Next State (after CP ⎍) (Note 3) PC	R $\overline{RE}$ = L	R $\overline{RE}$ = H	RAM	SP
		X	X	X	X	X	X	H	Instruction Disable	Note 1	—	D	—	—	—
PRST	0	L	L	L	L	L	X	L	RESET	"0"	"0"+C_i	D	—	—	Reset
FPC	1	L	L	L	L	H	X	L	FETCH PC	PC	PC+C_i	D	—	—	—
FR	2	L	L	L	H	L	X	L	FETCH R	R	PC+C_i	D	—	—	—
FD	3	L	L	L	H	H	X	L	FETCH D	D	PC+C_i	D	—	—	—
FRD	4	L	L	H	L	L	X	L	FETCH R+D	R+D+C_n	PC+C_i	D	—	—	—
FPD	5	L	L	H	L	H	X	L	FETCH PC+D	PC+D+C_n	PC+C_i	D	—	—	—
FPR	6	L	L	H	H	L	X	L	FETCH PC+R	PC+R+C_n	PC+C_i	D	—	—	—
FSD	7	L	L	H	H	H	X	L	FETCH S+D	S+D+C_n	PC+C_i	D	—	—	—
FPLR	8	L	H	L	L	L	X	L	FETCH PC → R	PC	PC+C_i	PC	PC	—	—
FRDR	9	L	H	L	L	H	X	L	FETCH R+D → R	R+D+C_n	PC+C_i	R+D+C_n	R+D+C_n	—	—
PLDR	10	L	H	L	H	L	X	L	LOAD R	PC	PC+C_i	D	D	—	—
PSHP	11	L	H	L	H	H	X	L	PUSH PC	PC	PC+C_i	D	—	PC → Loc SP+1	SP+1
PSHD	12	L	H	H	L	L	X	L	PUSH D	PC	PC+C_i	D	—	D → Loc SP+1	SP+1
POPS	13	L	H	H	L	H	X	L	POP S	S	PC+C_i	D	—	—	SP−1
POPP	14	L	H	H	H	L	X	L	POP PC	PC	PC+C_i	D	—	—	SP−1
PHLD	15	L	H	H	H	H	X	L	HOLD	PC	—	D	—	—	
	16-31	H	X	X	X	X	H	L	FAIL COND'L TEST (FETCH PC)	PC	PC+C_i	D	—	—	—
JMPR	16	H	L	L	L	L	L	L	JUMP R	R	R+C_i	D	—	—	—
JMPD	17	H	L	L	L	H	L	L	JUMP D	D	D+C_i	D	—	—	—
JMPZ	18	H	L	L	H	L	L	L	JUMP "0"	"0"	"0"+C_i	D	—	—	—
JPRD	19	H	L	L	H	H	L	L	JUMP R+D	R+D+C_n	R+D+C_n+C_i	D	—	—	—
JPPD	20	H	L	H	L	L	L	L	JUMP PC+D	PC+D+C_n	PC+D+C_n+C_i	D	—	—	—
JPPR	21	H	L	H	L	H	L	L	JUMP PC+R	PC+R+C_n	PC+R+C_n+C_i	D	—	—	—
JSBR	22	H	L	H	H	L	L	L	JSB R	R	R+C_i	D	—	PC → Loc SP+1	SP+1
JSBD	23	H	L	H	H	H	L	L	JSB D	D	D+C_i	D	—	PC → Loc SP+1	SP+1
JSBZ	24	H	H	L	L	L	L	L	JSB "0"	"0"	"0"+C_i	D	—	PC → Loc SP+1	SP+1
JSRD	25	H	H	L	L	H	L	L	JSB R+D	R+D+C_n	R+D+C_n+C_i	D	—	PC → Loc SP+1	SP+1
JSPD	26	H	H	L	H	L	L	L	JSB PC+D	PC+D+C_n	PC+D+C_n+C_i	D	—	PC → Loc SP+1	SP+1
JSPR	27	H	H	L	H	H	L	L	JSB PC+R	PC+R+C_n	PC+R+C_n+C_i	D	—	PC → Loc SP+1	SP+1
RTS	28	H	H	H	L	L	L	L	RETURN S	S	S+C_i	D	—	—	SP−1
RTSD	29	H	H	H	L	H	L	L	RETURN S+D	S+D+C_n	S+D+C_n+C_i	D	—	—	SP−1
CHLD	30	H	H	H	H	L	L	L	HOLD	PC	—	D	—	—	—
PSUS	31	H	H	H	H	H	L	L	SUSPEND	Z (Note 2)	—	D	—	—	—

PC — Program Counter SP — Stack Pointer
R — Auxiliary Register D — Direct Inputs

Notes: 1. When $\overline{IEN}$ is HIGH, the Y_0-Y_3 outputs contain the same data as when $\overline{IEN}$ is LOW, as determined by I_0-I_4 and $\overline{CC}$.
2. Z = High impedance state (outputs "OFF").
3. — = No change

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Part Number	Temperature	V_{CC}
Am2930PC, DC	T_A = 0 to 70°C	4.75V to 5.25V
Am2930DM, FM	T_C = −55 to +125°C	4.50V to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3 $\overline{G}$, C_{n+4}, C_{i+4}	I_{OH} = −1.6mA	2.4			Volts
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OH} = −1.2mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, C_{n+4} C_{i+4}	I_{OL} = 16mA			0.5	
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-3}				−.360	mA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				−.702	
			$\overline{CC}$				−.657	
			C_i				−2.31	
			C_n				−3.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-3}				20	μA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				40	
			$\overline{CC}$				50	
			C_i				90	
			C_n				250	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V	Y_{0-3}	V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = 5.0V		T_A = 25°C		150	205	mA
		V_{CC} = MAX.		T_C = −55 to +125°C			239	
				T_C = +125°C			170	
				T_A = 0 to 70°C			220	
				T_A = 70°C			185	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. Minimum I_{CC} is at maximum temperature.

Am2930 SWITCHING CHARACTERISTICS

Tables A, B, C and D define the timing characteristics of the Am2930. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

I. Typical Room Temperature Performance.

V_{CC} = 5.0V, T_A = 25°C

TABLE IA
Clock Characteristics.

Minimum Clock LOW Time	18ns
Minimum Clock HIGH Time	20ns

TABLE IB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	18	17
$\overline{CC}$ (Note 1)	Y	39	27
I_{4-0} (Note 1)	Y	57	41

TABLE IC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4=L	C_{i+4} I_4=H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	61	50	57	61	69	52	–
$\overline{CC}$	46	32	39	–	53	29	–
C_n	25	–	17	–	32	–	–
C_i	–	–	–	14	14	–	–
CP	52	40	46	33	58	40	40
D	37	23	30	–	43	–	–
$\overline{IEN}$	–	–	–	–	–	27	–

Note 1: "Suspend" instruction.

TABLE ID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
I_{4-0}	68	0
$\overline{CC}$	53	0
$\overline{IEN}$	39	0
C_n	28	0
C_i	18	3
D ($\overline{RE}$ = L, I_{4-0} = 0-8 or 10-15)	14	0
D (All other conditions)	44	0
$\overline{RE}$	13	2

II. Guaranteed Performance Over Commercial Operating Range.

V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C

TABLE IIA
Clock Characteristics.

Minimum Clock LOW Time	31ns
Minimum Clock HIGH Time	33ns

TABLE IIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	27	26
$\overline{CC}$ (Note 1)	Y	55	37
I_{4-0} (Note 1)	Y	80	55

TABLE IIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4=L	C_{i+4} I_4=H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	81	67	77	80	91	69	–
$\overline{CC}$	63	45	55	–	72	42	–
C_n	32	–	25	–	45	–	–
C_i	–	–	–	22	22	–	–
CP	69	53	61	43	78	55	55
D	49	33	40	–	59	–	–
$\overline{IEN}$	–	–	–	–	–	40	–

Note 1: "Suspend" instruction.

TABLE IID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
I_{4-0}	114	0
$\overline{CC}$	75	0
$\overline{IEN}$	55	0
C_n	43	0
C_i	32	5
D ($\overline{RE}$ = L, I_{4-0} = 0-8 or 10-15)	25	2
D (All other conditions)	66	2
$\overline{RE}$	24	4

III. Guaranteed Performance Over Military Operating Range.

V_{CC} = 4.5 to 5.5V, T_C = −55 to +125°C

TABLE IIIA
Clock Characteristics.

Minimum Clock LOW Time	35ns
Minimum Clock HIGH Time	35ns

TABLE IIIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	32	31
$\overline{CC}$ (Note 1)	Y	60	42
I_{4-0} (Note 1)	Y	85	60

TABLE IIIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4=L	C_{i+4} I_4=H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	88	74	82	87	97	78	–
$\overline{CC}$	68	52	60	–	78	47	–
C_n	37	–	30	–	46	–	–
C_i	–	–	–	23	23	–	–
CP	74	58	66	48	84	60	60
D	55	38	45	–	65	–	–
$\overline{IEN}$	–	–	–	–	–	45	–

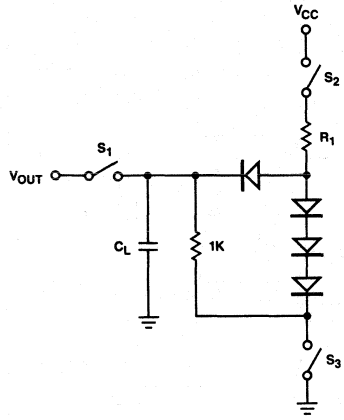
Note 1: "Suspend" instruction.

TABLE IIID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
I_{4-0}	124	0
$\overline{CC}$	80	0
$\overline{IEN}$	69	0
C_n	52	0
C_i	37	5
D ($\overline{RE}$ = L, I_{4-0} = 0-8 or 10-15)	30	2
D (All other conditions)	72	2
$\overline{RE}$	29	4

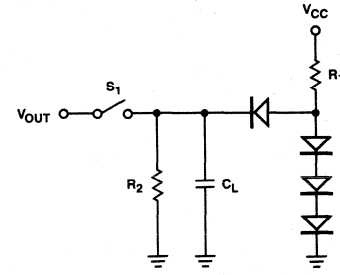
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2930

A. THREE STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2930

Pin #	Pin Label	Test Circuit	R_1	R_2
2	$\overline{FULL}$	B	300	2K
3	$\overline{EMPTY}$	B	300	2K
6	C_{i+4}	B	240	1.5K
8-11	Y_{0-3}	A	240	1K
12	$\overline{G}$	B	240	1.5K
13	C_{n+4}	B	240	1.5K
16	P	B	300	2K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

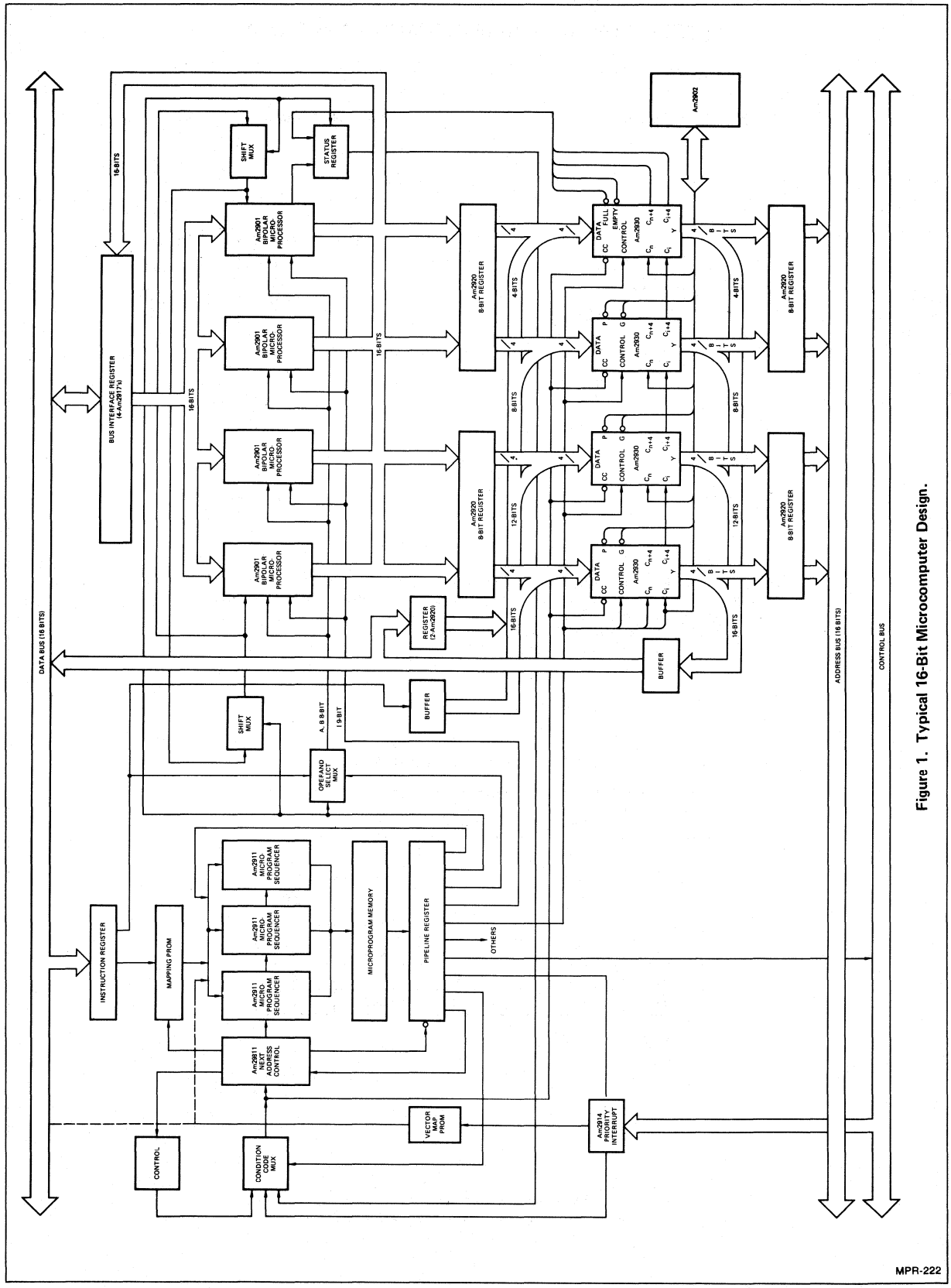


Figure 1. Typical 16-Bit Microcomputer Design.

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APPLICATIONS

The Am2930 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2930 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901's via a 16-bit register.

The Address outputs (Y) of the Am2930 are loaded into a 16-bit Memory Address Register (MAR). Although the MAR is shown as part of the CPU, in some applications it may be part of the memory.

An Am2902 High-Speed Lookahead Carry Generator is utilized to provide high-speed relative and indexed addressing. In slower systems, the C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

The Condition Code input ($\overline{CC}$) is derived from the same condition code multiplexer which generates the condition code input for the microprogram sequencer.

The control inputs of the Am2930 (I_{0-4}, $\overline{IEN}$, $\overline{RE}$, $\overline{OE}$, and C_i and C_n of the least significant device) are shown originating at the Pipeline Register. Although it is not shown in Figure 1, it is possible to share the Pipeline Register outputs which go to these pins with another device. This can be accomplished if both the Am2930 and the other device do not operate on the same microcycle. Forcing the $\overline{IEN}$ input HIGH inhibits any changes in the Am2930 internal registers, independent of the state of these seven inputs. This allows the Am2930 to be placed in a hold mode while the other device is using the same Pipeline Register outputs as control signals.

PIN DEFINITIONS

I_{0-4} The five Instruction control lines to the Am2930, used to establish data paths and enable internal registers.

$\overline{IEN}$ The Instruction Enable Input, used to enable and disable internal registers. When $\overline{IEN}$ is LOW, all internal registers are under control of the Instruction inputs. When $\overline{IEN}$ is HIGH, all internal registers except R are inhibited from changing state. R is controlled by the $\overline{RE}$ input. The $\overline{IEN}$ input does not affect the combinatorial data paths and the outputs established by the Instruction inputs.

$\overline{CC}$ The Condition Code input determines whether or not a conditional instruction (Instructions 16-31) is performed. If $\overline{CC}$ is LOW, the conditional instruction is executed. If $\overline{CC}$ is HIGH, Fetch PC (Instruction 1) is executed. The $\overline{CC}$ input may be either HIGH or LOW for unconditional instructions (Instructions 0-15).

$\overline{RE}$ The Register Enable input for the Auxiliary Register (R). A LOW on $\overline{RE}$ causes the Auxiliary Register (R) to be loaded from the D inputs unless Instruction 8 or 9 is being executed and $\overline{IEN}$ is LOW.

C_n The carry-in to the Full Adder.

C_{n+4} The carry-out of the Full Adder.

$\overline{P}$, $\overline{G}$ The carry generate and propagate outputs of the Full Adder.

C_i The carry-in to the program counter incrementer.

C_{i+4} The carry-out of the program counter incrementer.

Y_{0-3} The four address outputs of the Am2930. These are three-state output lines. When enabled, they display the outputs of the Full Adder.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high-impedance); when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

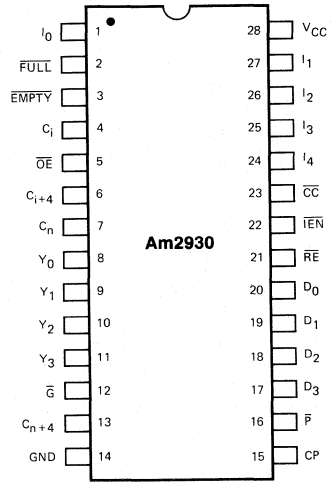
D_{0-3} The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.

$\overline{Empty}$ The Empty output is LOW when the Stack is empty.

$\overline{Full}$ The Full output is LOW when the LIFO stack is full — during and after the 17th push operation.

CP The clock input to the Am2930. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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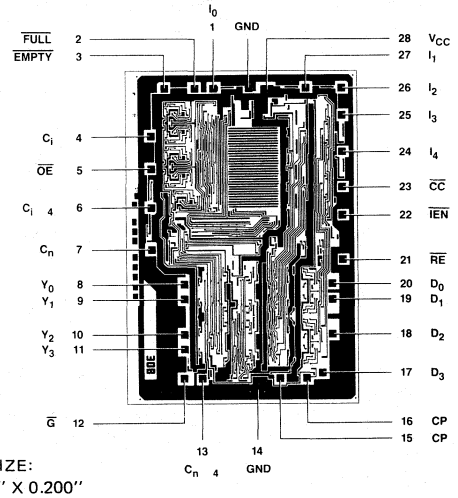
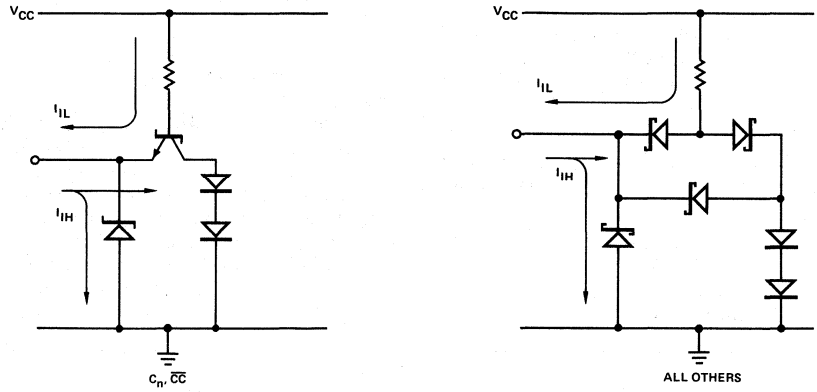
METALLIZATION AND PAD LAYOUT



DIE SIZE:
0.133" X 0.200"

INPUT/OUTPUT CIRCUIT CURRENT INTERFACE

DRIVEN INPUTS



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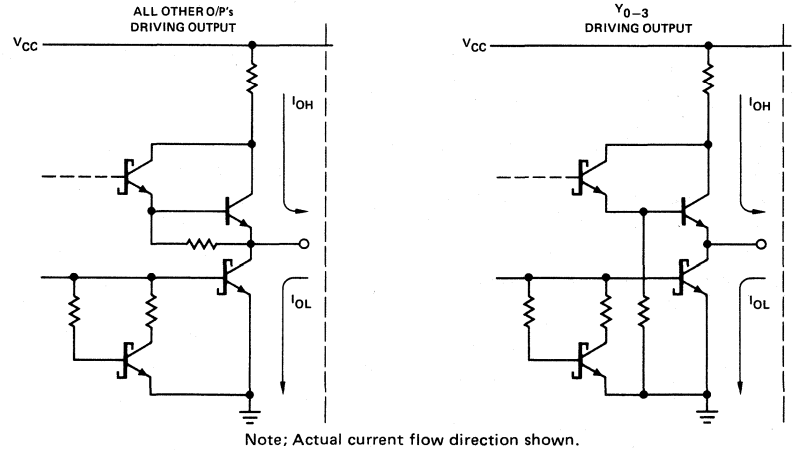
Note; C_i input is connected to both configurations in parallel.

DRIVING OUTPUTS



Note; Actual current flow direction shown.

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2930DC	D-28	C	C-1
AM2930DC-B	D-28	C	B-2 (Note 4)
AM2930DM	D-28	M	C-3
AM2930DM-B	D-28	M	B-3
AM2930FM	F-28-2	M	C-3
AM2930FM-B	F-28-2	M	B-3
AM2930XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2930XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V; M = −55 to +125°C, V_{CC} = 4.50 to 5.50V
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2932
Program Control Unit/Push-Pop Stack

DISTINCTIVE CHARACTERISTICS

- Powerful, 4-bit slice address controller for memories
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- Executes 16 instructions
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- Contains cascadable full adder
  Eight relative address instructions are provided, including jump relative and jump-to-subroutine relative
- Seventeen-level push/pop stack
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- Separate incrementer for program counter
  A relative address may be computed and PC may be incremented by one on a single cycle

GENERAL DESCRIPTION

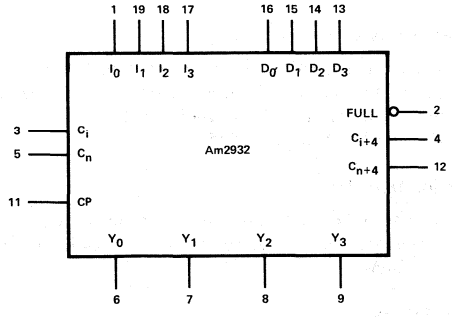
The Am2932 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2932s may be interconnected to generate a 16-bit address (64K words). The Am2932 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2932 performs five types of instructions. These are: 1) Fetch; 2) Jump; 3) Jump-to-Subroutine; 4) Return-from-Subroutine; and 5) miscellaneous instructions.

There are four sources of data for the adder which generates the Address outputs (Y_0-Y_3). These are: 1) the Program Counter(PC); 2) the Stack (S); 3) the auxiliary Register(R); and 4) the Direct inputs (D). Under control of the Instruction inputs (I_0-I_3), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register.

6

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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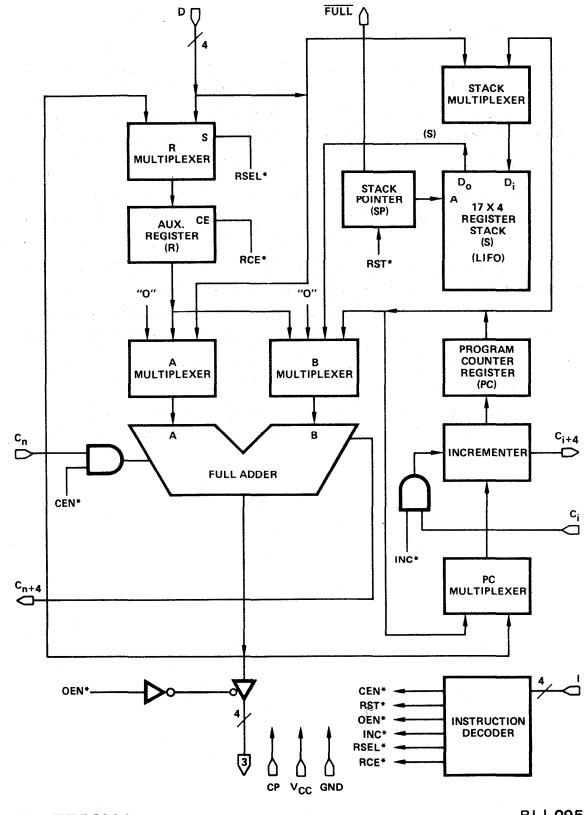
For applications information, see Chapter V of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

BLOCK DIAGRAM



*INTERNAL

BLI-095

ARCHITECTURE OF THE Am2932

The Am2932 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1) A full adder with input multiplexers
2) A Program Counter Register with an incrementer and an input multiplexer
3) A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4) An auxiliary register with an input multiplexer
5) An instruction decoder
6) Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition. The carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During the suspend instruction the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP+1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Instruction inputs call for it to be loaded.

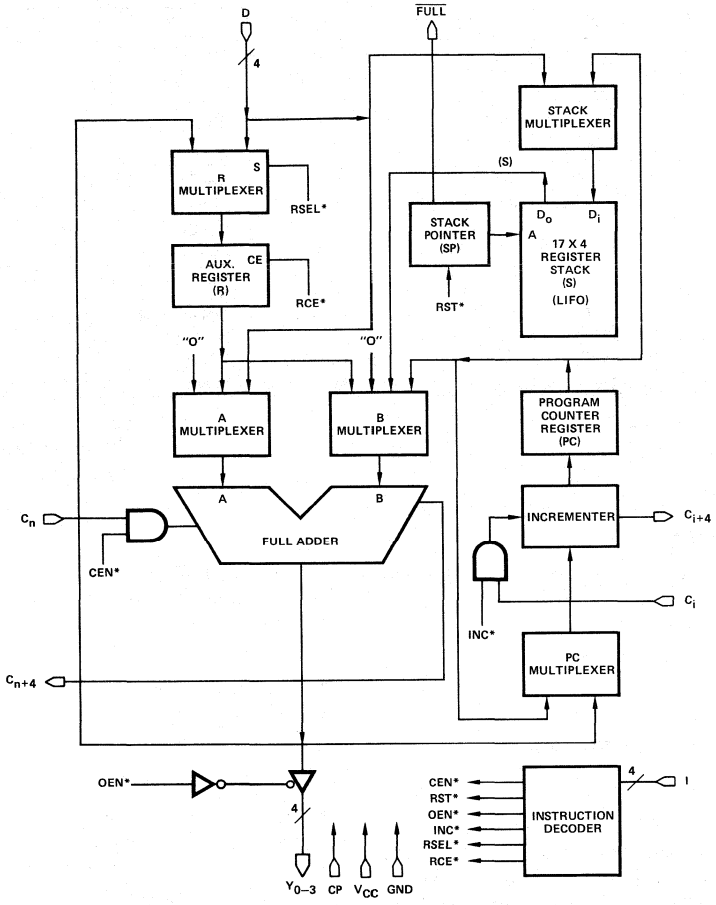
Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

Output Buffers

The Address outputs (Y_0-Y_3) are three-state drivers which may be disabled under Instruction control.

BLOCK DIAGRAM



*INTERNAL

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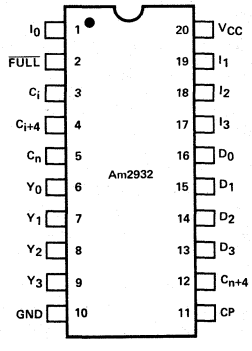
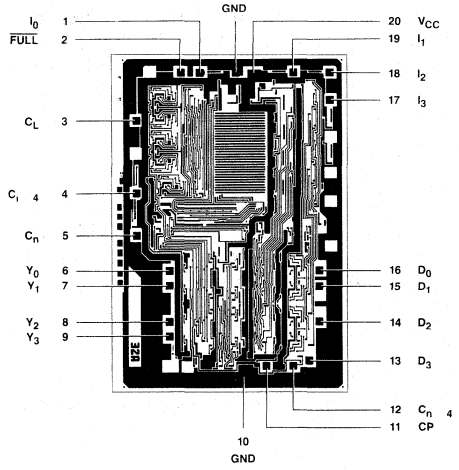
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-097

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.134" X 0.200"

TABLE I – Am2932 INSTRUCTION SET

Instruction Number	I_3	I_2	I_1	I_0	Mnemonic	Instruction	Y_0-Y_3	Next State (after CP↑) – Note 2			
								PC	R	RAM	SP
0	L	L	L	L	PRST	RESET	"0"	"0"+C_i	–	–	Reset
1	L	L	L	H	PSUS	SUSPEND	Z (Note 1)	–	–	–	–
2	L	L	H	L	PSHD	PUSH D	PC	PC+C_i	–	D→Loc SP+1	SP+1
3	L	L	H	H	POPS	POP S	S	PC+C_i	–	–	SP–1
4	L	H	L	L	FPC	FETCH PC	PC	PC+C_i	–	–	–
5	L	H	L	H	JMPD	JUMP D	D	D+C_i	–	–	–
6	L	H	H	L	PSHP	PUSH PC	PC	PC+C_i	–	PC→Loc SP+1	SP+1
7	L	H	H	H	RTS	RETURN S	S	S+C_i	–	–	SP–1
8	H	L	L	L	FR	FETCH R	R	PC+C_i	–	–	–
9	H	L	L	H	FPR	FETCH PC+R	PC+R+C_n	PC+C_i	–	–	–
10	H	L	H	L	FPLR	FETCH PC→R	PC	PC+C_i	PC	–	–
11	H	L	H	H	JMPR	JUMP R	R	R+C_i	–	–	–
12	H	H	L	L	JPPR	JUMP PC+R	PC+R+C_n	PC+R+C_n+C_i	–	–	–
13	H	H	L	H	JSBR	JSB R	R	R+C_i	–	PC→Loc SP+1	SP+1
14	H	H	H	L	JSPR	JSB PC+R	PC+R+C_n	PC+R+C_n+C_i	–	PC→Loc SP+1	SP+1
15	H	H	H	H	PLDR	LOAD R	PC	PC+C_i	D	–	–

Notes: 1. Z = High impedance state (outputs "OFF")
2. – = No change

PC – Program Counter
R – Auxiliary Register
SP – Stack Pointer
D – Direct Inputs

Am2932 INSTRUCTION SET

The Am2932 Instruction set can be divided into five types of instructions. These are:

- Fetches
- Jumps
- Jumps-to-Subroutine
- Return-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Fetches

As can be seen from Table I, there are four Fetch instructions (Instructions 4, 8, 9, 10). Under control of the Instructions inputs, the desired function is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instruction 10 R is loaded with PC. The RAM and Stack Pointer are not changed during a Fetch instruction.

Jumps

There are three Jump instructions (Instructions 5, 11, 12). Under control of the Instruction inputs, the desired function is placed at the Y outputs. Additionally, the desired function is incremented if C_i of the least significant device is HIGH and loaded into PC. The RAM, Stack Pointer and R are not changed during these instructions.

Jumps-to-Subroutine

There are two Jump-to-Subroutine instructions (Instructions 13 and 14). Under control of the Instruction inputs, the desired function is placed on the Y outputs. On the rising edge of the clock the data on the Y outputs is incremented and loaded into PC, PC is loaded into the RAM at location SP+1; and SP is incremented.

During these instructions, R is not changed.

Return-from-Subroutine (Instruction 7)

Under control of the instruction inputs, S is placed at the Y outputs. Additionally, S is incremented and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock).

During this instruction, R is not changed.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM and R are unchanged.

Load R (Instruction 15)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 6)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 2)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 3)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is not changed.

Suspend (Instruction 1)

The Suspend instruction inhibits any change in PC, SP, R and RAM and forces the Y outputs into the high impedance state.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Part Number	Temperature	V_{CC}
Am2932DC	T_A = 0 to 70°C	4.75V to 5.25V
Am2932DM	T_C = −55 to +125°C	4.50V to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3 C_{n+4} C_{i+4}	I_{OH} = −1.6mA	2.4			Volts
			$\overline{FULL}$	I_{OH} = −1.2mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			C_{n+4}, C_{i+4}	I_{OL} = 16mA			0.5	
			$\overline{FULL}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-3}				−.360	mA
			I_{0-3}, CP				−.702	
			C_i				−2.0	
			C_n				−3.69	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-3}				20	μA
			I_{0-3}, CP				40	
			C_i				90	
			C_n				250	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V	Y_{0-3}	V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = 5.0V		T_A = 25°C		128	176	mA
		V_{CC} = MAX.		T_C = −55 to +125°C			210	
				T_C = +125°C			145	
				T_A = 0 to 70°C			190	
				T_A = 70°C			160	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. Minimum I_{CC} is at maximum temperature.

Am2932 SWITCHING CHARACTERISTICS

Tables A, B, C and D define the timing characteristics of the Am2932. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

I. Typical Room Temperature Performance.

V_{CC} = 5.0V, T_A = 25°C

TABLE IA
Clock Characteristics.

Minimum Clock LOW Time	18ns
Minimum Clock HIGH Time	20ns

TABLE IB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	57	41

TABLE IC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	C_{n+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	61	57	69	61	52
C_n	25	17	32	–	–
C_i	–	–	14	14	–
CP	52	46	58	33	40
D	29	–	37	–	–

Notes: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

TABLE ID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
C_n	28	0
C_i	18	3
D	35	0
I_{3-0}	68	0

II. Guaranteed Performance Over Commercial Operating Range.

V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C

TABLE IIA
Clock Characteristics.

Minimum Clock LOW Time	31ns
Minimum Clock HIGH Time	33ns

TABLE IIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	80	55

TABLE IIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	C_{n+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	81	77	91	80	69
C_n	32	25	45	–	–
C_i	–	–	22	22	–
CP	69	61	78	43	55
D	39	–	50	–	–

Notes: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

TABLE IID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
C_n	43	0
C_i	32	5
D	52	2
I_{3-0}	114	0

III. Guaranteed Performance Over Military Operating Range.

V_{CC} = 4.5 to 5.5V, T_C = −55 to +125°C

TABLE IIIA
Clock Characteristics.

Minimum Clock LOW Time	35ns
Minimum Clock HIGH Time	35ns

TABLE IIIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	85	60

TABLE IIIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	C_{n+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	88	82	97	87	78
C_n	37	30	46	–	–
C_i	–	–	23	23	–
CP	74	66	84	45	60
D	44	–	55	–	–

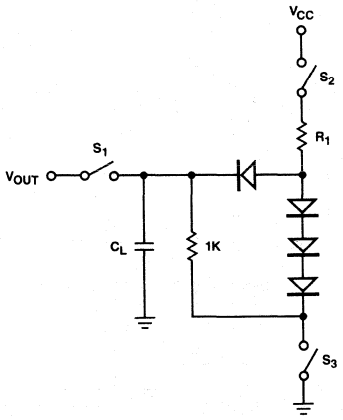
Notes: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

TABLE IIID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
C_n	52	0
C_i	37	5
D	60	2
I_{3-0}	124	0

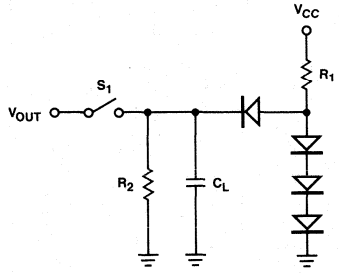
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2932

A. THREE STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2932

Pin #	Pin Label	Test Circuit	R_1	R_2
2	$\overline{FULL}$	B	300	2K
4	C_{i+4}	B	240	1.5K
6-9	Y_{0-3}	A	240	1K
12	C_{n+4}	B	240	1.5K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

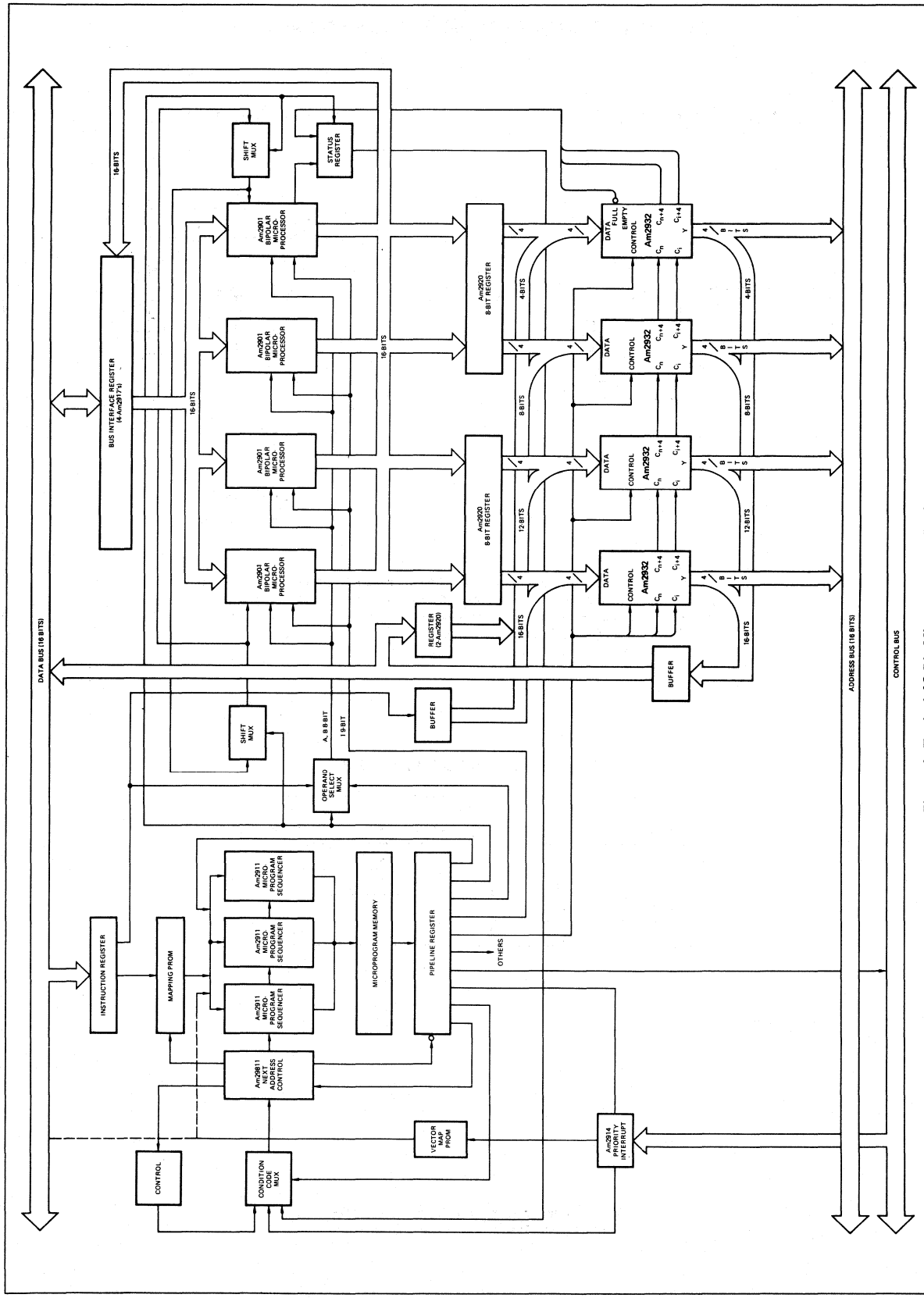


Figure 1. Typical 16-Bit Microcomputer Design.

APPLICATIONS

The Am2932 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2932 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901s via a 16-bit register.

The Address outputs (Y) of the Am2932 are passed to the address bus.

The C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

The control inputs of the Am2932 (I_{0-3}, C_i and C_n of the least significant device) are shown originating at the Pipeline Register.

PIN DEFINITIONS

I_{0-3} The four Instruction control lines to the Am2932, used to establish data paths and enable internal registers.

C_n The carry-in to the Full Adder.

C_{n+4} The carry-out of the Full Adder.

C_i The carry-in to the program counter incrementer.

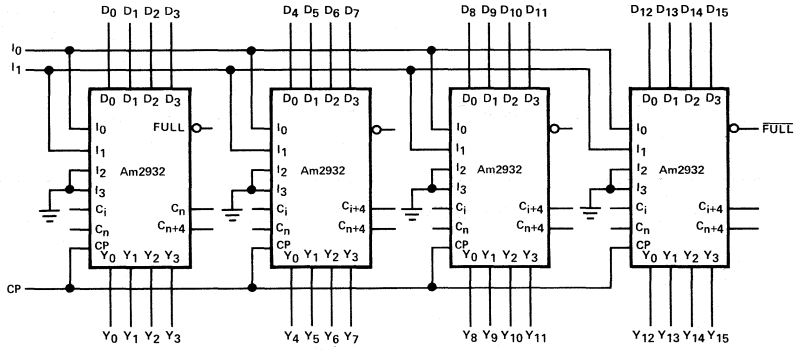
C_{i+4} The carry-out of the program counter incrementer.

Y_{0-3} The four address outputs of the Am2932. These are three-state output lines. When enabled, they display the outputs of the Full Adder.

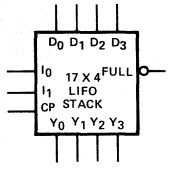
D_{0-3} The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.

$\overline{Full}$ The Full output is LOW when the LIFO stack is full – during and after the 17th push operation.

CP The clock input to the Am2932. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.



I_1	I_0	INSTRUCTION	Y OUTPUTS
L	L	RESET	"0"
L	H	SUSPEND	Z (HIGH IMPEDANCE)
H	L	PUSH D	SEE NOTE 1
H	H	POP S	TOP OF STACK



BLI-099

Equivalent Logic Symbol for Am2932 with I_2, I_3 Grounded

Figure shows the use of four Am2932s as a 17-word by 16-bit LIFO stack by grounding I_2 and I_3. The effect of grounding I_3 is shown in Figure 3.

Note 1. During this instruction, PC is placed on the Y outputs. If C_i is held LOW, the Y outputs will be LOW for this instruction after the device is initialized with a Reset instruction.

Figure 2. Application of Four Am2932s as a 17-Word by 16-Bit LIFO Stack.

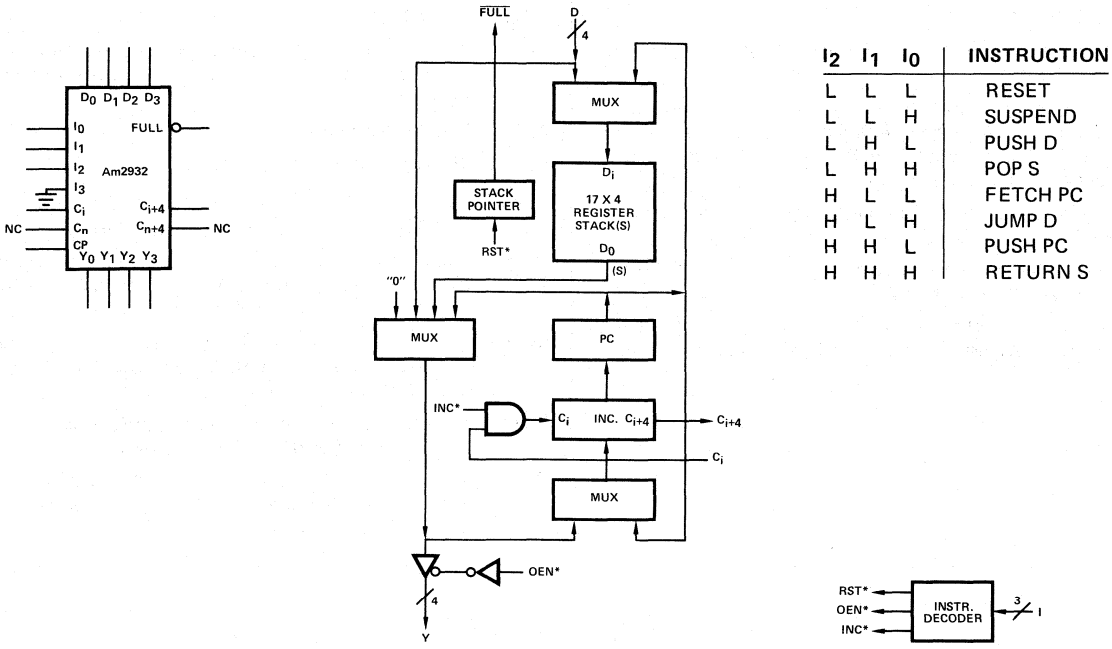


Figure 3. Equivalent Circuit of Am2932 with I_3 Grounded.

BLI-100

ORDERING INFORMATION

Am2932 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2932DC	D-20	C	C-1
AM2932DC-B	D-20	C	B-2 (Note 4)
AM2932DM	D-20	M	C-3
AM2932DMB	D-20	M	B-3
AM2932XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2932XM	Dice	M	

Notes:

1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V
   M = −55 to +125°C, V_{CC} = 4.50 to 5.50V
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2940
DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- DMA Address Generation
  Generates memory address, word count and DONE signal for DMA transfer operation.
- Expandable Eight-bit Slice
  Any number of Am2940's can be cascaded to form larger memory addresses – three devices address 16 megawords.
- Repeat Data Transfer Capability
  Initial memory address and word count are saved so that the data transfer can be repeated.
- Programmable Control Modes
  Provides four types of DMA transfer control plus memory address increment/decrement.
- High Speed, Bipolar LSI
  Advanced Low-Power Schottky TTL technology provides typical CLOCK to DONE propagation delay of 50ns and 24mA output current sink capability.
- Microprogrammable
  Executes 8 different instructions.

GENERAL DESCRIPTION

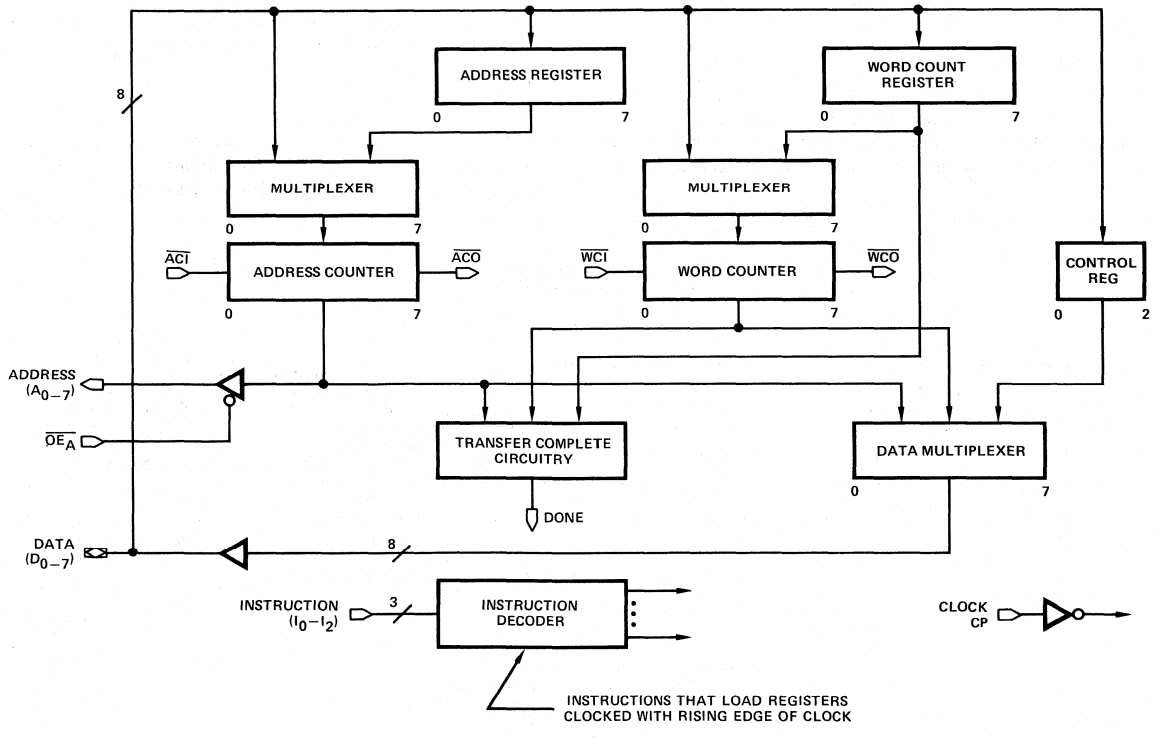
The Am2940, a 28-pin member of Advanced Micro Devices Am2900 family of Low-Power Schottky bipolar LSI chips, is a high-speed, cascadable, eight-bit wide Direct Memory Access Address Generator slice. Any number of Am2940's can be cascaded to form larger addresses.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

The Am2940 can be programmed to increment or decrement the memory address in any of four control modes, and executes eight different instructions. The initial address and word count are saved internally by the Am2940 so that they can be restored later in order to repeat the data transfer operation.

6

BLOCK DIAGRAM



Am2940 DMA Address Generator MPR-226

Am2940 ARCHITECTURE

As shown in the Block Diagram, the Am2940 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- Three-state address output buffers with external output enable control.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2940 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs A_0-A_7 under control of the Output Enable input, $\overline{OE}_A$.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D_0-D_7. The Data Multiplexer and three-state Data output buffers are instruction controlled.

Address Output Buffers

The three-state Address Output Buffers allow the Address Counter output to be enabled onto the ADDRESS lines, A_0-A_7, under external control. When the Output Enable input, $\overline{OE}_A$, is LOW, the Address output buffers are enabled; when $\overline{OE}_A$ is HIGH, the ADDRESS lines are in the high-impedance state. The address and Data Output Buffers can sink 24mA output current over the commercial operating range.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_2 and Control Register bits 0 and 1.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

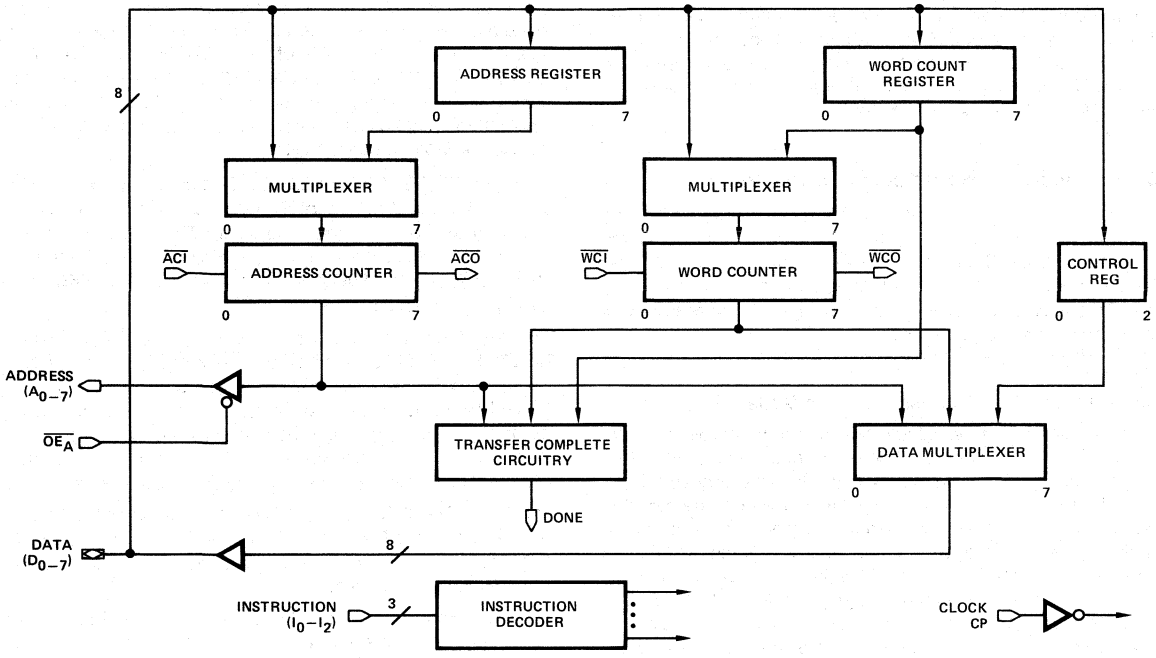
CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

H = HIGH
L = LOW

CR_2	Address Counter
L	Increment
H	Decrement

Figure 1. Control Register Format Definition.

BLOCK DIAGRAM



Am2940 DMA Address Generator

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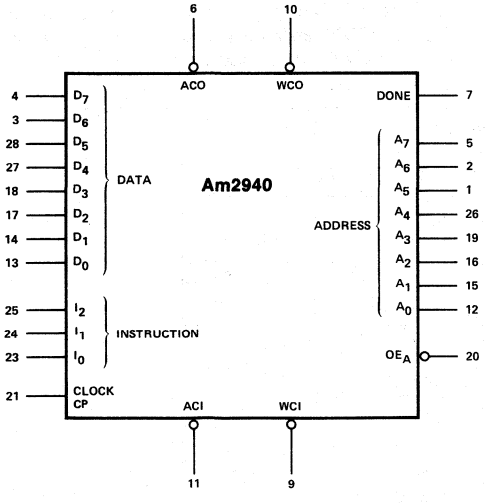
LOGIC SYMBOL



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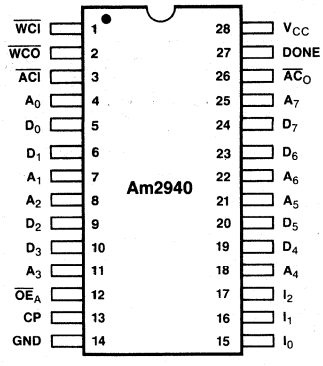
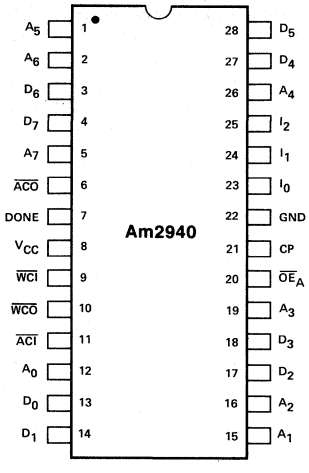
CONNECTION DIAGRAMS
Top Views

Flat Pack



MPR-586

DIP



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Note: Pin 1 is marked for orientation

Am2940 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, WCI, is LOW, the Word Counter decrements on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

Am2940 INSTRUCTIONS

The Am2940 instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register, one instruction enables the Address and Word counters, and one instruction reinitializes the Address and Word Counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 1 defines the Am2940 Instructions as a function of Instruction inputs I_0-I_2 and the four Am2940 Control Modes.

The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D_0-D_2. DATA lines D_3-D_7 are in the HIGH state during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA lines D_0-D_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA lines D_0-D_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

TABLE I. Am2940 INSTRUCTIONS

I_2 I_1 I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
L L L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-D_2→CR	INPUT
L L H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D_0-D_2 (Note 1)
L H L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
L H H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
H L L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
				1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
H L H	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
H H L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
				1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
H H H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
				2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.
AR = Address Reg.
AC = Address Counter
WCR = Word Count Reg.
WC = Word Counter
D = Data
L = LOW
H = HIGH
Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

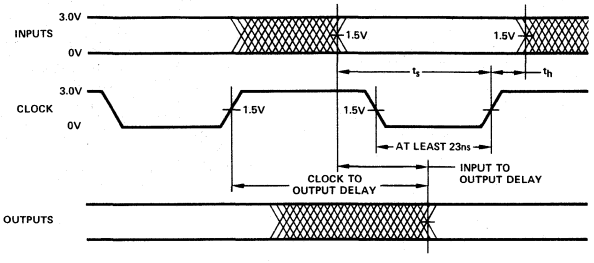
OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2940PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V MAX. = 5.25V)
Am2940DM, FM	MIL	T_C = −55° to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		MIL I_{OH} = −1.0mA	2.4			Volts
				COM'L I_{OH} = −2.6mA				
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL} (Note 5)	WCO, ACO	MIL I_{OL} = 8.0mA			0.5	Volts
				COM'L I_{OL} = 12mA				
			A_{0-7}, D_{0-7} DONE	MIL I_{OL} = 16mA				
				COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		D_{0-7}			−0.15	mA
				All Others			−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		D_{0-7}			150	µA
				All Others			40	
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX., V_O = 5.5V					250	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V	A_{0-7}			−50	µA
				D_{0-7}			−150	
I_{OZH}			V_{OUT} = 2.4V	A_{0-7}			50	
				D_{0-7}			150	
I_{CC}	Power Supply Current	V_{CC} = MAX.		T_A = 25°C		170	275	mA
			Am2940PC, DC	T_A = 0°C to +70°C			290	
				T_A = +70°C			235	
			Am2940DM, FM	T_C = −55°C to +125°C			315	
				T_C = +125°C			225	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. I_{OL} limit on A_i and D_i (i = 0 to 7) applies to either output individually, but not both at the same time. The sum of the loading on A_i plus D_i is limited to 24mA MIL or 32mA COM'L.



See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Figure 2. Switching Waveforms.

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SWITCHING CHARACTERISTICS

The tables below define the Am2940 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times ($\overline{OE}$ to A and I to D) which are specified for a 5pF load. All times are in ns.

I. TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	13	3
I_{012}	33	2
$\overline{ACI}$	15	2
$\overline{WCI}$ (Note 1)	15	1

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	12	–	–	–	–
$\overline{WCI}$ (Note 2)	–	12	–	27	–
I_{0-2}	–	–	–	–	21
CP (Note 3)	35	35	35	50	–

C. Clock Requirements

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	25	ns
Maximum Clock Frequency		MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	25	19	ns
$\overline{OE}$	A_{0-7}	19	13	ns

II. GUARANTEED ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	21	4
I_{012}	41	3
$\overline{ACI}$	27	3
$\overline{WCI}$ (Note 1)	27	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	18	–	–	–	–
$\overline{WCI}$ (Note 2)	–	18	–	41	–
I_{0-2}	–	–	–	–	34
CP (Note 3)	50	50	48	77	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	30	ns
Maximum Clock Frequency		MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	30	30	ns
$\overline{OE}$	A_{0-7}	23	23	ns

III. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE
Am2940PC, DC (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	5
I_{012}	46	4
$\overline{ACI}$	30	4
$\overline{WCI}$ (Note 1)	30	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	20	–	–	–	–
$\overline{WCI}$ (Note 2)	–	20	–	46	–
I_{0-2}	–	–	–	–	37
CP (Note 3)	58	58	54	85	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	35	35	ns
$\overline{OE}$	A_{0-7}	25	25	ns

IV. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE
Am2940DM, FM (T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	6
I_{012}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$ (Note 1)	34	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	21	–	–	–	–
$\overline{WCI}$ (Note 2)	–	21	–	54	–
I_0-I_2	–	–	–	–	41
CP (Note 3)	64	64	62	88	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency		MHz

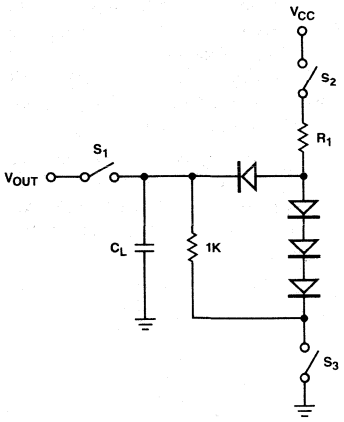
D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	42	42	ns
$\overline{OE}$	A_{0-7}	30	30	ns

Notes: 1. Control modes 0, 1, and 3 only.
2. WCI to Done occurs only in control modes 0 and 1.
3. CP to Done occurs only in control modes 0, 1, and 2.

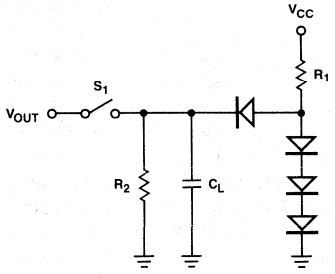
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2940

A. THREE STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

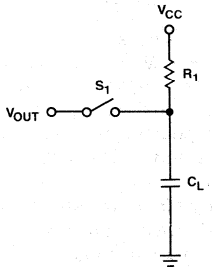
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2940

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	A_{0-7}	A	220	1K
–	D_{0-7}	A	220	1K
6	$\overline{ACO}$	B	470	2.4K
7	DONE	C	270	–
10	$\overline{WCO}$	B	470	2.4K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS

The Am2940 is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory. One or more Am2940's can be used in each peripheral controller of a distributed DMA system to provide the memory address and word count required for DMA operation.

Figure 3 shows a block diagram of an example microprogrammed DMA peripheral controller. The Am2910 Microprogram Sequencer, Microprogram Memory, and the Microinstruction Register form the microprogram control portion of this peripheral controller. The Am2940 generates the memory address and maintains the word count required for DMA operation. An internal three-state bus provides the communication path between the Microinstruction Register, the Am2917 Data Transceivers, the Am2940, the Am2901A Microprocessor, and the Device Interface Circuitry.

The Am2940 interconnections are shown in detail in Figure 4. Two Am2940's are cascaded to generate a sixteen-bit address. The Am2940 ADDRESS and DATA output current sink capability is 24mA over the commercial operating range. This allows the Am2940's to drive the System Address Bus and Internal Three-State Bus directly, thereby eliminating the need for separate bus drivers. Three-bits in the Microinstruction Register provide the Am2940 Instruction Inputs, I_0-I_2. The microprogram clock is used to clock the Am2940's and, when the ENABLE COUNTERS instruction is applied, address and word counting is controlled by the CNT bit of the Microinstruction Register.

Asynchronous interface control circuitry generates System Bus control signals and enables the Am2940 Address onto the System Address Bus at the appropriate time. The open-collector DONE outputs are dot-anded and used as a test input to the Am2910 Microprogram Sequencer.

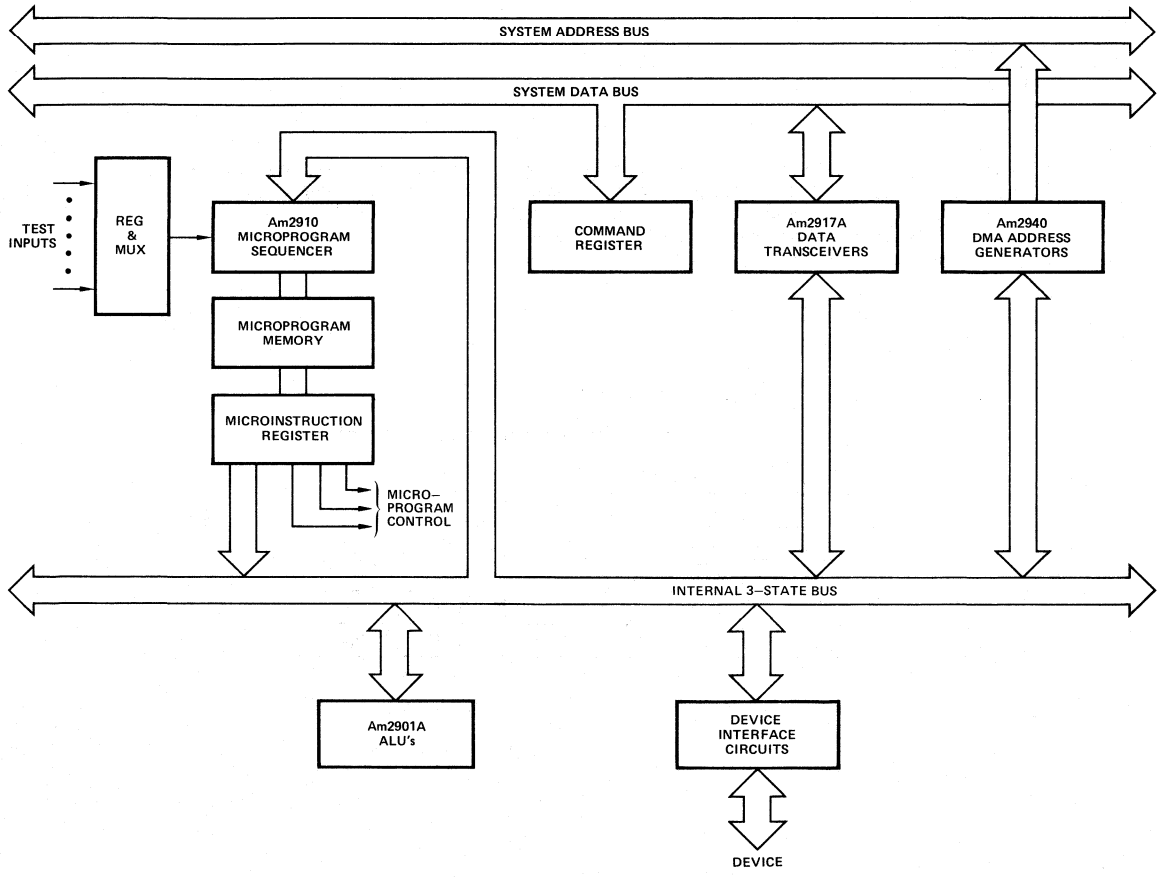


Figure 3. DMA Peripheral Controller Block Diagram.

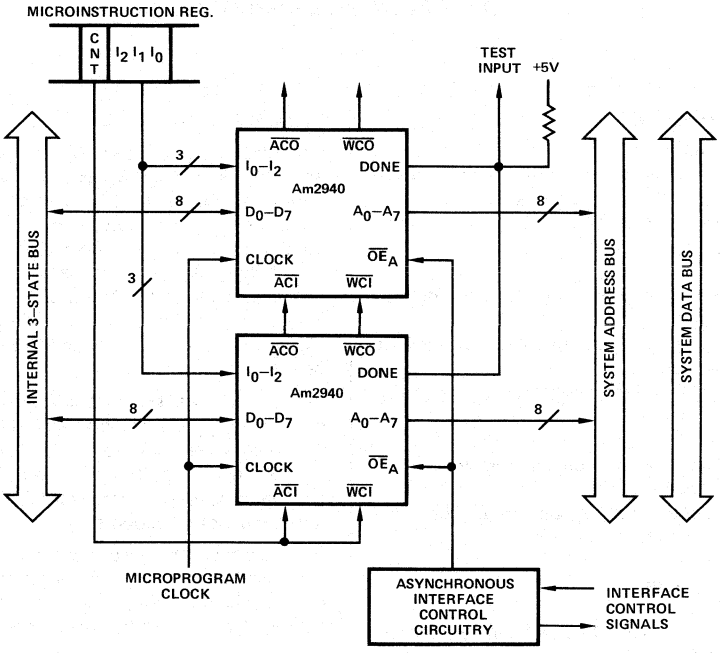


Figure 4. Am2940 Interconnections.

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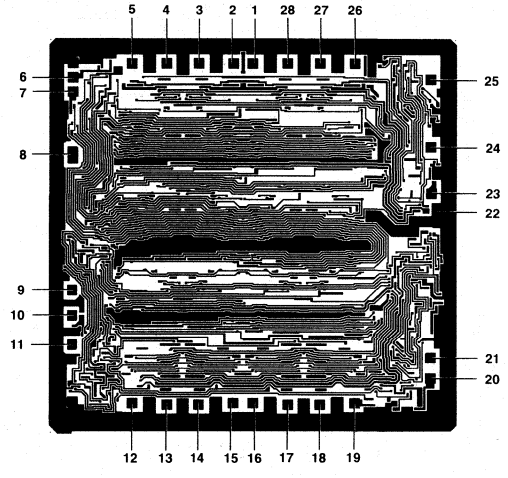
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2940PC	P-28	C	C-1
AM2940DC	D-28	C	C-1
AM2940DC-B	D-28	C	B-2 (Note 4)
AM2940DM	D-28	M	C-3
AM2940DM-B	D-28	M	B-3
AM2940FM	F-28-2	M	C-3
AM2940FM-B	F-28-2	M	B-3
AM2940XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2940XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

METALLIZATION AND PAD LAYOUT



Note: Numbers refer to DIP pin connections.

DIE SIZE: 0.178" X 0.181"

Am2942

Programmable Timer/Counter DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- 22-pin version of Am2940 –
  Provides multiplexed Address and Data lines plus additional Instruction Input and Instruction Enable pins.
- Can be used as either DMA Address Generator or Programmable Timer Counter.
- Executes 16 instructions –
  Eight DMA instructions plus eight Timer/Counter instructions
- Provides two independent programmable 8-bit up/down counters in a 22-pin package –
  Counters can be cascaded to form single-chip 16-bit up/down counter.
- Reinitialize capability –
  Counters can be reinitialized from on-chip registers.
- Expandable eight-bit slice –
  Any number of Am2942s can be cascaded. Three devices provide a 48 bit counter.
- Programmable control modes –
  Provide four types of control.
- High speed bipolar LSI –
  Advanced Low-Power Schottky TTL technology provides typical count frequency of 25MHz and 24mA output current sink capability.

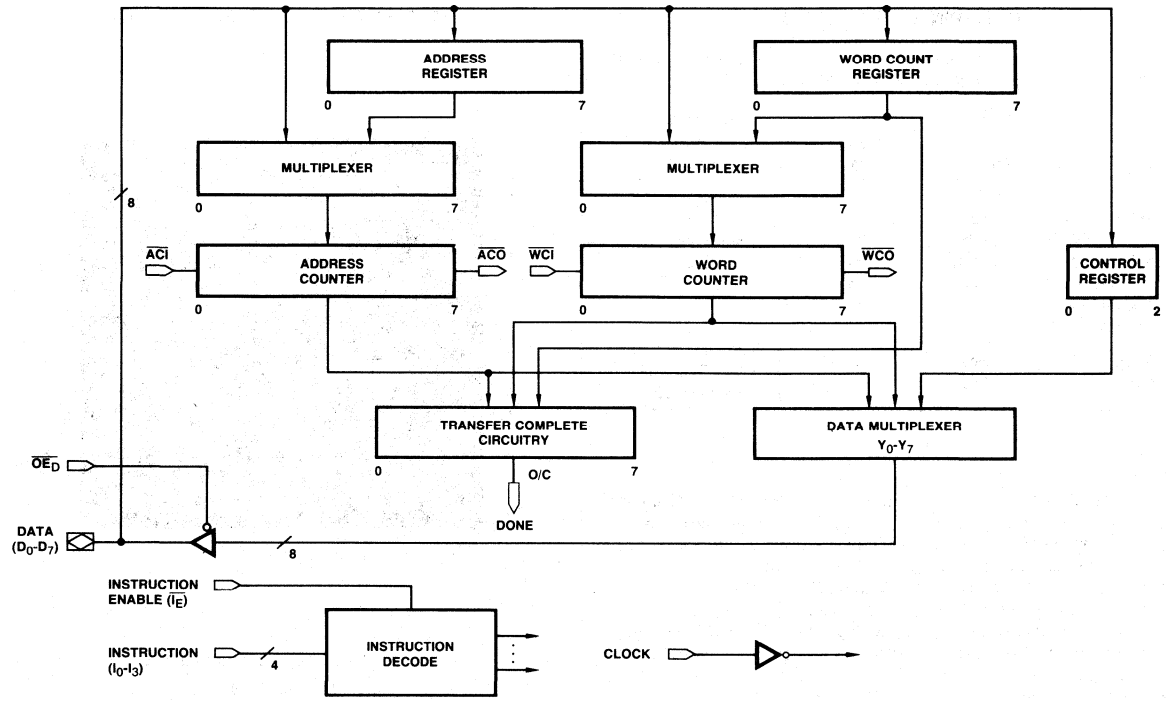
GENERAL DESCRIPTION

The Am2942, a 22-pin version of the Am2940, can be used as a high-speed DMA Address Generator or Programmable Timer/Counter. It provides multiplexed Address and Data lines, for use with a common bus, and additional Instruction Input and Instruction Enable pins. The Am2942 executes 16 instructions; eight are the same as the Am2940 instructions, and eight instructions facilitate the use of the Am2942 as a Programmable Timer/Counter. The Instruction Enable input allows the sharing of the Am2942 instruction field with other devices.

When used as a Timer/Counter, the Am2942 provides two independent, programmable, eight-bit, up-down counters in a 22-pin package. The two on-chip counters can be cascaded to form a single chip, 16-bit counter. Also, any number of chips can be cascaded – for example three cascaded Am2942s form a 48-bit timer/counter.

Reinitialization instructions provide the capability to reinitialize the counters from on-chip registers. Am2942 Programmable Control Modes, identical to those of the Am2940, offer four different types of programmable control.

BLOCK DIAGRAM



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Am2942 ARCHITECTURE

As shown in the Block Diagram, the Am2942 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2942 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, and decrements in Control Modes 0 and 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, three-input multiplexer which allows the Address Counter, Word Counter and Control Register to be read at DATA lines D_0-D_7. The Data Multiplexer output, Y_0-Y_7, is enabled onto DATA lines D_{0-7} if and only if the Output Enable input, $\overline{OE}_D$, is LOW. (Refer to Figure 2.)

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_3 Control Register bits 0 and 1, and the INSTRUCTION ENABLE input, $\overline{I}_E$.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Decrement	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

H = HIGH
L = LOW

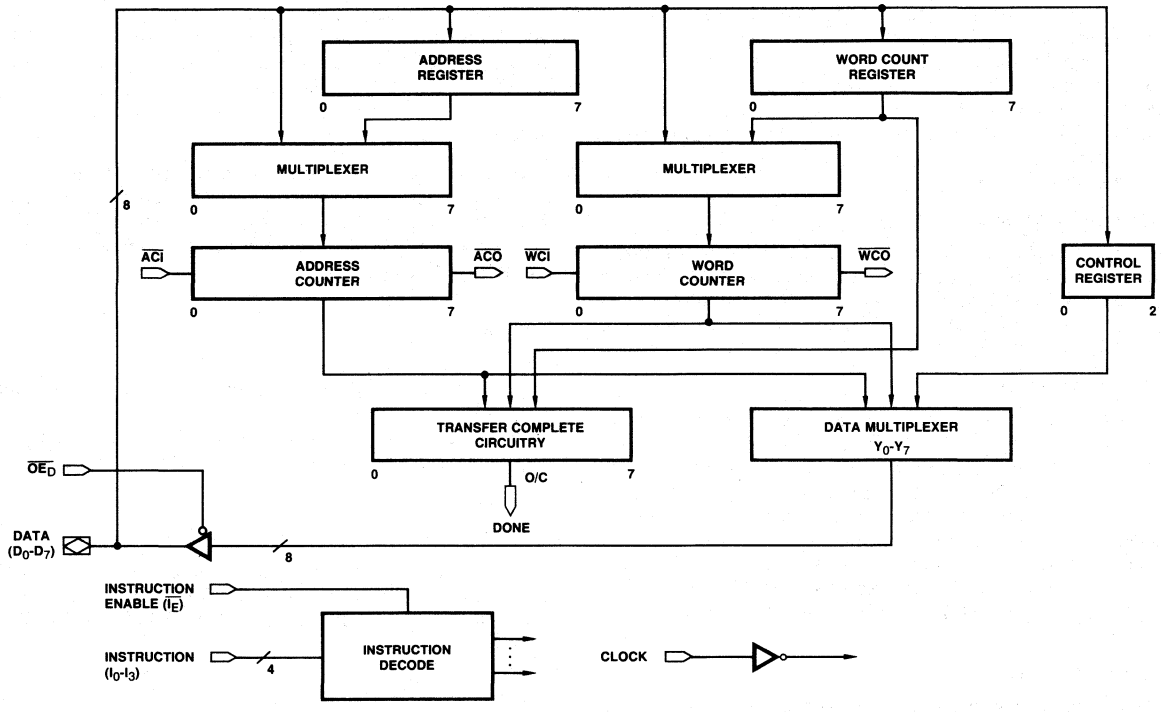
CR_2	Address Counter
L	Increment
H	Decrement

Figure 1. Control Register Format Definition.

$\overline{OE}_D$	D_0-D_7
L	DATA MULTIPLEXER OUTPUT, Y_0-Y_7
H	HIGH Z

Figure 2. Data Bus Output Enable Function.

BLOCK DIAGRAM



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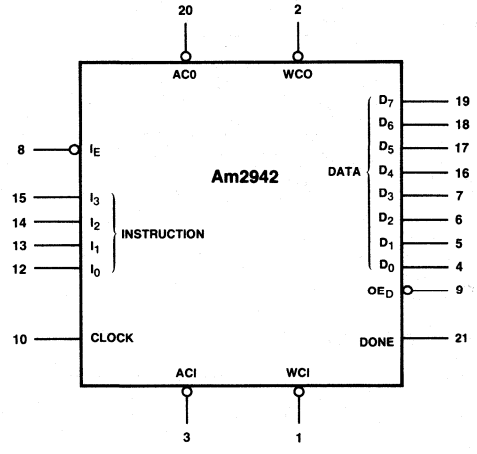
LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

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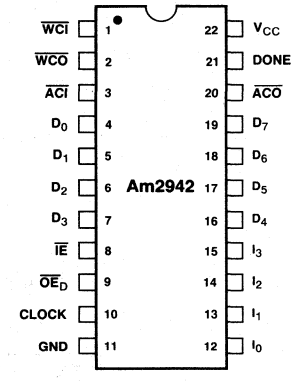
CONNECTION DIAGRAM
Top View

DIP AND FLATPACK



Note: Pin 1 is marked for orientation.

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Am2942 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter decrements on the LOW to HIGH transition of the CLOCK input, CP. Figure 1 specifies when the DONE signal is generated in this mode.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

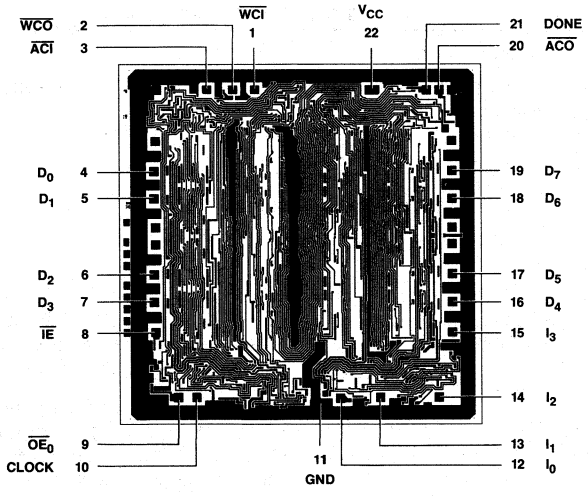
Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need to be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.181" X 0.178"

Am2942 INSTRUCTIONS

The Am2942 instruction set consists of sixteen instructions. Eight are DMA Instructions and are similar to the Am2940 instructions. The remaining eight instructions are designed to facilitate the use of the Am2942 as a Programmable Timer/Counter. Figures 3 and 4 define the Am2942 Instructions.

Instructions 0-7 are DMA instructions. The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register to Data Multiplexer outputs Y_0-Y_2. Outputs Y_3-Y_7 are HIGH during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter to Data Multiplexer outputs, Y_0-Y_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter to Data Multiplexer outputs, Y_0-Y_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

When $\overline{I_E}$ is HIGH, Instruction inputs, I_0-I_2, are disabled. If I_3 is LOW, the function performed is identical to that of the ENABLE COUNTERS instruction. Thus, counting can be controlled by the carry inputs with the ENABLE COUNTERS instruction applied or with Instruction Inputs I_0-I_2 disabled.

Instructions 8-F facilitate the use of the Am2942 as a Programmable Timer/Counter. They differ from instructions 0-7 in that they provide independent control of the Address Counter, Word Counter and Control Register.

The WRITE CONTROL REGISTER, T/C instruction writes DATA input D_0-D_2 into the Control Register. DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The Address and Word Counters are enabled, and the Control Register contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS COUNTER instruction allows the independent reinitialization of the Address Counter. The Word Counter is enabled and the contents of the Address Counter appear at the Data Multiplexer output.

$\overline{I_E}$	I_3	I_2	I_1	I_0	HEX CODE		
0	0	0	0	0	0	WRITE CONTROL REGISTER	DMA INSTRUCTIONS
0	0	0	0	1	1	READ CONTROL REGISTER	
0	0	0	1	0	2	READ WORD COUNTER	
0	0	0	1	1	3	READ ADDRESS COUNTER	
0	0	1	0	0	4	REINITIALIZE COUNTERS	
0	0	1	0	1	5	LOAD ADDRESS	
0	0	1	1	0	6	LOAD WORD COUNT	
0	0	1	1	1	7	ENABLE COUNTERS	
1	0	X	X	X	0-7	INSTRUCTION DISABLE	
0	1	0	0	0	8	WRITE CONTROL REGISTER, T/C	TIMER/COUNTER INSTRUCTIONS
0	1	0	0	1	9	REINITIALIZE ADDRESS COUNTER	
0	1	0	1	0	A	READ WORD COUNTER, T/C	
0	1	0	1	1	B	READ ADDRESS COUNTER, T/C	
0	1	1	0	0	C	REINITIALIZE ADDRESS & WORD COUNTERS	
0	1	1	0	1	D	LOAD ADDRESS, T/C	
0	1	1	1	0	E	LOAD WORD COUNT, T/C	
0	1	1	1	1	F	REINITIALIZE WORD COUNTER	
1	1	X	X	X	8-F	INSTRUCTION DISABLE, T/C	

0 = LOW 1 = HIGH X = DON'T CARE

Notes: 1. When I_3 is tied LOW, the Am2942 acts as a DMA circuit: When I_3 is tied HIGH, the Am2942 acts as a Timer/Counter circuit.
2. Am2942 instructions 0 through 7 are the same as Am2940 instructions.

Figure 3. Am2942 Instructions.

The Word Counter can be read, using the READ WORD COUNTER, T/C instruction. Both counters are enabled when this instruction is executed.

When the READ ADDRESS COUNTER, T/C instruction is executed, both counters are enabled and the address counter contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS and WORD COUNTERS instruction provides the capability to reinitialize both counters at the same time. The Address Counter contents appear at the Data Multiplexer output.

DATA inputs D_0-D_7 are loaded into both the Address Register and Counter when the LOAD ADDRESS, T/C instruction is executed. The Word Counter is enabled and its contents appear at the Data Multiplexer output.

The LOAD WORD COUNT, T/C instruction is identical to the LOAD WORD COUNT instruction with the exception that Address Counter is enabled.

The Word Counter can be independently reinitialized using the REINITIALIZE WORD COUNTER instruction. The Address Counter is enabled and the Word Counter contents appear at the Data Multiplexer output.

When the $\overline{I_E}$ input is HIGH, Instruction inputs, I_0-I_2, are disabled. The function performed when I_3 is HIGH is identical to that performed when I_3 is LOW, with the exception that the Word Counter contents appear at the Data Multiplexer output.

$\overline{I_E}$	$I_3I_2I_1I_0$ (Hex)	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Adr. Reg.	Adr. Counter	Control Reg.	Data Multiplexer Output
L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	$D_{0-2} \rightarrow$ CR	FORCED HIGH
L	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CONTROL REG.
L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WORD COUNTER
L	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	ADR. COUNTER
L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D → AR	D → AC	HOLD	WORD COUNTER
L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D → WR	D → WC	HOLD	HOLD	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	HOLD	HOLD	FORCED HIGH
L	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
H	0-7	INSTRUCTION DISABLE	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
L	8	WRITE CONTROL REGISTER, T/C	WCRT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	$D_{0-2} \rightarrow$ CR	CONTROL REG.
L	9	REINITIALIZE ADR. COUNTER	REAC	0, 1, 2, 3	HOLD	ENABLE	HOLD	AR → AC	HOLD	ADR. COUNTER
L	A	READ WORD COUNTER, TC	RWCT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WORD COUNTER
L	B	READ ADDRESS COUNTER, T/C	RACT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. COUNTER
L	C	REINITIALIZE ADDRESS AND WORD COUNTERS	RAWC	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	D	LOAD ADDRESS, T/C	LDAT	0, 1, 2, 3	HOLD	ENABLE	D → AR	D → AC	HOLD	WORD COUNTER
L	E	LOAD WORD COUNT, T/C	LWCT	0, 2, 3	D → WR	D → WC	HOLD	ENABLE	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	ENABLE	HOLD	FORCED HIGH
L	F	REINITIALIZE WORD COUNTER	REWC	0, 2, 3	HOLD	WR → WC	HOLD	ENABLE	HOLD	WD. CNTR.
				1	HOLD	ZERO → WC	HOLD	ENABLE	HOLD	WD. CNTR.
H	8-F	INSTRUCTION DISABLE, T/C	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WD. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	WD. CNTR.

WR = WORD REGISTER
WC = WORD COUNTER
AR = ADDRESS REGISTER
AC = ADDRESS COUNTER
CR = CONTROL REGISTER
D = DATA

Figure 4. Am2942 Function Table.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

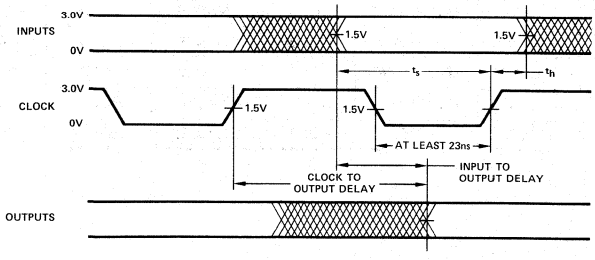
OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2942DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V MAX. = 5.25V)
Am2942DM, FM	MIL	T_C = −55° to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		MIL I_{OH} = −1.0mA	2.4			Volts
				COM'L I_{OH} = −2.6mA				
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	WCO, ACO	MIL I_{OL} = 8.0mA			0.5	Volts
				COM'L I_{OL} = 12mA				
			D_{0-7}, DONE	MIL I_{OL} = 16mA				
				COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		D_{0-7}			−0.15	mA
				All Others			−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		D_{0-7}			150	μA
				All Others			40	
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX., V_0 = 5.5V					250	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V	D_{0-7}			−150	μA
I_{OZH}			V_{OUT} = 2.4V	D_{0-7}			150	
I_{CC}	Power Supply Current	V_{CC} = MAX.		T_A = 25°C		155	250	mA
			Am2942PC, DC	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			Am2942DM, FM	T_C = −55°C to +125°C			285	
				T_C = +125°C			205	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.



See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Figure 5. Switching Waveforms.

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SWITCHING CHARACTERISTICS

The tables below define the Am2942 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times (I to D) which are specified for a 5pF load. All times are in ns.

I. TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	13	3
I_{0-3}	33	2
$\overline{ACI}$	15	2
$\overline{WCI}$	15	1
I_E	33	2

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	12	–	–	–
$\overline{WCI}$ (Note 1)	–	12	27	–
I_{0-3}	–	–	–	21
CP (Note 2)	35	35	50	37
I_E	–	–	–	21

C. Clock Requirements

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	30	ns
Maximum Clock Frequency	28	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	19	13	ns

II. GUARANTEED ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	21	4
I_{0-3}	41	3
$\overline{ACI}$	27	3
$\overline{WCI}$	27	3
I_E	41	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	18	–	–	–
$\overline{WCI}$ (Note 1)	–	18	41	–
I_{0-3}	–	–	–	34
CP (Note 2)	50	50	77	53
I_E	–	–	–	34

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	30	ns
Maximum Clock Frequency	22	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	23	23	ns

III. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2942PC, DC (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	6
I_{0-3}	46	5
$\overline{ACI}$	30	4
$\overline{WCI}$	30	3
I_E	46	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	20	–	–	–
$\overline{WCI}$ (Note 1)	–	20	46	–
I_{0-3}	–	–	–	37
CP (Note 2)	58	58	85	59
I_E	–	–	–	37

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	20	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	25	25	ns

IV. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2942DM, FM (T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	7
I_{0-3}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$	34	5
I_E	49	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	21	–	–	–
$\overline{WCI}$ (Note 1)	–	21	54	–
I_{0-3}	–	–	–	41
CP (Note 2)	64	64	88	68
I_E	–	–	–	41

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	15	MHz

D. Enable/Disable Times

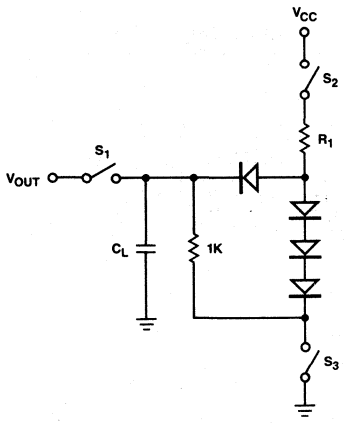
From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	30	30	ns

Notes: 1. $\overline{WCI}$ to Done occurs only in control modes 0 and 1.
2. CP to Done occurs only in control modes 0, 1, and 2.

6

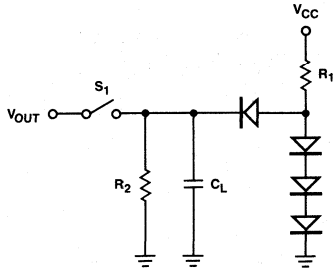
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2942

A. THREE STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

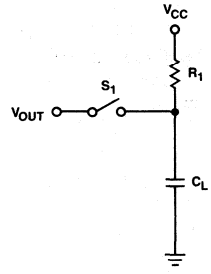
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2942

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	D_{0-7}	A	220	1K
20	$\overline{ACO}$	B	470	2.4K
21	DONE	C	270	–
2	$\overline{WCO}$	B	470	2.4K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS

Figure 6 shows an Am2942 used as two independent, programmable eight-bit timer/counters. In this example, an Am2910 Microprogram Sequencer provides an address to Am27S27 512 x 8 Registered PROMs. The on-chip PROM output register is used as the Microinstruction Register.

The Am2942 Instruction input, I_3, is tied HIGH to select the eight Timer/Counter instructions. The $\overline{I_E}$, I_0-I_2, and $\overline{OE_D}$ inputs are provided by the microinstruction, and the D_0-D_7 data lines are connected to a common Data Bus. GATE WC and GATE AC are separate enable controls for the respective Word Counter and Address Counter. The DONE, $\overline{ACO}$ and $\overline{WCO}$ output signals indicate that a pre-programmed time or count has been reached.

Figure 7 shows an Am2942 used as a single 16-bit programmable timer/counter. In this example, the Word Counter carry-out, $\overline{WCO}$, is connected to the Address Counter carry-in, $\overline{ACI}$, to form a single 16-bit counter which is enabled by the GATE signal.

Figure 8 shows two Am2942s cascaded to form a 32-bit programmable timer/counter. The two Word Counters form the low order 16 bits, and the two Address Counters form the high order bits. This allows the timer/counter to be loaded and read 16 bits at a time.

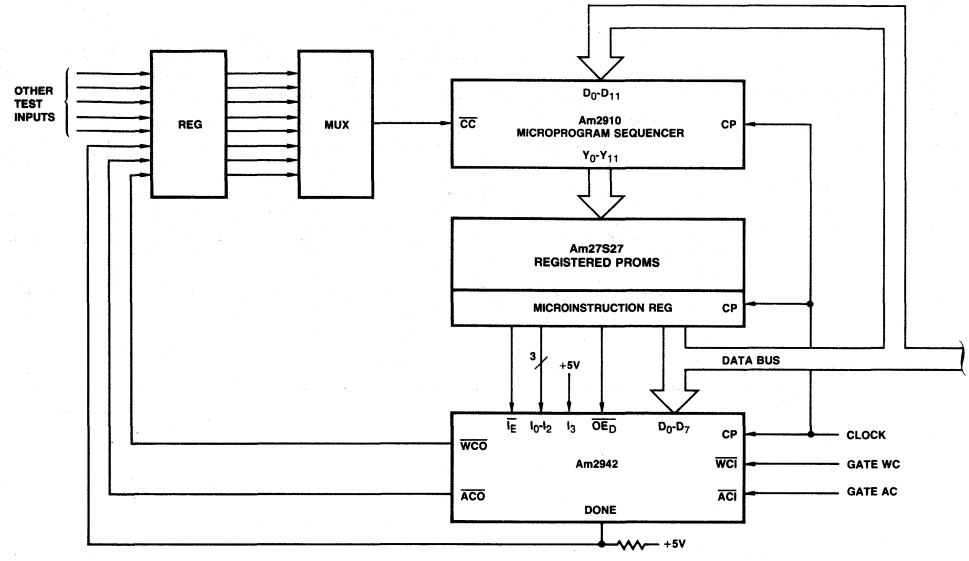


Figure 6. Two 8-Bit Programmable Counters/Timers in a 22-Pin Package.

MPR-234

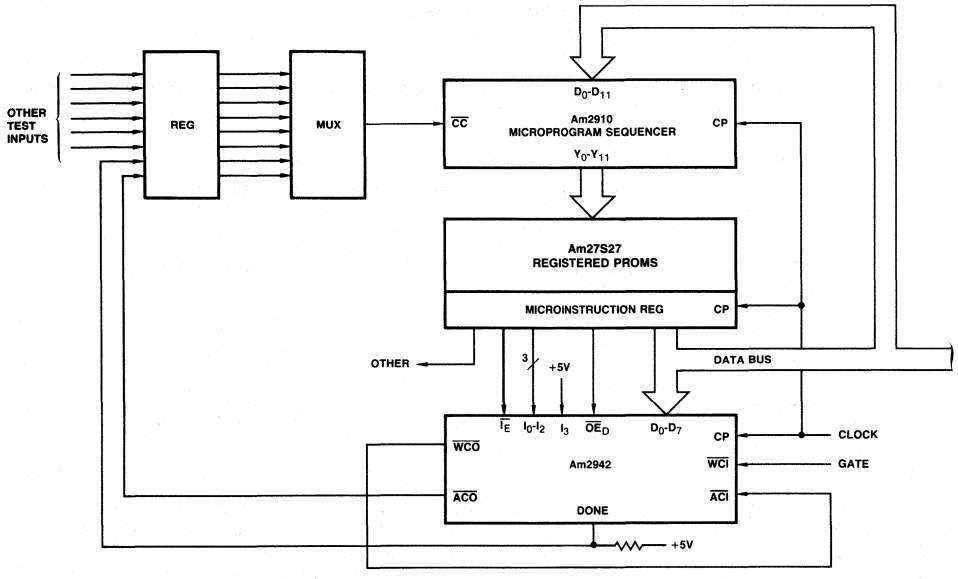


Figure 7. 16-Bit Programmable Counter/Timer Using a Single Am2942.

MPR-235

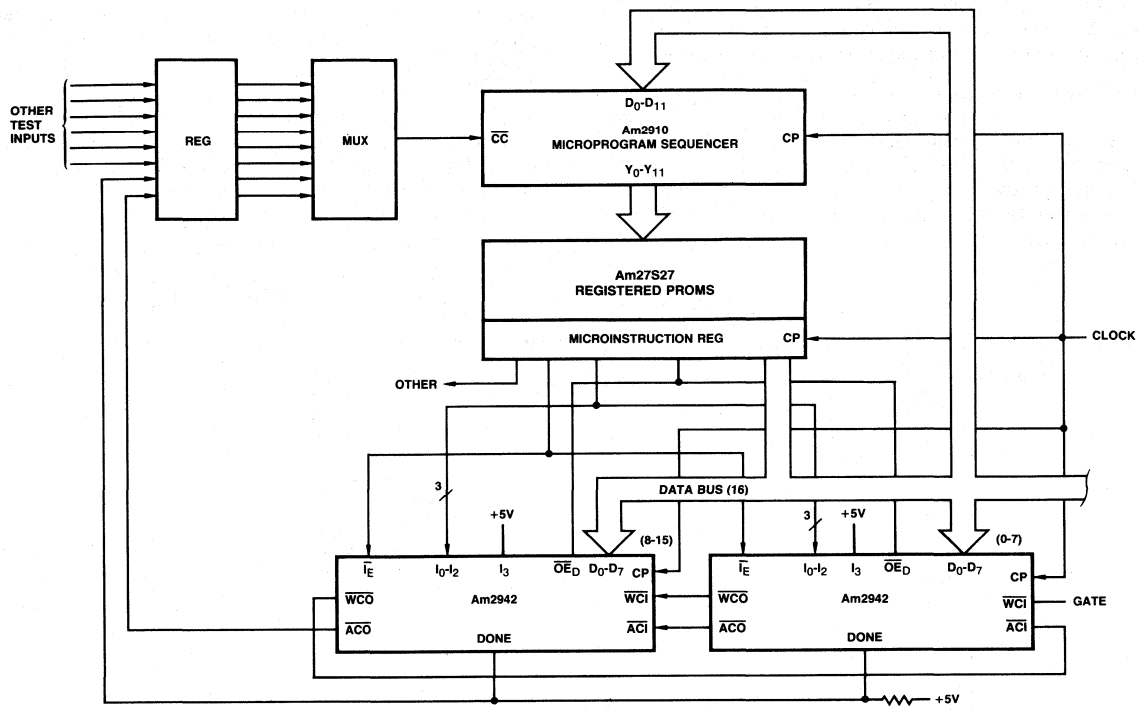


Figure 8. 32-Bit Programmable Counter/Timer Using Two Am2942s.

MPR-236

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2942DC	D-22	C	C-1
AM2942DC-B	D-22	C	B-2 (Note 4)
AM2942DM	D-22	M	C-3
AM2942DM-B	D-22	M	B-3
AM2942FM	F-22	M	C-3
AM2942FM-B	F-22	M	B-3
AM2942XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2942XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2946 • Am2947

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} – 1.15 V_{OH} interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- Am2946 inverting transceivers
- Am2947 noninverting transceivers
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20-pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

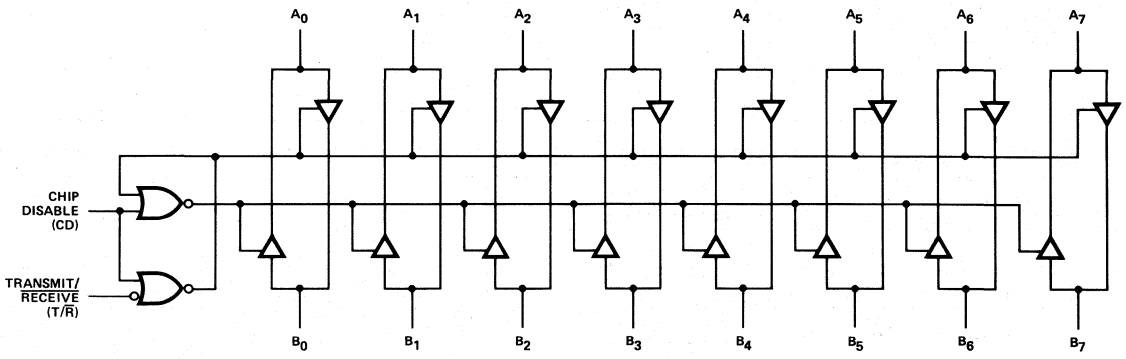
The Am2946 and Am2947 are 8-bit state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage (V_{OH}) is specified at V_{CC} – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

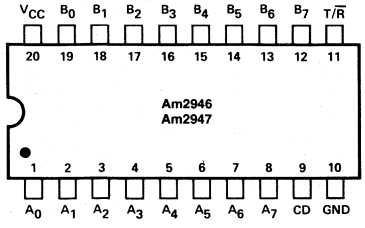
6

Am2947
LOGIC DIAGRAM



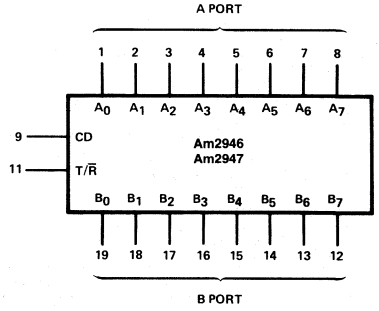
Am2946 has inverting transceivers.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientaton.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Am2946 • Am2947

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL	T_A = −55 to +125°C	V_{CC} MIN = 4.5V	V_{CC} MAX = 5.5V
COM'L	T_A = 0 to +70°C	V_{CC} MIN = 4.75V	V_{CC} MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
		A PORT (A_0-A_7)					
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.7		Volts
			I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OL} = 12mA		0.3	0.4	Volts
			COM'L I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			80	
		B PORT (B_0-B_7)					
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.8		Volts
			I_{OH} = −5.0mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_O = 0V V_{CC} = MAX, Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			200	
		CONTROL INPUTS CD, T/$\overline{R}$					
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage		COM'L			0.8	Volts
			MIL			0.7	
I_{IH}	Logical "1" Input Current	V_I = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX, V_I = V_{CC} MAX				1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.1	−0.25	
V_C	Input Clamp Voltage	I_{IN} = −12mA			−0.8	−1.5	Volts
		POWER SUPPLY CURRENT					
I_{CC}	Power Supply Current	Am2946	CD = V_I = 2.0V, V_{CC} = MAX		70	100	mA
			CD = 0.4V, V_{INA} = T/$\overline{R}$ = 2.0V, V_{CC} = MAX		100	150	
		Am2947B	CD = 2.0V, V_I = 0.4V, V_{CC} = MAX		70	100	mA
			CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2.0V, V_{CC} = MAX		90	140	

Am2946
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	19	25	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	7	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	22	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	23	33	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	22	33	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	26	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	27	35	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

FUNCTION TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{Receive}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

Am2946

AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am2946 COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Max	Am2946 MIL T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	16	19	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	20	23	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	28	33	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	24	29	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	16	19	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	25	30	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	19	22	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	23	26	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	38	43	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	26	30	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	38	43	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	38	43	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	38	43	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	41	47	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	41	47	ns

Am2947
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	19	25	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	26	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	28	38	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	28	38	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	31	40	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	31	40	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is LOW and are transmit inputs when T/$\overline{R}$ is HIGH.

B_0-B_7 B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW.

CD Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$).

T/$\overline{R}$ Transmit/$\overline{\text{Receive}}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH A port is the input and B port is the output. With T/$\overline{R}$ LOW A port is the output and B port is the input.

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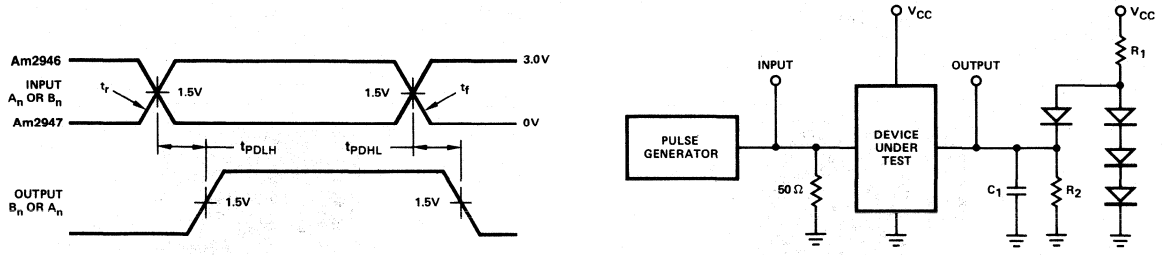
Am2947

AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am2947 COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Max	Am2947 MIL T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	21	24	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	21	24	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	28	33	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	28	34	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	25	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	28	34	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	25	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	23	26	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	38	43	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	26	30	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	38	43	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	42	48	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	42	48	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	45	51	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	45	51	ns

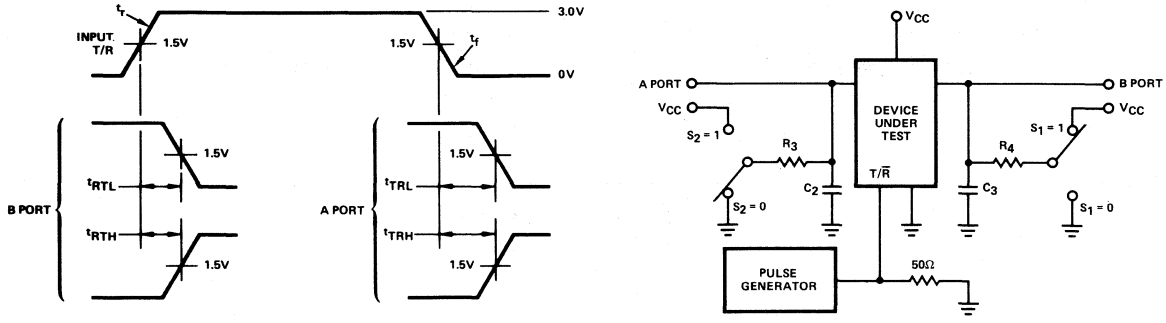
SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



$t_r = t_f < 10ns$
10% to 90%

Note: C_1 includes test fixture capacitance.

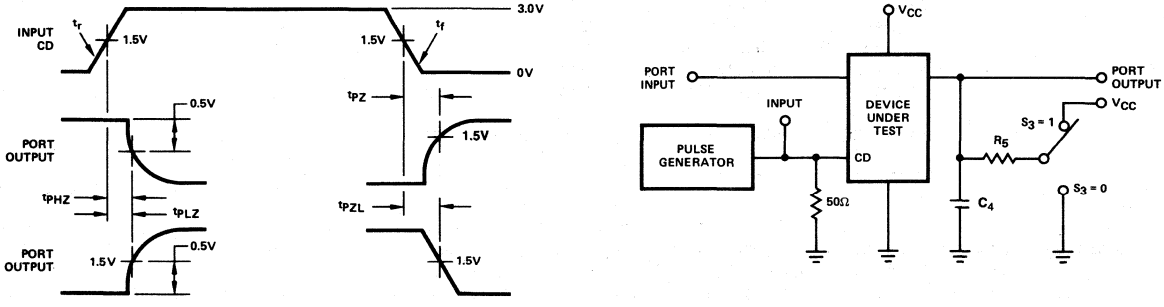
Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.



$t_r = t_f < 10ns$
10% to 90%

Note: C_2 and C_3 include test fixture capacitance.

Figure 2. Propagation Delay from T/$\overline{R}$ to A Port or B Port.



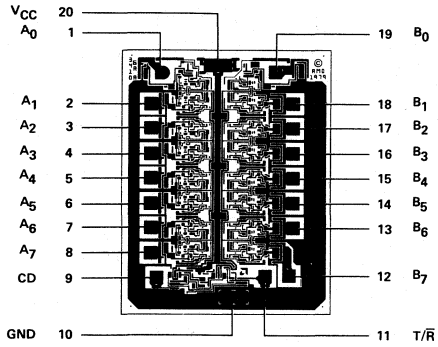
$t_r = t_f < 10ns$
10% to 90%

Note: C_4 includes test fixture capacitance.
Port input is in a fixed logical condition.

Figure 3. Propagation Delay from CD to A Port or B Port.

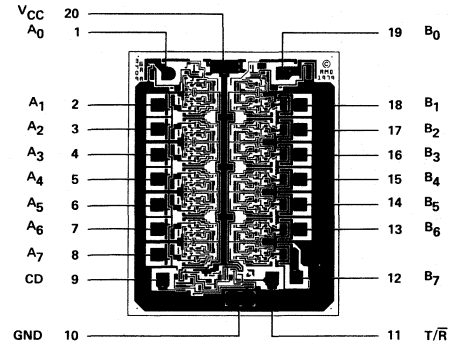
Metallization and Pad Layouts

Am2946



DIE SIZE .069" X .089"

Am2947



DIE SIZE .069" X .089"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2946 Order Number	Am2947 Order Number	Package Type (Note 1)	Operating (Note 2)	Screening Level (Note 3)
AM2946PC	AM2947PC	D-20-1	C	C-1
AM2946DC	AM2947DC	D-20-1	C	C-1
AM2946DC-B	AM2947DC-B	D-20-1	C	B-1
AM2946DM	AM2947DM	D-20-1	M	C-3
AM2946DM-B	AM2947DM-B	D-20-1	M	B-3
AM2946XC	AM2947XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2948 • Am2949

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} – 1.15V V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- Am2948 has inverting tranceivers
- Am2949 has noninverting transceivers
- Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

GENERAL DESCRIPTION

The Am2948 and Am2949 are 8-bit, 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables are provided for microprocessor system with separated read and write control bus lines.

The output high voltage (V_{OH}) is specified at V_{CC} – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

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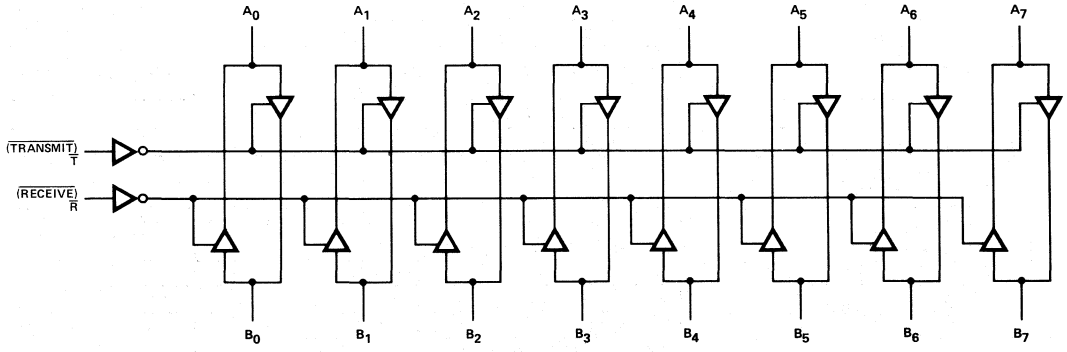
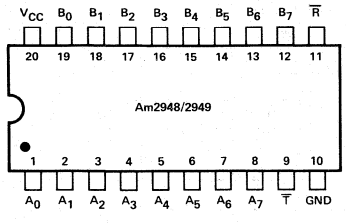
Am2949
LOGIC DIAGRAM



Am2948 has inverting transceivers.

BLI-177

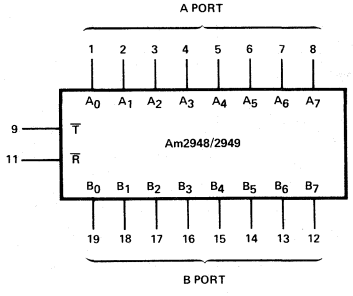
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
Am2948 is inverting from Ai to Bi

BLI-108

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

BLI-109

Am2948 • Am2949

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL	T_A = −55 to +125°C	V_{CC} MIN = 4.5V	V_{CC} MAX = 5.5V
COM'L	T_A = 0 to +70°C	V_{CC} MIN = 4.75V	V_{CC} MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description		Test Conditions			Min	Typ (Note 1)	Max	Units
A PORT (A_0-A_7)									
V_{IH}	Logical "1" Input Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V			2.0			Volts
V_{IL}	Logical "0" Input Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V		COM'L			0.8	Volts
					MIL			0.7	
V_{OH}	Logical "1" Output Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.7		Volts
				I_{OH} = −3.0mA		2.7	3.95		
V_{OL}	Logical "0" Output Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OL} = 12mA			0.3	0.4	Volts
				COM'L	I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2			−10	−38	−75	mA
I_{IH}	Logical "1" Input Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V				−200	μA
				V_O = 4.0V				80	
B PORT (B_0-B_7)									
V_{IH}	Logical "1" Input Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V			2.0			Volts
V_{IL}	Logical "0" Input Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V		COM'L			0.8	Volts
					MIL			0.7	
V_{OH}	Logical "1" Output Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.8		Volts
				I_{OH} = −5.0mA		2.7	3.9		
				I_{OH} = −10mA		2.4	3.6		
V_{OL}	Logical "0" Output Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OL} = 20mA			0.3	0.4	Volts
				I_{OL} = 48mA			0.4	0.5	
I_{OS}	Output Short Circuit Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_O = 0V V_{CC} = MAX, Note 2			−25	−50	−150	mA
I_{IH}	Logical "1" Input Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V				−200	μA
				V_O = 4.0V				200	
CONTROL INPUTS $\overline{T}$, $\overline{R}$									
V_{IH}	Logical "1" Input Voltage					2.0			Volts
V_{IL}	Logical "0" Input Voltage				COM'L			0.8	Volts
					MIL			0.7	
I_{IH}	Logical "1" Input Current		V_I = 2.7V				0.5	20	μA
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX, V_I = V_{CC} MAX					1.0	mA
I_{IL}	Logical "0" Input Current		V_I = 0.4V		$\overline{R}$		−0.1	−0.25	mA
					$\overline{T}$		−0.25	−0.5	
V_C	Input Clamp Voltage		I_{IN} = −12mA				−0.8	−1.5	Volts
POWER SUPPLY CURRENT									
I_{CC}	Power Supply Current	Am2948	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 2.0V, V_{CC} = MAX				70	100	mA
			$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2.0V, V_{CC} = MAX				100	150	
		Am2949	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 0.4V, V_{CC} = MAX				70	100	mA
			$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2.0V, V_{CC} = MAX				90	140	

Am2948

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	20	27	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	8	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	18	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	25	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	16	25	ns

FUNCTION TABLE

Control Inputs		Resulting Conditions	
Transmit	Receive	A Port	B Port
1	0	Out	In
0	1	In	Out
1	1	3-State	3-State
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Am2948
AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am2948 COM'L $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max	Am2948 MIL $T_A = -55$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max	Units
		A PORT DATA/MODE SPECIFICATIONS			
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	19	16	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	23	20	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
		B PORT DATA/MODE SPECIFICATIONS			
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	29	24	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	19	16	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	30	25	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	19	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

Am2949
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ	Max	Units
	A PORT DATA/MODE SPECIFICATIONS				
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	20	27	ns
	B PORT DATA/MODE SPECIFICATIONS				
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	17	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	24	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	17	25	ns

DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 A port inputs/outputs are receiver output drivers when $\overline{\text{Receive}}$ is LOW and $\overline{\text{Transmit}}$ is HIGH, and are transmit inputs when $\overline{\text{Receive}}$ is HIGH and $\overline{\text{Transmit}}$ is LOW.

B_0-B_7 B port inputs/outputs are transmit output drivers when $\overline{\text{Transmit}}$ is LOW and $\overline{\text{Receive}}$ is HIGH, and are receiver inputs when $\overline{\text{Transmit}}$ is HIGH and $\overline{\text{Receive}}$ is LOW.

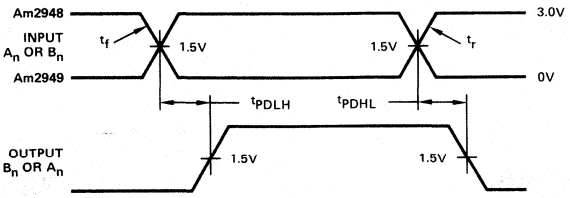
$\overline{\text{Transmit}}$, $\overline{\text{Receive}}$ These controls determine whether A port and B port drivers are in 3-state. With both $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ HIGH both ports are in 3-state. $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ both LOW activate both drivers and may cause oscillations. This is not an intended logic condition. With $\overline{\text{Transmit}}$ HIGH and $\overline{\text{Receive}}$ LOW A port is the output and B port is the input. With $\overline{\text{Transmit}}$ LOW and $\overline{\text{Receive}}$ HIGH B port is the output and A port is the input.

Am2949

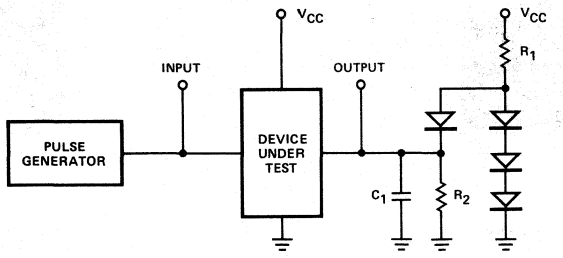
AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am2949 COM'L $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max	Am2949 MIL $T_A = -55$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

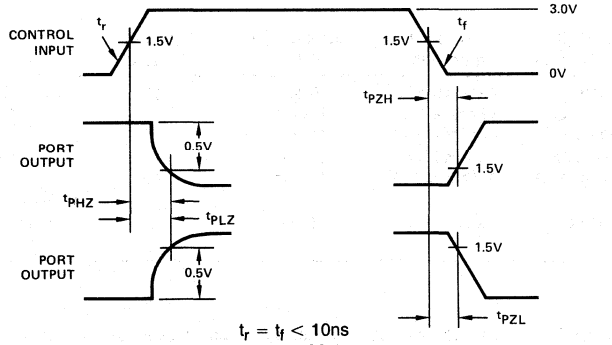


$t_r = t_f < 10ns$
10% to 90%

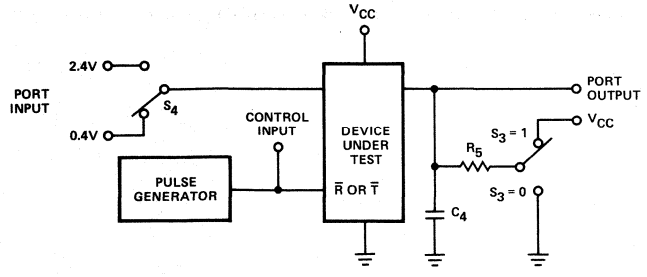


Note: C_1 includes test fixture capacitance.

Figure A. Propagation Delay from A Port to B Port or from B Port to A Port



$t_r = t_f < 10ns$
10% to 90%

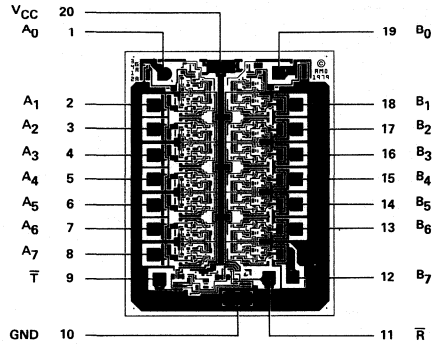


Note: C_4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

Figure B. Propagation Delay to/from Three-State from $\overline{R}$ to A Port and $\overline{T}$ to B Port

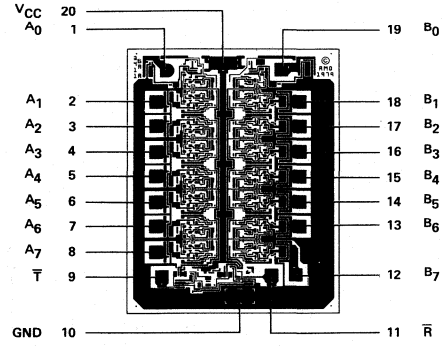
Metallization and Pad Layouts

Am2948



DIE SIZE .069" X .089"

Am2949



DIE SIZE .069" X .089"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2948 Order Number	Am2949 Order Number	Package Type (Note 1)	Operating (Note 2)	Screening Level (Note 3)
AM2948PC	AM2949PC	P-20-1	C	C-1
AM2948DC	AM2949DC	D-20-1	C	C-1
AM2948DC-B	AM2949DC-B	D-20-1	C	B-1
AM2948DM	AM2949DM	D-20-1	M	C-3
AM2948DM-B	AM2949DM-B	D-20-1	M	B-3
AM2948XC	AM2949XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2950 • Am2951

Eight-Bit Bidirectional I/O Ports with Handshake

DISTINCTIVE CHARACTERISTICS

- Eight-Bit, Bidirectional I/O Port with Handshake –
  Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional busses.
- Register Full/Empty Flags –
  On-chip flag flip-flops provide data transfer handshaking signals.
- Separate Clock, Clock Enable and Three-State Output Enable for Each Register.
- Separate, Edge-Sensitive Clear Control for Each Flag Flip-Flop.
- Inverting and Non-Inverting Versions –
  The Am2950 provides non-inverting data outputs. The Am2951 provides inverting data outputs.
- 24mA Output Current Sink Capability.
- 100% Reliability Assurance Testing in Compliance with MIL-STD-883.

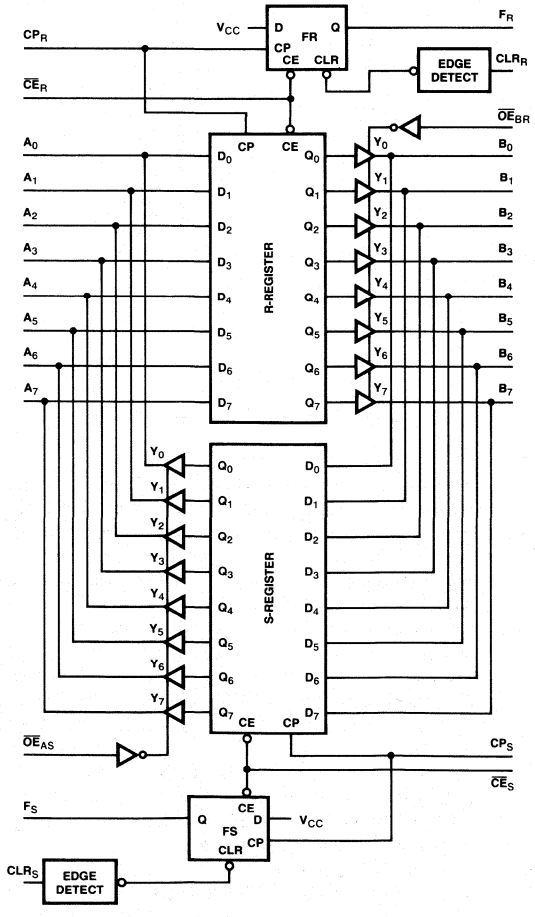
GENERAL DESCRIPTION

The Am2950 and Am2951, members of Advanced Micro Devices Am2900 Family, are designed for use as parallel data I/O ports. Two eight-bit, back to back registers store data moving in both directions between two bidirectional, 3-state busses. On chip flag flip-flops, set automatically when a register is loaded, provide the handshaking signals required for demand-response data transfer.

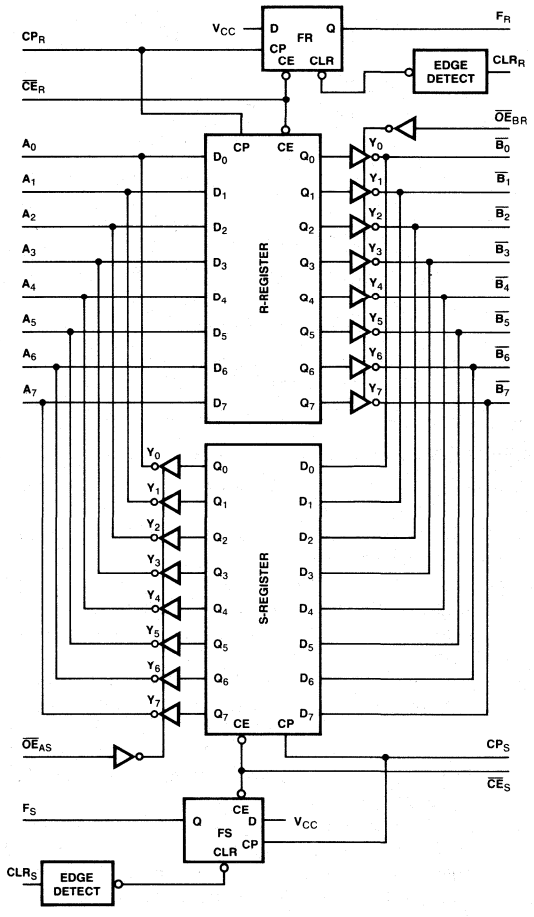
Considerable flexibility is designed into the Am2950 • Am2951. Separate clock, clock enable and three-state output enable signals are provided for each register, and edge-sensitive clear inputs are provided for each flag flip-flop. A number of these circuits can be used for wider I/O ports. Both inverting and non-inverting versions are available.

Twenty-four mA output current sink capability, sufficient for most three-state busses, is provided by the Am2950 • Am2951.

Am2950 BLOCK DIAGRAM



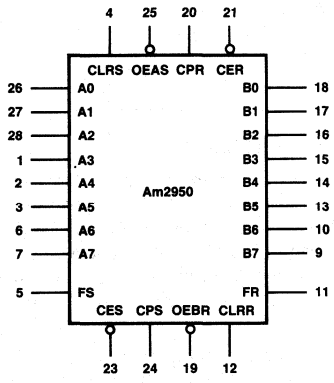
Am2951 BLOCK DIAGRAM



6

LOGIC SYMBOLS

Am2950



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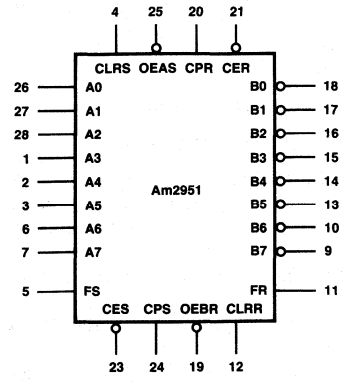
Am2951



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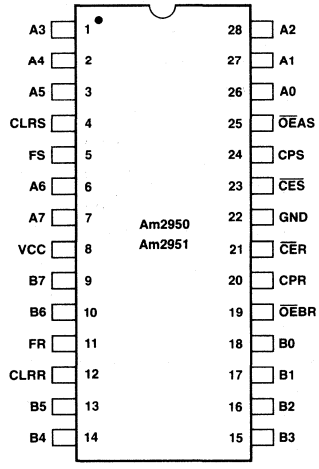
CONNECTION DIAGRAMS
Top Views

DIP



Note: Pin 1 is marked for orientation.
Bi is inverted on Am2951.

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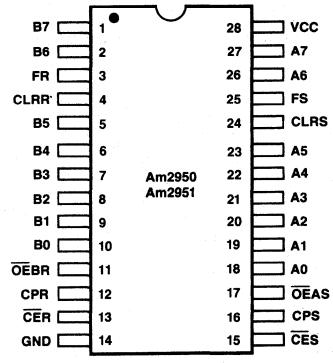
FLAT PACK



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DEFINITION OF FUNCTIONAL TERMS

A0-7 Eight bidirectional lines carrying the R Register inputs or S Register outputs.

B0-7 Eight bidirectional lines carrying the S Register inputs or R Register outputs.

CPR The clock for the R Register and FR Flip-Flop. When $\overline{CER}$ is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW to HIGH transition of the CPR signal.

$\overline{CER}$ The Clock Enable for the R Register and FR Flip-Flop. When $\overline{CER}$ is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW to HIGH transition of the CPR signal. When $\overline{CER}$ is HIGH, The R Register and FR Flip-Flop hold their contents, regardless of CPR signal transitions.

$\overline{OEBR}$ The Output Enable for the R Register. When $\overline{OEBR}$ is LOW, The R Register three-state outputs are enabled onto the B0-7 lines. When $\overline{OEBR}$ is HIGH, the R Register outputs are in the high-impedance state.

FR The FR Flip-Flop output.

CLRR The clear control for the FR Flip-Flop. The FR Flip-Flop is cleared on the LOW to HIGH transition of CLRR signal.

CPS The clock for the S Register and FS Flip-Flop. When $\overline{CES}$ is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW to HIGH transtion of the CPS signal.

$\overline{CES}$ The clock enable for the S Register and FS Flip-Flop. When $\overline{CES}$ is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW to HIGH transition of the CPS signal. When $\overline{CES}$ is HIGH, the S Register and FS Flip-Flop hold their contents, regardless of CPS signal transitions.

$\overline{OEAS}$ The output enable for the S Register. When $\overline{OEAS}$ is LOW, the S Register three-state outputs are enabled onto the A0-7 lines. When OEAS is HIGH, the S Register outputs are in the high-impedance state.

FS The FS Flip-Flop output.

CLRS The clear control for the FS Flip-Flop. The FS Flip-Flop is cleared on the LOW to HIGH transition of CLRS signal.

REGISTER FUNCTION TABLE
(Applies to R or S Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

OUTPUT CONTROL

	Internal	Y-Outputs		
$\overline{OE}$	Q	Am2950	Am2951	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

FLAG FLIP-FLOP FUNCTION TABLE
(Applies to R or S Flag Flip-Flop)

Inputs			F-Output	Function
$\overline{CE}$	CP	CLR		
H	X	↟	NC	Hold Flag
X	X	↑	L	Clear Flag
L	↑	↟	H	Set Flag

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
NC = NO CHANGE
↑ = LOW-to-HIGH Transition
↟ = NO LOW-to-HIGH Transition

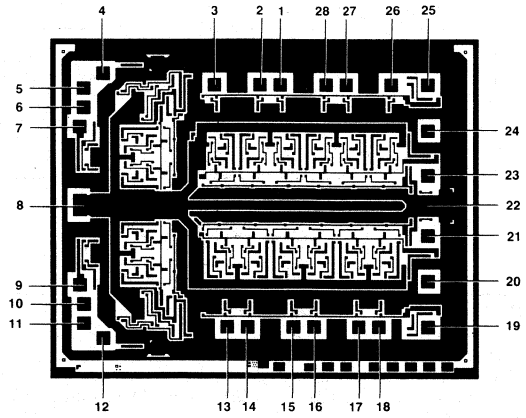
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2950 Order Number	Am2951 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2950PC	AM2951PC	P-28	C	C-1
AM2950DC	AM2951DC	D-28	C	C-1
AM2950DC-B	AM2951DC-B	D-28	C	B-2 (Note 4)
AM2950DM	AM2951DM	D-28	M	C-3
AM2950DM-B	AM2951DM-B	D-28	M	B-3
AM2950FM	AM2951FM	F-28-2	M	C-3
AM2950FM-B	AM2951FM-B	F-28-2	M	B-3
AM2950XC	AM2951XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2950XM	AM2951XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

METALLIZATION AND PAD LAYOUT



Numbers refer to DIP pin connection
DIE SIZE 0.107" X 0.138"

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +VCC max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

Part Number	Range	Temperature	VCC
Am2950/51PC, DC	COM'L	T_A = 0°C to +70°C	VCC = 5.0V ±5% (MIN. = 4.75V, MAX. =5.25V)
Am2950/51DM, FM	MIL	TC = −55°C to +125°C	VCC = 5.0V ±10% (MIN. = 4.50V, MAX. = 5.50V)

Am2950, Am2951
DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
VOH	Output HIGH Voltage	VCC = MIN., VIN = VIH or VIL	FR, FS	IOH = −1mA	2.4	3.4		Volts
			A0-7, B0-7	MIL, IOH = −2mA	2.4	3.4		
				COM'L, IOH = −6.5mA	2.4	3.4		
VOL	Output LOW Voltage (Note 5)	VCC = MIN., VIN = VIH or VIL	FR, FS	IOL = 12mA			0.5	Volts
			A0-7, B0-7	MIL IOL = 16mA			0.5	
				COM'L IOL = 24mA			0.5	
VIH	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
VIL	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
VI	Input Clamp Voltage	VCC = MIN., IIN = −18mA					−1.5	Volts
IIL	Input LOW Current	VCC = MAX., VIN = 0.5V		A0-7, B0-7			−250	μA
				CLRR, CLRS			−2.0	mA
				Others			−360	μA
IIH	Input HIGH Current	VCC = MAX., VIN = 2.7V		A0-7, B0-7			70	μA
				CLRR, CLRS			100	
				Others			20	
II	Input HIGH Current	VCC = MAX., VIN = 5.5V					1.0	mA
IO	Output Off-state Leakage Current	VCC = MAX.	A0-7, B0-7	V0 = 2.4V			70	μA
				V0 = 0.4V			−250	
ISC	Output Short Circuit Current (Note 3)	VCC =MAX.			−30		−85	mA
ICC	Power Supply Current (Notes 4, 6)	VCC = MAX.		T_A = 25°C		156	263	mA
			COM'L	T_A = 0°C to +70°C			275	
				T_A = +70°C			228	
			MIL	T_C = −55°C to +125°C			309	
				T_C = +125°C			202	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at VCC = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. ICC is measured with all inputs at 4.5V and all outputs open.
5. The sum of IOL into Ai and Bi for each i must not exceed 32mA COM'L, 24mA MIL at a given point in time.
6. Worst case ICC is at minimum temperature.

SWITCHING CHARACTERISTICS

The tables below define the Am2950 • Am2951 switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are recovery times. Tables D are pulse-width requirements. Tables E are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with RL on Ai and Bi = 220Ω and RL on FS and FR = 300Ω. CL = 50pF except output disable times which are specified at CL = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, VCC = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPS ↓	7	5
B0-7	CPR ↓	7	5
$\overline{CES}$	CPS ↓	*19/15	4
$\overline{CER}$	CPR ↓	*19/15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓	*30/26	–	20	–
CPR ↓	–	*30/26	–	20
CLRS ↓	–	–	22	–
CLRR ↓	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ↓	CPS ↓	31
CLRR ↓	CPR ↓	31

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	22	27
$\overline{OE}$BR	B0-7	22	27

*Where two numbers appear, the first is the Am2950 spec, the second is the Am2951 spec

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, VCC = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPS ↓	11	8
B0-7	CPR ↓	11	8
$\overline{CES}$	CPS ↓	*20/15	4
$\overline{CER}$	CPR ↓	*20/15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓	*35/28	–	20	–
CPR ↓	–	*35/28	–	20
CLRS ↓	–	–	22	–
CLRR ↓	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ↓	CPS ↓	34
CLRR ↓	CPR ↓	34

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

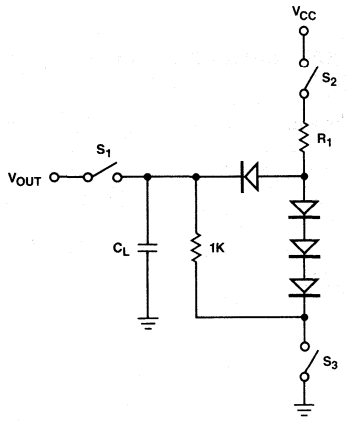
E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	24	28
$\overline{OE}$BR	B0-7	24	28

*Where two numbers appear, the first is the Am2950 spec, the second is the Am2951 spec

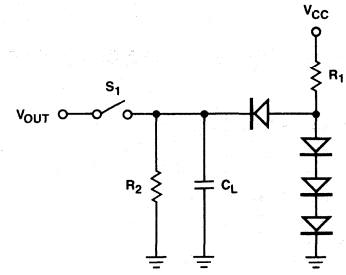
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2950/2951

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2950/2951

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	A_{0-7}	A	220	1K
–	B_{0-7}	A	220	1K
5	FS	B	300	2.4K
11	FR	B	300	2.4K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS

The Am2950 • Am2951 provides data transfer handshaking signals as well as eight-bit, bidirectional data storage. Its flexibility allows it to be used in any type of computer system, including Am2900, 8080, 8085, 8086, Z80, and Z8000 systems.

Figure 1 shows an Am2950 used to store data moving in both directions between a bidirectional system data bus and a bidirectional peripheral data bus. The on-chip Flag flip-flops provide the data in, data out handshaking signals required for data transfer and interrupt request generation.

Figure 2 shows a multiple I/O port system using Am2950's. Two Am2950's are used at each port to interface the 16-bit system data bus. The Am2950 flags are used to generate I/O interrupt requests.

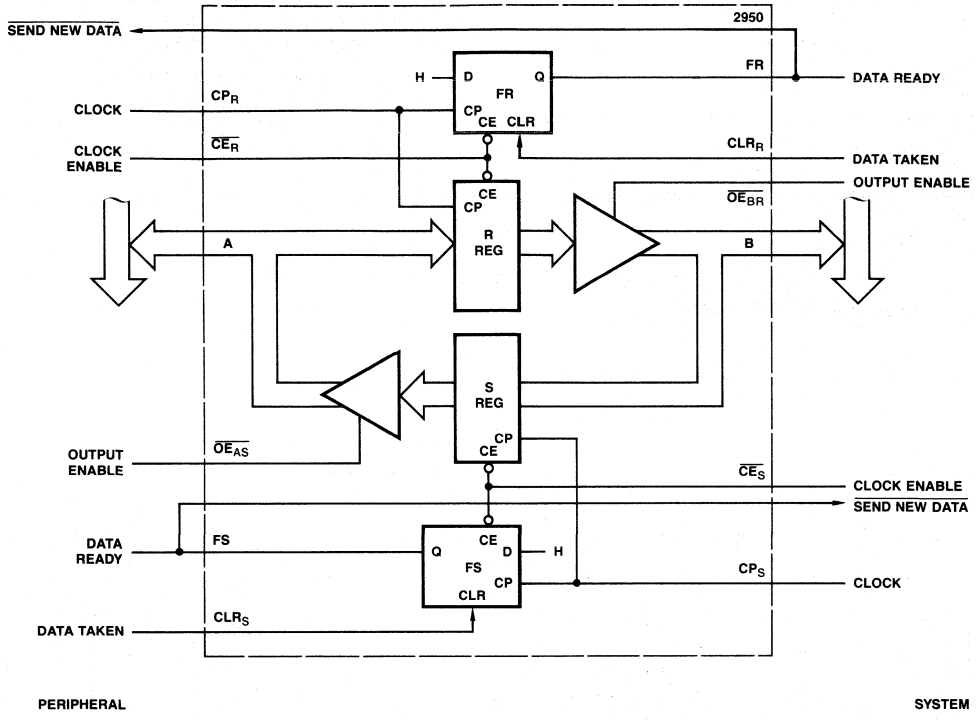


Figure 1. A Bidirectional I/O Port with Handshaking Using the Am2950.

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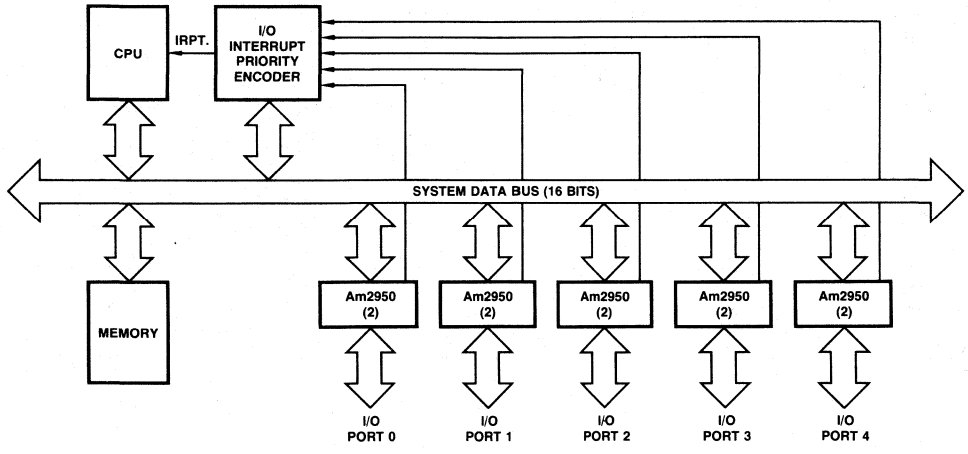

Figure 2. Multiple I/O Port System.

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Am2952 • Am2953

Eight-Bit Bidirectional I/O Ports

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Eight-Bit, Bidirectional I/O Port
  Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional busses.
- Separate Clock, Clock Enable and Three-State Output Enable for Each Register.
- Inverting and Non-Inverting Versions –
  The Am2952 provides non-inverting data ouputs. The Am2953 provides inverting data outputs.
- 24mA Output Current Sink Capability.
- 100% Reliability Assurance Testing in Compliance with MIL-STD-883.
- 24-Pin Slim Package

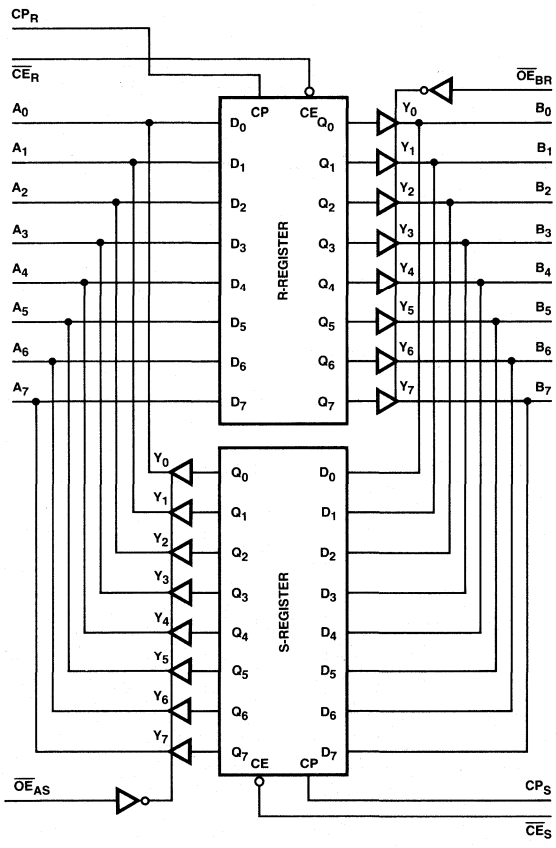
GENERAL DESCRIPTION

The Am2952 and Am2953, members of Advanced Micro Devices Am2900 Family, are designed for use as parallel data I/O ports. Two eight-bit, back to back registers store data moving in both directions between two bidirectional, 3-state busses.

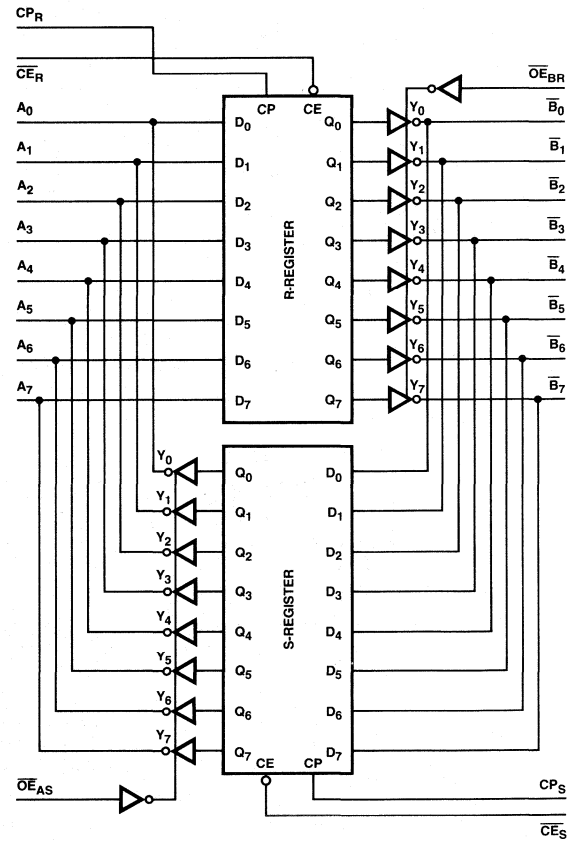
Considerable flexibility is designed into the Am2952 • Am2953. Separate clock, clock enable and three-state output enable signals are provided for each register. A number of these circuits can be used for wider I/O ports. Both inverting and non-inverting versions are available.

Twenty-four mA output current sink capability, sufficient for most three-state busses, is provided by the Am2952 • Am2953.

Am2952 BLOCK DIAGRAM



Am2953 BLOCK DIAGRAM



Am2954 • Am2955

Octal Registers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high-speed parallel registers
- Am2954 has non-inverting inputs
- Am2955 has inverting inputs
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- V_{OL} = 0.5V (max) at I_{OL} = 32mA
- High-speed – Clock to output 11ns typical
- 100% product assurance screening to MIL-STD-883 requirements

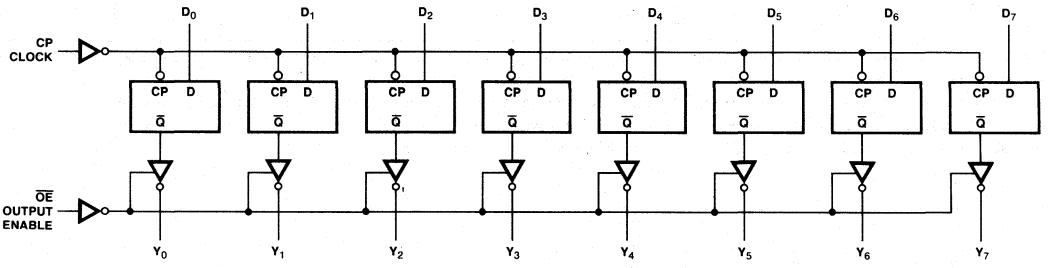
FUNCTIONAL DESCRIPTION

The Am2954 and Am2955 are 8-bit registers built using high-speed Schottky technology. The registers consist of eight D-type flip-flops with a buffered common clock and a buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the 3-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

LOGIC DIAGRAM
Am2954



Inputs D_0 through D_7 are inverted on the Am2955.

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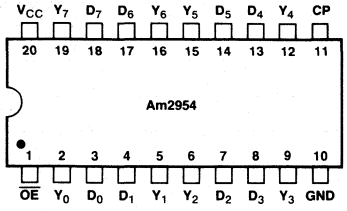
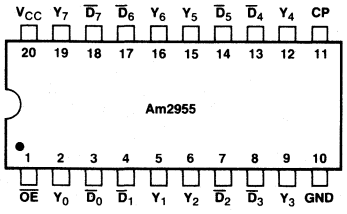
CONNECTION DIAGRAMS – Top Views

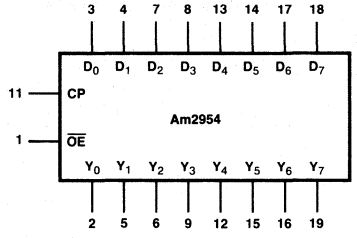


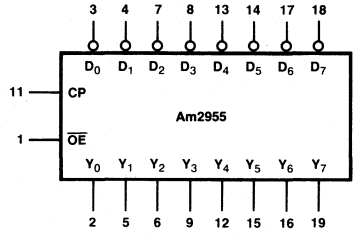


Note: Pin 1 is marked for orientation.

BLI-111

LOGIC SYMBOLS





V_{CC} = Pin 20
GND = Pin 10

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2954XC, DC, PC	Am2955XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am2954XM, DM, FM	Am2955XM, DM, FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.45	Volts
			I_{OL} = 32mA			.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.5V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			90	140	mA

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Am2954 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.
   Am2955 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

SWITCHING CHARACTERISTICS

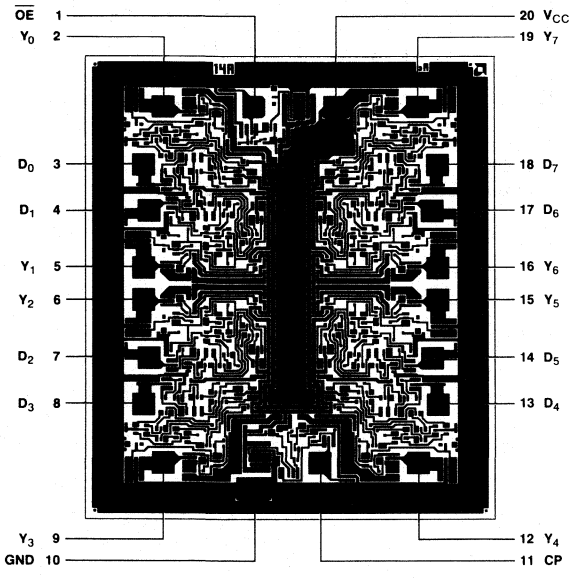
(T_A = 25°C, V_{CC} = 5.0V)

Parameters	Description		Am2954 • Am2955 Min	Typ	Max	Units	Test Conditions
t_{PLH}	Clock to Output, Y_i			8	15	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}				11	17	ns	
t_{ZH}	$\overline{OE}$ to Y_i			8	15	ns	
t_{ZL}				11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i			5	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}				7	12	ns	
t_{PW}	Clock Pulse Width	HIGH	6			ns	C_L = 15pF, R_L = 280Ω
		LOW	7.3			ns	
t_S	Data to Clock		5			ns	
t_H			2			ns	
f_{max}	Maximum Clock Frequency (Note 1)		75	100		MHz	

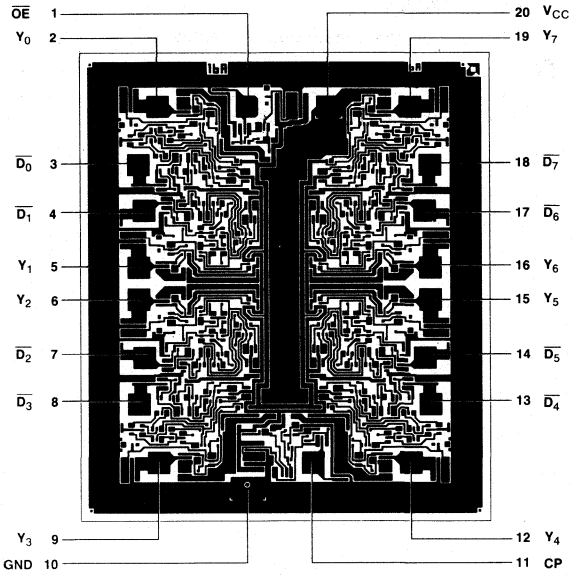
Note: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Metallization and Pad Layouts

Am2954



Am2955



DIE SIZE 0.096" X 0.083"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2954 Order Number	Am2955 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2954PC	AM2955PC	P-20-1	C	C-1
AM2954DC	AM2955DC	D-20-1	C	C-1
AM2954DC-B	AM2955DC-B	D-20-1	C	B-1
AM2954DM	AM2955DM	D-20-1	M	C-3
AM2954DM-B	AM2955DM-B	D-20-1	M	B-3
AM2954FM	AM2955FM	F-20	M	C-3
AM2954FM-B	AM2955FM-B	F-20	M	B-3
AM2954XC	AM2955XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2954XM	AM2955XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs (Am2954, non-inverting).

$\overline{D_i}$ The D flip-flop data inputs (Am2955, inverting).

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Y_i The register three-state outputs (Am2954, non-inverting).

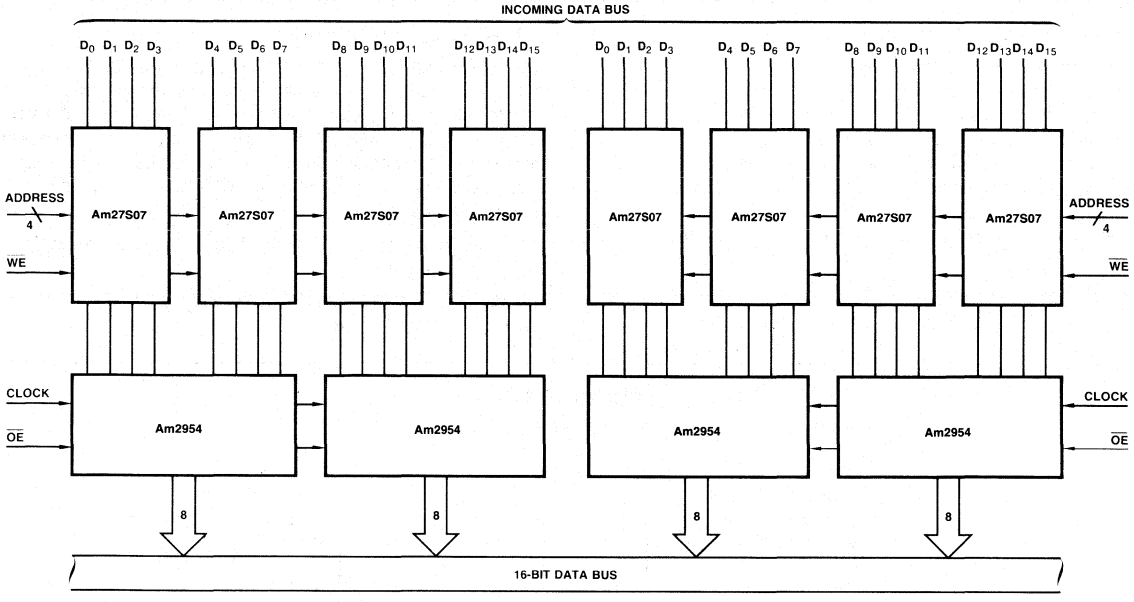
$\overline{OE}$ Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

FUNCTION TABLE

Function	Inputs				Internal	Outputs
	$\overline{OE}$	Clock	Am2954 D_i	Am2955 $\overline{D_i}$	Q_i	Y_i
Hi-Z	H	L	X	X	NC	Z
	H	H	X	X	NC	Z
LOAD REGISTER	L	↑	L	H	L	L
	L	↑	H	L	H	H
	H	↑	L	H	L	Z
	H	↑	H	L	H	Z

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance
↑ = LOW-to-HIGH transition

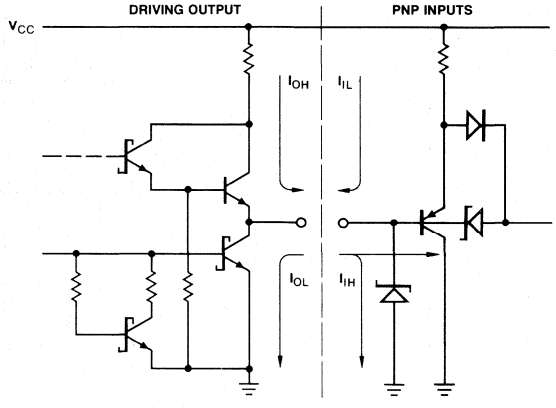
APPLICATION



Dual 16-word by 16-bit non-inverting high-speed data buffer.

BLI-113

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI-114

Am2956 • Am2957

Octal Latches with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 8-bit, high-speed parallel latches
- Am2956 has non-inverting inputs
- Am2957 has inverting inputs
- V_{OL} = 0.5V (max) at I_{OL} = 32mA
- Hysteresis on latch enable input for improved noise margin
- 3-state outputs interface directly with bus organized systems
- 100% product assurance screening to MIL-STD-883 requirements

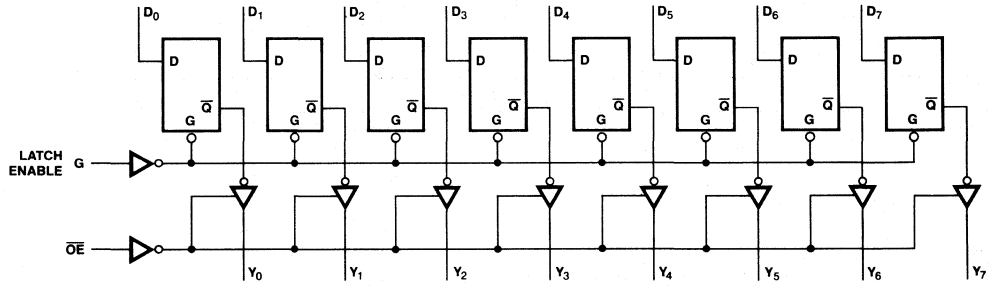
FUNCTIONAL DESCRIPTION

The Am2956 and Am2957 are octal latches with 3-state outputs for bus organized system applications. The latches appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

The Am2956 presents non-inverted data at the outputs while the Am2957 is inverting.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

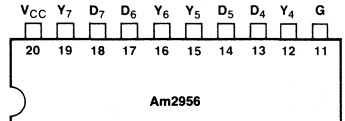
LOGIC DIAGRAM
Am2956



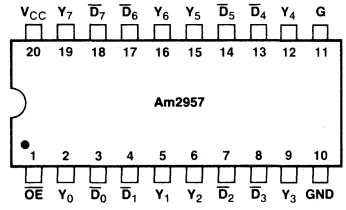
Inputs D_0 through D_7 are inverted on the Am2957.

BLI-139

CONNECTION DIAGRAMS – Top Views



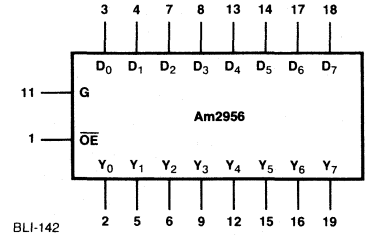
BLI-140



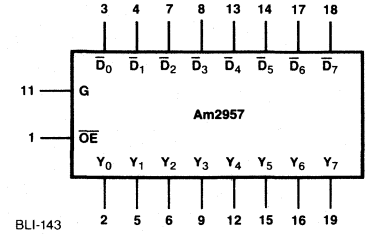
BLI-141

Note: Pin 1 is marked for orientation.

LOGIC SYMBOLS



BLI-142



BLI-143

V_{CC} = Pin 20
GND = Pin 10

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2956/2957XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am2956/2957XM, DM	T_A = −55 to +125°C	V_{CC} = 4.50 to 5.50V
Am2956/2957FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
				COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.45	Volts
				I_{OL} = 32mA			.5	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current		V_{CC} = MAX	V_O = 0.5V			−50	μA
				V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	2956	V_{CC} = MAX			105	160	mA
		2957				110	168	

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

Am2956
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min	Typ	Max	Units	Test Conditions
t_{PLH}	Enable to Output		7	14	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			12	18	ns	
t_{PLH}	Data Input to Output		5	9	ns	
t_{PHL}			9	13	ns	
t_s(H)	HIGH Data to Enable	0			ns	
t_s(L)	LOW Data to Enable	0			ns	
t_h(H)	HIGH Data to Enable	10			ns	
t_h(L)	LOW Data to Enable	10			ns	
t_{pwH}	Enable Pulse Width	6			ns	
t_{pwL}		7.3			ns	
t_{ZH}	$\overline{OE}$ to Y_i		8	15	ns	
t_{ZL}			11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i		6	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}			8	12	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLES

Am2956

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	D_i	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	L	Transparent
L	H	H	L	H	
L	L	X	NC	NC	Latched

Am2957

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	$\overline{D_i}$	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	H	Transparent
L	H	H	L	L	
L	L	X	NC	NC	Latched

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

Am2956

D_i The latch data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i The 3-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

Am2957

$\overline{D_i}$ The latch inverting data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

$\overline{Y_i}$ The 3-state latch outputs.

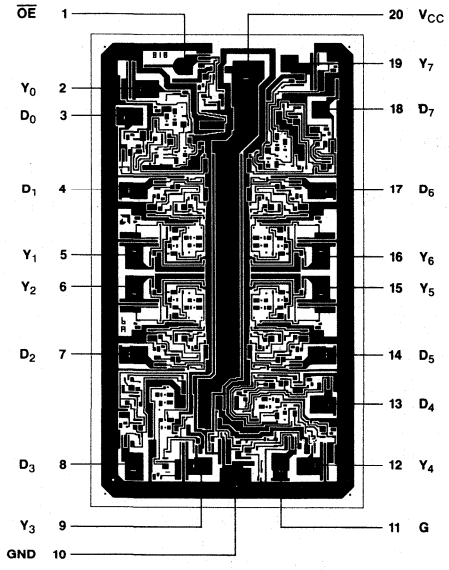
$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the inverted outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

Am2957
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min	Typ	Max	Units	Test Conditions
t_{PLH}	Enable to Output		17	24	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			19	26	ns	
t_{PLH}	Data Input to Output		10	14	ns	
t_{PHL}			14	20	ns	
$t_s(H)$	HIGH Data to Enable	0			ns	
$t_s(L)$	LOW Data to Enable	0			ns	
$t_h(H)$	HIGH Data to Enable	10			ns	
$t_h(L)$	LOW Data to Enable	10			ns	
t_{pwH}	Enable Pulse Width	6			ns	
t_{pwL}		7.3			ns	
t_{ZH}	$\overline{OE}$ to Y_i		8	15	ns	
t_{ZL}			11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i		6	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}			8	10	ns	

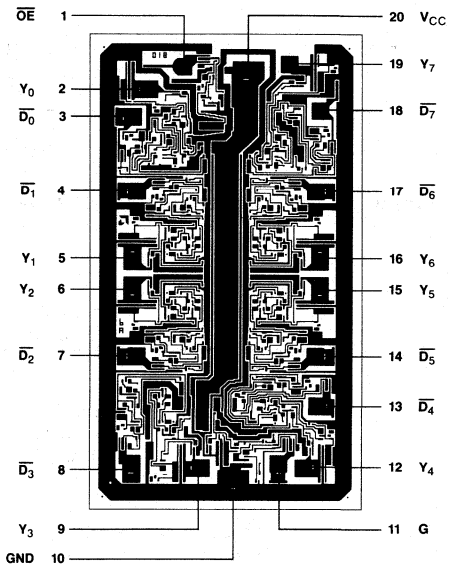
Metallization and Pad Layouts

Am2956



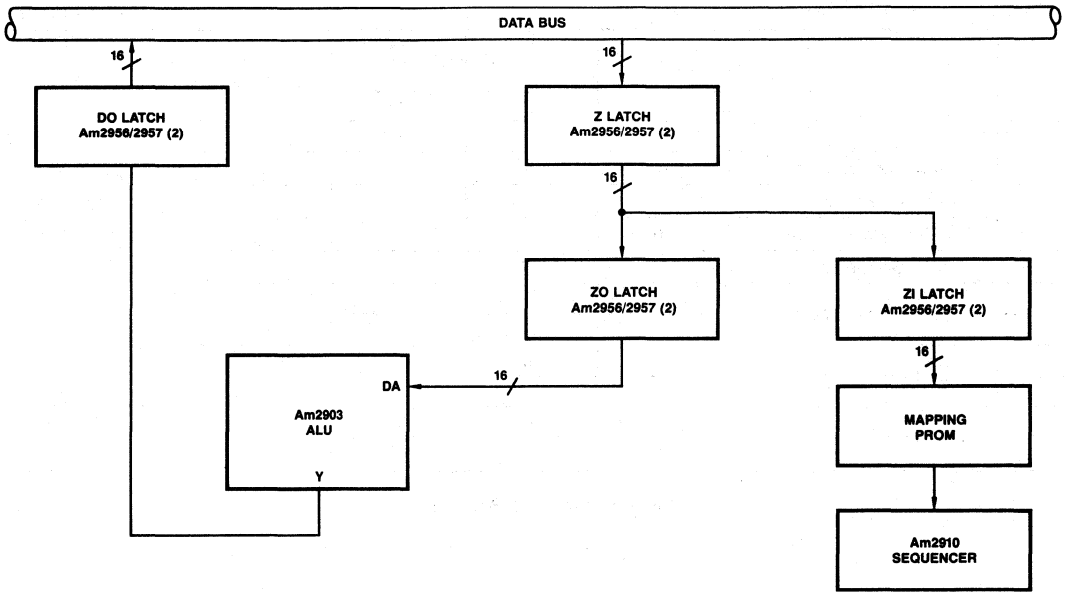
DIE SIZE 0.066" X 0.119"

Am2957



DIE SIZE 0.066" X 0.119"

APPLICATION



Transparent Latches are used in high performance CPU designs. The Z Latch configuration shown provides overlapped fetch of machine instructions and operand data.

BLI-144

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am2956 Order Number	Am2957 Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2956PC	AM2957PC	P-20	C	C-1
AM2956DC	AM2957DC	D-20	C	C-1
AM2956DCB	AM2957DCB	D-20	C	B-1
AM2956DM	AM2957DM	D-20	M	C-3
AM2956DMB	AM2957DMB	D-20	M	B-3
AM2956FM	AM2957FM	F-20	M	C-3
AM2956FMB	AM2957FMB	F-20	M	B-3
AM2956XC	AM2957XC	Dice	C	Visual Inspection to MIL-STD-883 Method 2010B.
AM2956XM	AM2957XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpak. Number following letter is number of leads.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See standard AMD Product Assurance Brochures for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2958 • Am2959

Octal Buffers/Line Drivers/Line Receivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Advanced Schottky processing
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- V_{OL} of 0.55V at 65mA for commercial-range product; 48mA for military-range product
- Data-to-output propagation delay times:
  Inverting – 7.0ns MAX
  Non-inverting – 9.0ns MAX
- Enable-to-output – 15.0ns MAX
- 100% reliability assurance testing in compliance with MIL-STD-883
- 20-pin hermetic and molded DIP packages

FUNCTIONAL DESCRIPTION

These buffers/line drivers, used as memory-address drivers, clock drivers, and bus oriented transmitters/receivers, provide improved PC board density. The outputs of the commercial temperature range versions have 64mA sink and 15mA source capability, which can be used to drive terminated lines down to 133Ω. The outputs of the military temperature range versions have 48mA sink and 12mA source current capability.

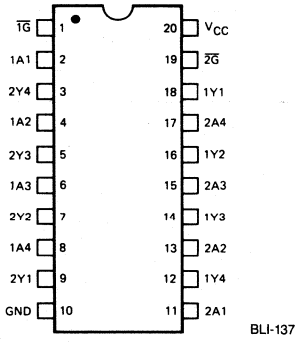
Featuring 0.2V minimum guaranteed hysteresis at each low-current PNP data input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely.

The Am2958 and Am2959 have four buffers enabled from one common line, and the other four buffers enabled from another common line. The Am2958 is inverting, while the Am2959 presents true data at the outputs.

6

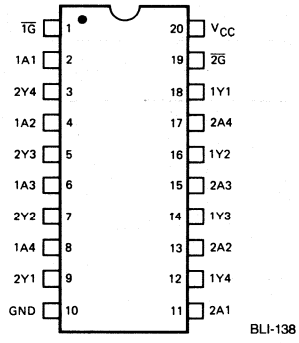
CONNECTION DIAGRAMS
Top Views

Am2958



BLI-137

Am2959



BLI-138

ORDERING INFORMATION

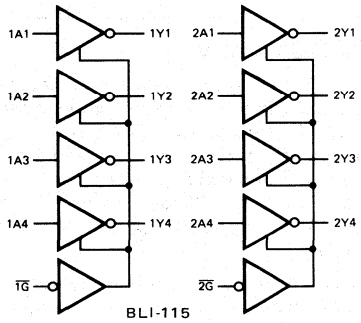
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2958 Order Number	Am2959 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2958PC	AM2959PC	P-20-1	C	C-1
AM2958DC	AM2959DC	D-20-1	C	C-1
AM2958DC-B	AM2959DC-B	D-20-1	C	B-1
AM2958DM	AM2959DM	D-20-1	M	C-3
AM2958DM-B	AM2959DM-B	D-20-1	M	B-3
Am2958XC	Am2959XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am2958XM	Am2959XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883.

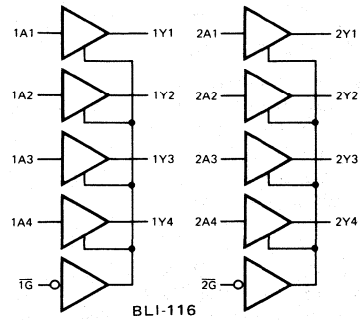
LOGIC DIAGRAMS

Am2958



BLI-115

Am2959



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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	–0.5V to +V_{CC} max.
DC Input Voltage	–0.5V to +7.0V
DC Output Current	150mA
DC Input Current	–30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am2958 (MIL)	T_A = −55 to +125°C	V_{CC} (MIN.) = 4.50V	V_{CC} (MAX.) = 5.50V
Am2959 (COM'L)	T_A = 0 to 70°C	V_{CC} (MIN.) = 4.75V	V_{CC} (MAX.) = 5.25V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

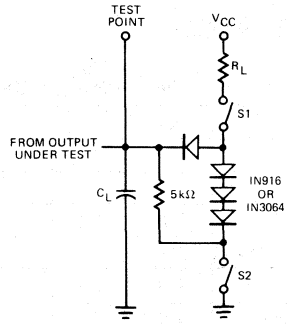
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{IH}	High-Level Input Voltage			2.0			Volts
V_{IL}	Low-Level Input Voltage				0.8		Volts
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., I_I = −18mA				−1.2	Volts
	Hystersis ($V_{T+} - V_{T-}$)	V_{CC} = MIN.		0.2	0.4		Volts
V_{OH}	High-Level Output Voltage	V_{CC} = MIN., V_{CC} = 0.8V	COM'L, I_{OH} = −1mA	2.7			Volts
			I_{OH} = −3mA	2.4	3.4		
		V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
			COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN., V_{IL} = 0.8V	MIL, I_{OL} = 48mA			0.55	Volts
			COM'L, I_{OL} = 64mA			0.55	
I_{OZH}	Off-State Output Current, High-Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = 0.8V	V_O = 2.4V			50	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage applied		V_O = 0.5V			−50	
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 5.5V				1.0	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} MAX., V_{IH} = 2.7V				50	μA
I_{IL}	Low-Level Input Circuit	V_{CC} = MAX., V_{IL} = 0.5V	Any A			−400	μA
			Any G			−2.0	mA
I_{OS}	Short-Circuit Output Current (Note 3)	V_{CC} = MAX.		−50		−225	mA
I_{CC}	Supply Current, Am2958	V_{CC} = MAX., Outputs Open	All Outputs HIGH, MIL and COM'L		37	65	mA
			All Outputs LOW, MIL and COM'L		59	90	
			Outputs at Hi-Z, MIL and COM'L		69	105	
	Supply Current, Am2959	V_{CC} = MAX., Outputs Open	All Outputs HIGH, MIL and COM'L		37	65	mA
			All Outputs LOW, MIL and COM'L		63	105	
			Outputs at Hi-Z, MIL and COM'L		72	120	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed on second.

WITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

arameter	Description	Test Conditions	Am2958 Min.	Am2958 Typ.	Am2958 Max.	Am2959 Min.	Am2959 Typ.	Am2959 Max.	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 50pF, R_L = 90Ω (Note 3)		4.5	7.0		6.0	9.0	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			4.5	7.0		6.0	9.0	ns
t_{ZL}	Output Enable Time to Low Level			10	15		10	15	ns
t_{ZH}	Output Enable Time to High Level			6.5	10		8.0	12	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0pF, R_L = 90Ω (Note 3)		10	15		10	15	ns
t_{HZ}	Output Disable Time from High Level			6.0	9.0		6.0	9.0	ns

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



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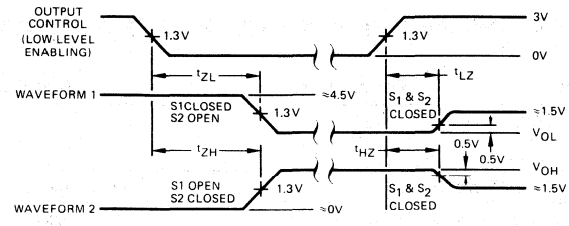
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



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Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.

FUNCTION TABLES

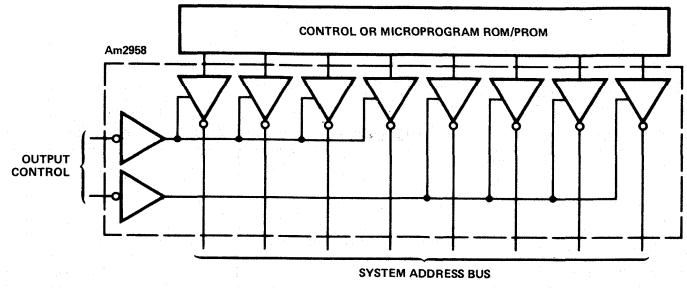
Am2958

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am2959

INPUTS		OUTPUT
$\overline{G}$	A	
H	X	Z
L	H	H
L	L	L

Am2958 USED AS SYSTEM BUS DRIVER – 4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



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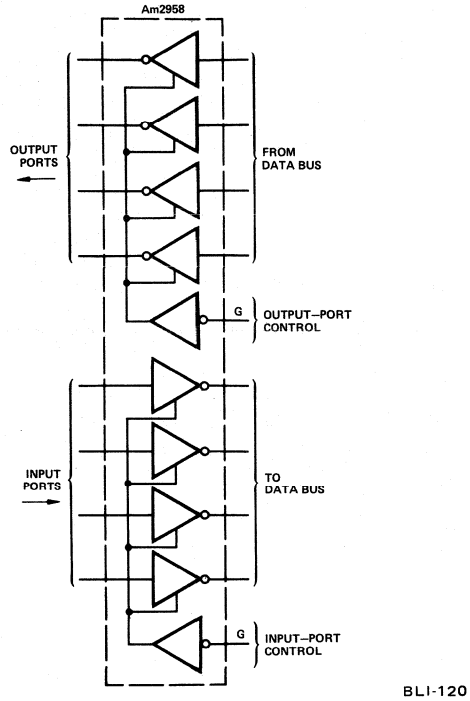
APPLICATIONS (Cont.)

INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



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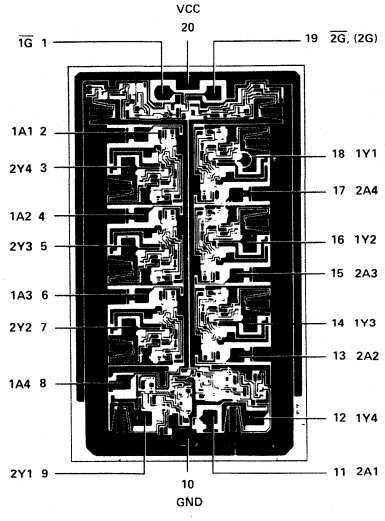
Metallization and Pad Layout

Am2958 • Am2959



DIE SIZE 0.077" X 0.124"

Am2960
Dynamic Memory Support Index

The Am2960 Family Dynamic Memory Support Products

Advanced Micro Devices has developed a set of bipolar high-performance memory-support products to maximize the speed and reliability of MOS dynamic RAM systems. This family is designed to provide, in the minimum package count, all the logic, interface and control functions required in the address and data paths of memory systems based on 16K and 64K devices.

These TTL-compatible products are specified for use in equipment based on either bipolar or MOS CPUs. The Am2960 Series serves bipolar microprocessors such as the Am2901, Am29203, etc., while the AmZ8160 Series serves MOS microprocessors, such as the 16-bit AmZ8000.

Key System Level Features

Maximum Memory Performance

- Schottky performance with matched T_{PD} paths and skew limit guarantees.
- Optimized interface devices for maximum speed.
- Hamming code EDC with internal ECL circuitry for maximum speed combined with maximum memory reliability.

Lowest Package Count Plus Maximum Flexibility

- LSI DMC Controller is designed for up to 64K RAMs.
- EDC is 16-bit expandable slice with byte I/O controls.
- Flexible interface for speed or minimum parts count.

Operation in Any Timing Environment

- Synchronous Clock Timing (AmZ8000 systems).
- Delay-line timing for maximum performance.

Operation with Any RAM Refresh Mode

- 128 of 256 Line Refresh

All Refresh Modes

- Burst Refresh
- Hidden (transparent) Refresh
- Cycle Steal Refresh

Am2960 Family Product Summary

Am2960 • AmZ8160 Error Detection and Correction (EDC)

- High-speed 16-bit slice expandable to 64 bits
- Single-bit correction/double-bit detection
- Byte-op controls
- Initialization and diagnostics built-in

Am2961/62 • AmZ8161/62 EDC Data Bus Buffer

- EDC interface between RAM, EDC and data bus
- 24mA bus drive with three-state control
- Separated RAM I/O with undershoot protection
- Bus latches for byte-op or multiplexed buses

AmZ8163 EDC and Refresh Control for AmZ8000 Systems

- RAS/MUX/CAS timing control for AmZ8164
- EDC control for word or byte read and write
- Memory/refresh request arbitration
- Refresh timer and control independent of CPU

Am2964 • AmZ8164 Dynamic Memory Control (DMC)

- 16-bit address for up to 64K RAMs
- Refresh Counter for 128- or 256-line refresh
- 3-port 8-bit Schottky speed address MUX
- RAS and CAS paths on-chip for minimum skew

Am2965/66 • AmZ8165/66 Octal Dynamic RAM Drivers

- −0.5V maximum undershoot
- V_{OH}/I_{OH} specs for MOS with no external resistors
- t_{PLH}/t_{PHL} min and max specs for 50pF and 500pF
- Pin-compatible with 'S240/244

Am2960
Fast Error Detection and Correction for Memories

Corrects All Single-Bit Errors

Corrects all single bit errors. Detects all double and some triple bit errors.

Expandable

One Am2960 provides Error Detection and Correction for 16-bits. Two Am2960s handle 32 bits; four Am2960s handle 64 bits.

Fast

Worst case 32 nanoseconds for error detect and 65 nanoseconds for error correct (16 bits).

Latches Built-In

Check Bit, Data, and Diagnostic latches are built-in to save MSI.

Flexible

Can be used with Am2900-based designs, the AmZ8000 or other processors.

Diagnostics Built-In

Logic on-chip for device test and software-controlled diagnostics.

Increases Memory Reliability

And can significantly reduce field maintenance costs.

A Must for 64K RAMs

Alpha error rates are several times higher for 64K RAMs than 16Ks.

Also available as the AmZ8160 for AmZ8000 Systems

Am2960 EDC

Cascadable 16-Bit Error Detection and Correction Unit

DISTINCTIVE CHARACTERISTICS

- **Boosts Memory Reliability**
  Corrects all single-bit errors. Detects all double and some triple-bit errors. Reliability of dynamic RAM systems is increased more than 60-fold.
- **Very High Speed**
  Perfect for MOS microprocessor, minicomputer, and mainframe systems.
  - Data in to error detect: 32ns worst case.
  - Data in to corrected data out: 65ns worst case.

  High performance systems can use the Am2960 EDC in check-only mode to avoid memory system slowdown.
- **Replaces 25 to 50 MSI chips**
  All necessary features are built-in to the Am2960 EDC, including diagnostics, data in, data out, and check bit latches.
- **Handles Data Words From 8 to 64 Bits**
  The Am2960 EDC cascades: 1 EDC for 8 or 16 bits, 2 for 32 bits, 4 for 64 bits.
- **Easy Byte Operations**
  Separate byte enables on the data out latch simplify the steps and cuts the time required for byte writes.
- **Diagnostics Built-In**
  The processor may completely exercise the EDC under software control to check for proper operation of the EDC.

GENERAL DESCRIPTION

The Am2960 Error Detection and Correction Unit (EDC) contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the Am2960 will correct any single bit error and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The Am2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Am2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product is supplied in a 48 lead hermetic DIP package.

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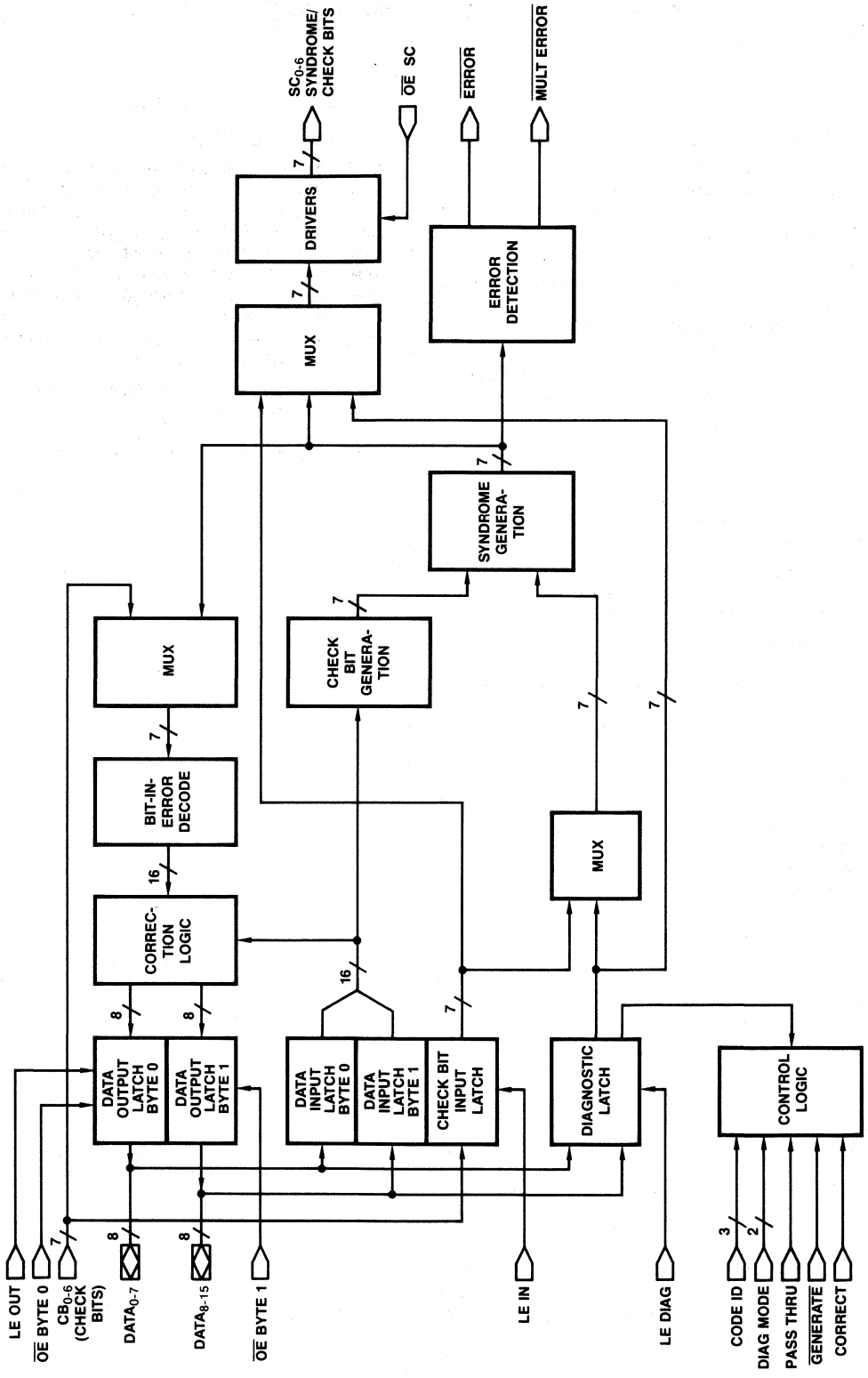
TABLE OF CONTENTS

BLOCK DIAGRAM



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EDC Architecture

The EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics.

As shown in the block diagram, the device consists of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

Data Input Latch

16 bits of data are loaded from the bidirectional DATA lines under control of the Latch Enable input, LE IN. Depending on the control mode the input data is either used for check bit generation or error detection/correction.

Check Bit Input Latch

Seven check bits are loaded under control of LE IN. Check bits are used in the Error Detection and Error Correction modes.

Check Bit Generation Logic

This block generates the appropriate check bits for the 16 bits of data in the Data Input Latch. The check bits are generated according to a modified Hamming code.

Syndrome Generation Logic

In both Error Detection and Error Correction modes, this logic block compares the check bits read from memory against a newly generated set of check bits produced for the data read in from memory. If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors) the syndrome bits will be all zeroes. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit-in-error.

Error Detection Logic

This section decodes the syndrome bits generated by the Syndrome Generation Logic. If there are no errors in either the input data or check bits, the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs remain HIGH. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ go LOW.

Error Correction Logic

For single errors, the Error Correction Logic complements (corrects) the single data bit in error. This corrected data is loadable into the Data Output Latch, which can then be read onto the bidirectional data lines. If the single error is one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed the EDC must be switched to Generate Mode.

Data Output Latch

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE OUT. The Data Output Latch may also be loaded directly from the Data Input Latch under control of the PASS THRU control input.

The Data Output Latch is split into two 8-bit (byte) latches which may be enabled independently for reading onto the bidirectional data lines.

Diagnostic Latch

This is a 16-bit latch loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. The Diagnostic Latch contains check bit information in one byte and control information in the other byte. The Diagnostic Latch is used for driving the device when in Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

Control Logic

The control logic determines the specific mode the device operates in. Normally the control logic is driven by external control inputs. However, in Internal Control Mode, the control signals are instead read from the Diagnostic Latch.

PIN DEFINITIONS

$DATA_{0-15}$ 16 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.

CB_{0-6} Seven Check Bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32 and 64-bit configurations.

LE IN Latch Enable – Data Input Latch. Controls latching of the input data. When HIGH the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.

$\overline{\text{GENERATE}}$ Generate Check Bits input. When this input is LOW the EDC is in the Check Bit Generate Mode. When HIGH the EDC is in the Detect Mode or Correct Mode.

In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs.

In the Detect or Correct Modes the EDC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected – corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.

SC_{0-6} Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.

$\overline{\text{OE SC}}$ Output Enable – Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.

$\overline{\text{ERROR}}$ Error Detected output. When the EDC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.)

$\overline{\text{MULT ERROR}}$ Multiple Errors Detected output. When the EDC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH this indicates that either one or no errors have been detected. In Generate mode, $\overline{\text{MULT ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{MULT ERROR}}$ must be externally implemented.)

CORRECT Correct input. When HIGH this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it onto the Data Output Latch. When LOW the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.

LE OUT Latch Enable – Data Output Latch. Controls the latching of the Data Output Latch. When LOW the Data Output Latch is latched to its previous state. When HIGH the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDC is in Generate Mode.

$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1 Output Enable – Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW these lines enable the Data Output Latch and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.

PASS THRU Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.

DIAG $MODE_{0-1}$ Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDC.

CODE ID_{0-2} Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32 and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.

LE DIAG Latch Enable – Diagnostic Latch. When HIGH the Diagnostic Latch follows the 16-bit data on the input lines. When LOW the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU.

FUNCTIONAL DESCRIPTION

The EDC contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code. Operating on data read from memory, the EDC will correct any single-bit error, and will detect all double and some triple-bit errors. The Am2960 may be configured to operate on 16-bit data words (with 6 check bits), 32-bit data words (with 7 check bits) and 64-bit data words (with 8 check bits). In fact the EDC can be configured to work on data words from 8 to 64 bits. In all configurations, the device makes the error syndrome bits available on separate outputs for error data logging.

Code and Byte Specification

The EDC may be configured in several different ways and operates differently in each configuration. It is necessary to indicate to the device what size data word is involved and which bytes of the data word it is processing. This is done with input lines CODE ID_{0-2}, as shown in Table I. The three modified Hamming codes referred to in Table I are:

- 16/22 – 16 data bits
  – 6 check bits
  – 22 bits in total.
- 32/39 code – 32 data bits
  – 7 check bits
  – 39 bits in total.
- 64/72 code – 64 data bits
  – 8 check bits
  – 72 bits in total.

CODE ID input 001 (ID_2, ID_1, ID_0) is a special code used to operate the device in Internal Control Mode (described later in this section).

Control Mode Selection

The device control lines are $\overline{\text{GENERATE}}$, CORRECT, PASS THRU, DIAG $MODE_{0-1}$ and CODE ID_{0-2}. Table III indicates the operating modes selected by various combinations of the control line inputs.

Diagnostics

Table II shows specifically how DIAG $MODE_{0-1}$ select between normal operation, initialization and one of two diagnostic modes.

The Diagnostic Modes allow the user to operate the EDC under software control in order to verify proper functioning of the device.

Check and Syndrome Bit Labeling

The check bits generated in the EDC are designated as follows:

- 16-bit configuration – CX C0, C1, C2, C4, C8;
- 32-bit configuration – CX, C0, C1, C2, C4, C8, C16;
- 64-bit configuration – CX, C0, C1, C2, C4, C8, C16, C32.

Syndrome bits are similarly labeled SX through S32. There are only 6 syndrome bits in the 16-bit configuration, 7 for 32 bits and 8 syndrome bits in the 64-bit configuration.

Initialize Mode

The inputs of the Data Output Latch are forced to zeroes. The check bit outputs (SC) are generated to correspond to the all-zero data. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in the Initialize Mode.

Initialize Mode is useful after power up when RAM contents are random. The EDC may be placed in initialize mode and its' outputs written in to all memory locations by the processor.

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TABLE I. HAMMING CODE AND SLICE IDENTIFICATION.

CODE ID_2	CODE ID_1	CODE ID_0	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE II. DIAGNOSTIC MODE CONTROL.

DIAG $MODE_1$	DIAG $MODE_0$	Diagnostic Mode Selected
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Detect/Correct.** In the Detect or Correct Mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	**Initialize.** The outputs of the Data Input Latch are forced to zeroes (and latched upon removal of the Initialize Mode) and the check bits generated correspond to the all-zero data.

HAMMING CODE SELECTION

The Am2960 EDC uses a modified Hamming Code that allows 1) the EDC to be cascaded, 2) all double errors to be detected, 3) the gross error conditions of all 0s or 1s to be detected.

The error correction code can be selected independent of the processor with the exception of diagnostics software.

Diagnostic software run by a processor to checkout the EDC system must know specifically which code is being used. This is only a problem when the EDC replaces an existing MSI implementation on an existing computer. In this case, the computer's software must first determine which of two codes (the old one used by the MSI implementation or the new one used by the EDC) is used by the computer's memory system.

This is easily determined by writing a test data word into memory and then examining whether the generated check bits are typical of the old or the new code. From then on the software runs only the diagnostic appropriate for the code used on that particular computer's memory system.

TABLE III. Am2960 OPERATING MODES

Operating Mode	Diagnostic Mode**		$\overline{\text{GENERATE}}$	
	DM_1	DM_0	0	1
Normal	0	0	Generate	Correct*
Diagnostic Generate	0	1	Diagnostic Generate	Correct*
Diagnostic Correct	1	0	Generate	Diagnostic Correct*
Initialize	1	1	Initialize	Initialize
Pass Thru	When PASS THRU is asserted the Operating Mode is defaulted to the Pass Thru Mode.			

*Correct if the CORRECT Input is HIGH, Detect if the CORRECT Input is LOW.
**In Code $ID_{2\text{-}0}$ 001 (ID_2, ID_1, ID_0) DM_1 and DM_0 are taken from the Diagnostic Latch.

FUNCTIONAL DESCRIPTION – 16-BIT DATA WORD CONFIGURATION

The 16-bit format consists of 16 data bits, 6 check bits and is referred to as 16/22 code (see Figure 5.)

The 16-bit configuration is shown in Figure 6.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs SC_{0-5} (SC_6 is a logical one, or high).

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table IV. Each check bit is generated as either an XOR or XNOR of eight of the 16 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR is an odd parity check bit.

Figure 1 shows the data flow in the Generate Mode.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, $\overline{\text{MULT ERROR}}$ goes LOW. Both error indicators are HIGH if there are no errors.

Also available on device outputs SC_{0-5} are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table V gives the chart for decoding the syndrome bits generated by the 16-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8 were 101001 this would be decoded to indicate that there is a single-bit error at data bit 9). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. (see Figure 2.) If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction. If check bit correction is desired, this can be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs SC_{0-5}. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in this mode.

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table VI shows the loading definitions for the DATA lines.

Diagnostic Generate
Diagnostic Detect
Diagnostic Correct

These are special diagnostic modes selected by DIAG $MODE_{0-1}$ where either normal check bit inputs or outputs are substituted for by check bits loaded into the Diagnostic Latch. See Table III for details. Figures 3 and 4 illustrate the flow of data during the two diagnostic modes.

Internal Control Mode

This mode is selected by CODE ID_{0-2} input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode, the EDC takes the CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU control signals from the internal Diagnostic Latch rather than from the external input lines.

Table VI gives the format for loading the Diagnostic Latch.

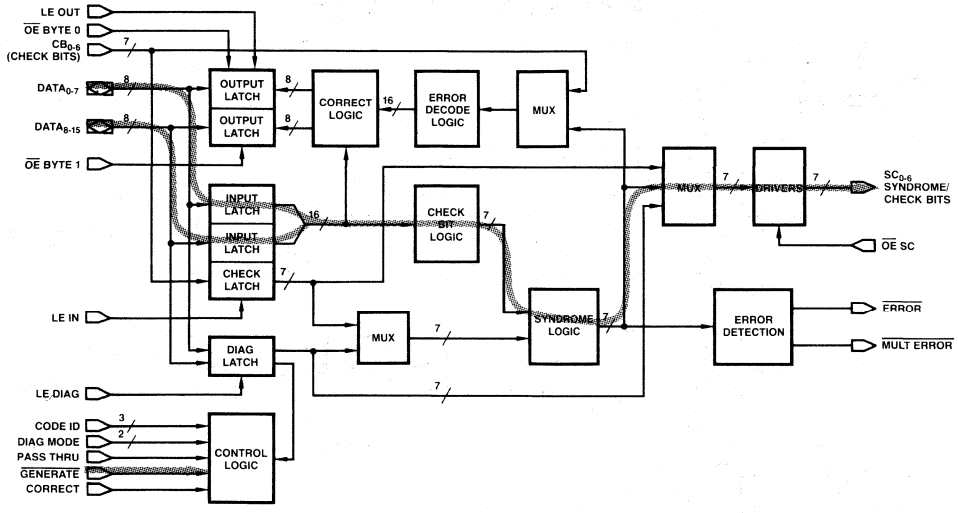


Figure 1. Check Bit Generation

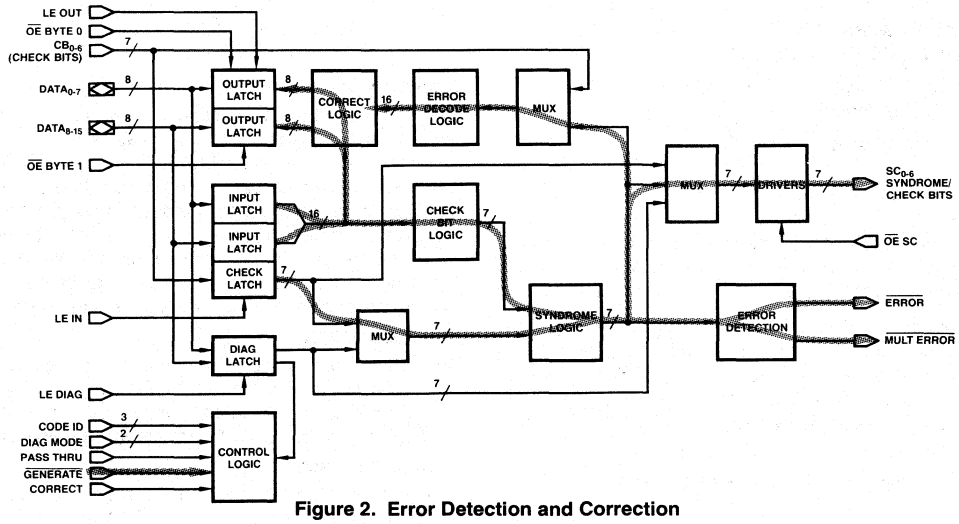


Figure 2. Error Detection and Correction

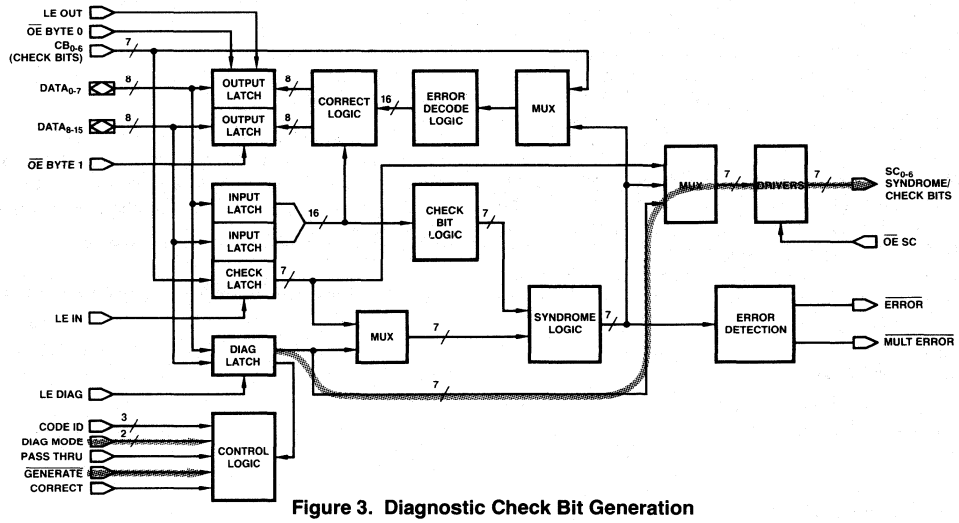


Figure 3. Diagnostic Check Bit Generation

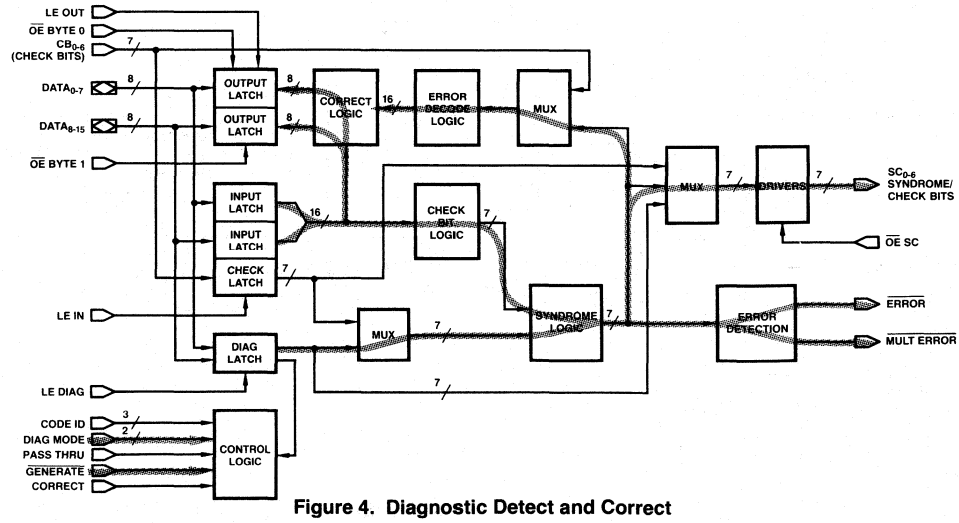
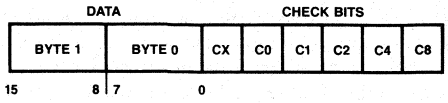


Figure 4. Diagnostic Detect and Correct



Uses Modified Hamming Code 16/22
- 16 data bits
- 6 check bits
- 22 bits in total

Figure 5. 16-Bit Data Format

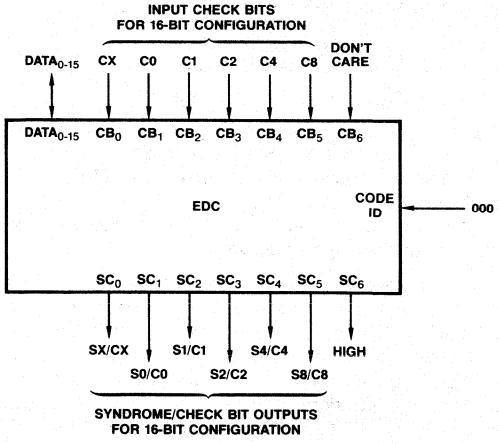


Figure 6. 16-Bit Configuration

TABLE IV. 16-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART.

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

TABLE V. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits SX	S0	S1	S8	0	1	0	1	0	1	0	1
			S4	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1
0	0	0		*	C8	C4	T	C2	T	T	M
0	0	1		C1	T	T	15	T	13	7	T
0	1	0		C0	T	T	M	T	12	6	T
0	1	1		T	10	4	T	0	T	T	M
1	0	0		CX	T	T	14	T	11	5	T
1	0	1		T	9	3	T	M	T	T	M
1	1	0		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

* – no errors detected
Number – the location of the single bit-in-error
T – two errors detected
M – three or more errors detected

TABLE VI. DIAGNOSTIC LATCH LOADING – 16-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID 0
9	CODE ID 1
10	CODE ID 2
11	DIAG MODE 0
12	DIAG MODE 1
13	CORRECT
14	PASS THRU
15	Don't Care

7

FUNCTIONAL DESCRIPTION – 32-BIT DATA WORD CONFIGURATION

The 32-bit format consists of 32 data bits, 7 check bits and is referred to as 32/39 code (see Figure 7).

The 32-bit configuration is shown in Figure 8.

The upper EDC (Slice 0/1) handles the least significant bytes 0 and 1 – the external DATA lines 0 to 15 are connected to the same numbered inputs of the upper device. The lower EDC (Slice 2/3) handles the most significant bytes 2 and 3 – the external DATA lines for bits 16 to 31 are connected to inputs $DATA_0$ through $DATA_{15}$ respectively.

The valid syndrome and check bit outputs are those of Slice 2/3 as shown in the diagram. In Correct Mode these must be read into Slice 0/1 via the CB inputs and are selected by the MUX as inputs to the bit-in-error decoder (see block diagram), thus requiring external buffering and output enabling of the check bit lines as shown. The $\overline{OE}$ SC signal can be used to control enabling of check bit inputs – when syndrome outputs are enabled, the external check bit inputs will be disabled.

The valid $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs are those of the Slice 2/3. The $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs of Slice 0/1 are unspecified. All of the latch enables and control signals must be input to both of the devices.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs $SC_{0\text{-}6}$ of Slice 2/3.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table X. Check bits are generated as either an XOR or XNOR of 16 of the 32 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If two or more errors are detected, $\overline{MULT\ ERROR}$ goes LOW. Both error indicators are HIGH if there are no errors. The valid $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signals are those of Slice 2/3 – those of Slice 0/1 are undefined.

Also available on Slice 2/3 outputs $SC_{0\text{-}6}$ are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table VII gives the chart for decoding the syndrome bits generated for the 32-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8/S16 were 0010011 this would be decoded to indicate that there is a single-bit error at data bit 25). If no error is detected the syndrome bits will be all zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction – if desired this would be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

For data correction, both Slices 0/1 and 2/3 require access to the syndrome bits on Slice 2/3's outputs $SC_{0\text{-}6}$. Slice 2/3 has access to these syndrome bits through internal data paths, but for Slice 0/1 they must be read through the inputs $CB_{0\text{-}6}$. The device connections for this are shown in Figure 8. When in Correct Mode the SC outputs must be enabled so that they are available for reading in through the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs $SC_{0\text{-}6}$ of Slice 2/3. $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ are forced HIGH in this mode.

TABLE VII. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

* – no errors detected
Numbers – number of the single bit-in-error
T – two errors detected
M – three or more errors detected

Uses Modified Hamming Code 32/39
- 32 data bits
- 7 check bits
- 39 bits in total

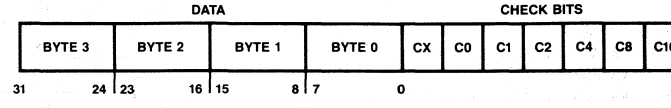


Figure 7. 32-Bit Data Format

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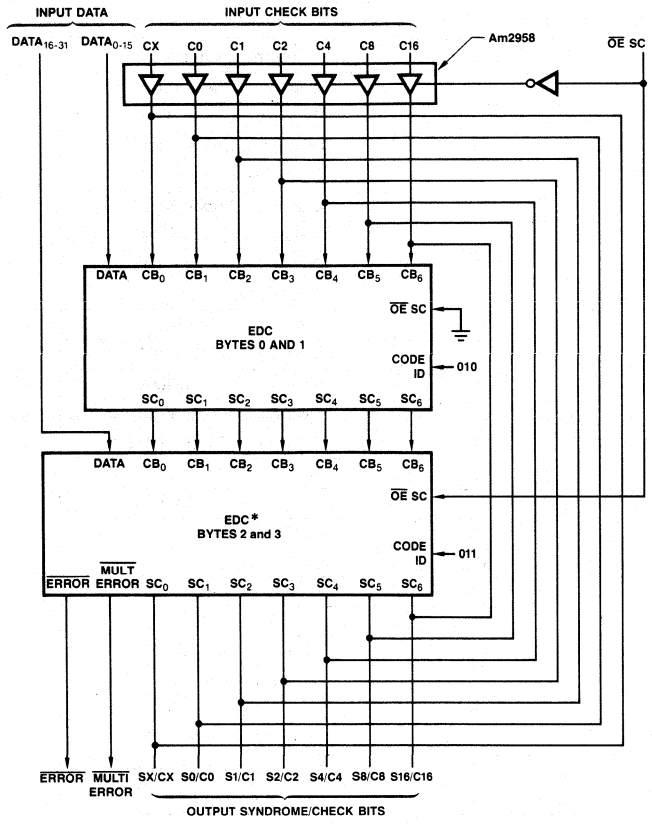


*Check Bit Latch is Forced Transparent in this Code ID Combination for this Slice.

Figure 8. 32-Bit Configuration

TABLE VIII. KEY AC CALCULATIONS FOR THE 32-BIT CONFIGURATION

32-Bit Propagation Delay		Component Delay from Am2960 AC Specifications, Table C
From	**To**	
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA In	Corrected DATA Out	(DATA to SC) + (CB to SC, CODE ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID 011)
DATA	$\overline{\text{MULT ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)

TABLE IX. DIAGNOSTIC LATCH LOADING – 32-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU
31	Don't Care

TABLE X. 32-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART.

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the sixteen data bits noted by an "X" in the table.

FUNCTIONAL DESCRIPTION – 64-BIT DATA WORD CONFIGURATION

The 64-bit format consists of 64 data bits, 8 check bits and is referred to as 64/72 code (see Figure 9.).

The configuration to process 64-bit format is shown in Figure 6. In this configuration a portion of the syndrome generation and error detection is implemented externally of the EDCs in MSI. For error correction the syndrome bits generated must be read back into all four EDCs through the CB inputs. This necessitates the check bit buffering shown in the connection diagram of Figure 10. The $\overline{OE}$ SC signal can control the check bit enabling – when syndrome bit outputs are enabled the external check bit lines will be disabled so that the syndrome bits may be read onto the CB inputs.

The error detection signals for the 64-bit configuration differ from the 16 and 32-bit configurations. The $\overline{ERROR}$ signal functions the same: it is LOW if one or more errors are detected, and HIGH if no errors are detected. The DOUBLE ERROR signal is HIGH if and only if a double-bit error is detected – it is LOW otherwise. All of the $\overline{MULT\ ERROR}$ outputs of the four devices are valid. $\overline{MULT\ ERROR}$ is LOW for all three ERROR cases and some DOUBLE ERROR combinations. (See TOME definition in Functional Equations section.) It is HIGH if either zero or one errors are detected.

This is a different meaning for $\overline{MULT\ ERROR}$ than in other configurations.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated appear at the outputs of the XOR gates as indicated in Figure 10.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table XII. Check bits are generated as either an XOR or XNOR of 32 of the 64 bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If exactly two errors are detected, DOUBLE ERROR goes HIGH. If three or more errors are detected, $\overline{MULT\ ERROR}$ goes LOW – the $\overline{MULT\ ERROR}$ output of any of the four EDCs may be used.

Available as XOR gate outputs are the generated syndrome bits (see Figure 10). The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table XIII gives the chart for encoding the syndrome bits generated for the 64-bit configuration (as an example, if the syndrome bits SX/S1/S2/S4/S8/S16/S32 were 00100101 this would be decoded to indicate that there is a single-bit error at data bit 41). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single bit error is a check bit there is no automatic correction. Check bit correction can be done by placing the device in generate mode to produce a correct check bit sequence for the data in the Data Input Latch.

To perform the correction step, all four slices require access to the syndrome bits which are generated externally of the devices. This access is provided by reading the syndrome bits in through the CB inputs where they are selected as inputs to the bit-in-error decoder by the multiplexer (see block diagram). The device connections for this are shown in Figure 10. When in Correct Mode the SC outputs must be enabled so that the syndrome bits are available at the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch, and the contents of the Check Bit Input Latch are passed through the external XOR network and appear inverted at the XOR gate outputs labeled CX to C32 (see Figure 10).

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table XIV shows the loading definitions for the DATA lines.

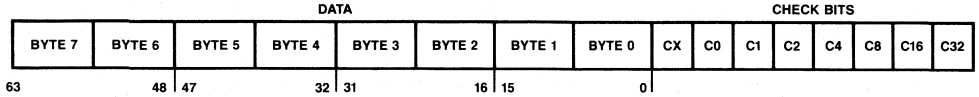
Diagnostic Generate
Diagnostic Detect
Diagnostic Correct

These are special diagnostic modes selected by DIAG $MODE_{0\text{-}1}$ where either normal check bit inputs or outputs are substituted for by check bits from the Diagnostic Latch. See Table II for details.

Internal Control Mode

This mode is selected by CODE $ID_{0\text{-}2}$, input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode the EDC takes the CODE $ID_{0\text{-}2}$, DIAG $MODE_{0\text{-}1}$, CORRECT and PASS THRU signals from the internal Diagnostic Latch rather than from the external control lines. Table XIV gives format for loading the Diagnostic Latch.



Uses Modified Hamming Code 64/72
- 64 data bits
- 8 check bits
- 72 bits in total

Figure 9. 64-Bit Data Format

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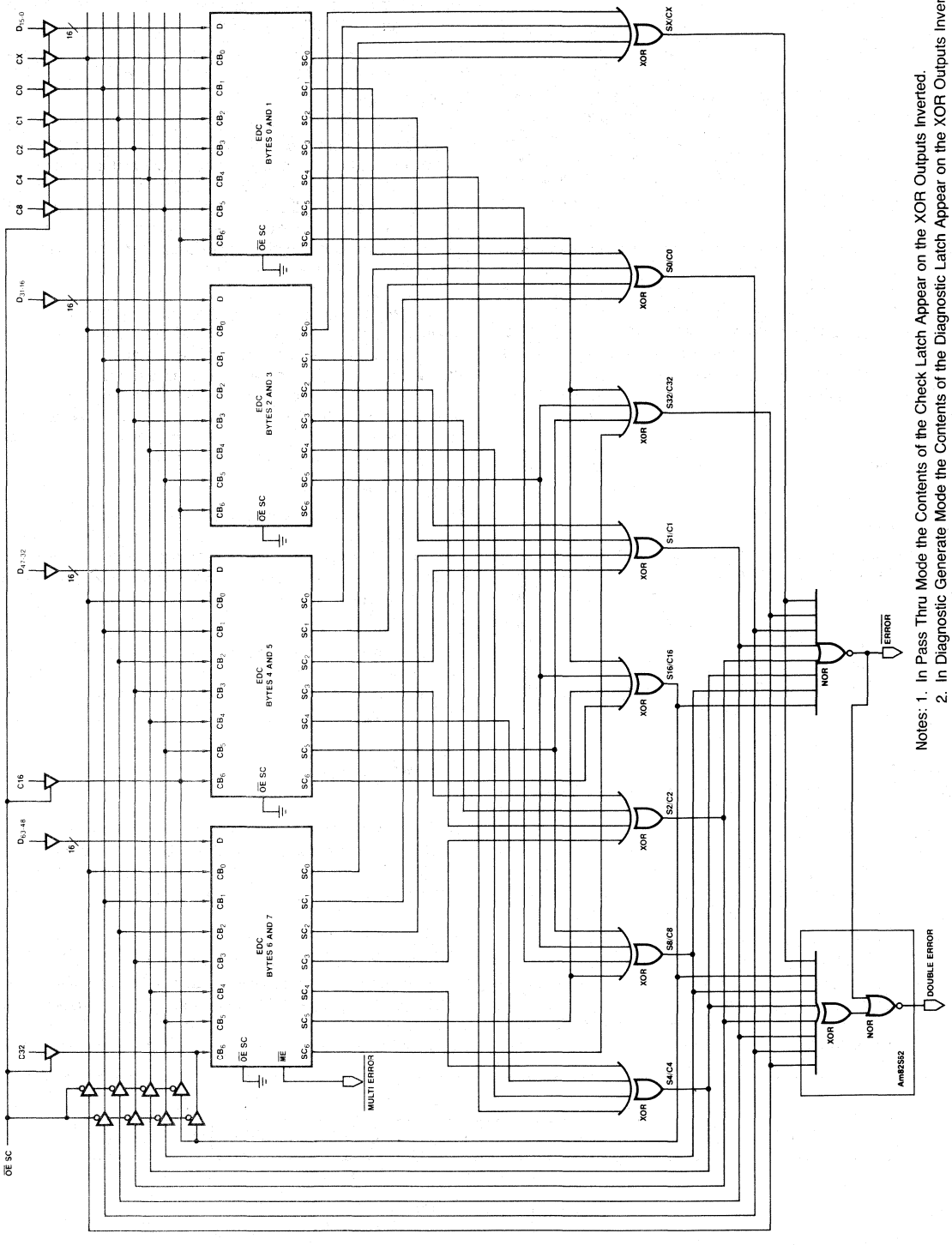

Notes: 1. In Pass Thru Mode the Contents of the Check Latch Appear on the XOR Outputs Inverted.
2. In Diagnostic Generate Mode the Contents of the Diagnostic Latch Appear on the XOR Outputs Inverted.

Figure 10. Am2960 — 64-Bit Data Configuration

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TABLE XI. KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-Bit Propagation Delay		Component Delays from Am2960 AC Specifications, Table C (plus MSI)
From	To	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA In	Corrected DATA Out	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64 Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

TABLE XII. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

TABLE XIII. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits SX	S0	S1	S2	S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0		*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1		C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0		C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1		T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0		C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1		T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0		T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1		16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0		CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1		T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0		T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1		M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0		T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1		17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0		M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1		T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

* – no errors detected
Number – the number of the single bit-in-error
T – two errors detected
M – more than two errors detected

TABLE XIV. DIAGNOSTIC LATCH LOADING – 64-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU

Data Bit	Internal Function
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5 – CODE ID 0
41	Slice 4/5 – CODE ID 1
42	Slice 4/5 – CODE ID 2
43	Slice 4/5 – DIAG MODE 0
44	Slice 4/5 – DIAG MODE 1
45	Slice 4/5 – CORRECT
46	Slice 4/5 – PASS THRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7 – CODE ID 0
57	Slice 6/7 – CODE ID 1
58	Slice 6/7 – CODE ID 2
59	Slice 6/7 – DIAG MODE 0
60	Slice 6/7 – DIAG MODE 1
61	Slice 6/7 – CORRECT
62	Slice 6/7 – PASS THRU
63	Don't Care

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Case) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for high Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0 mA

OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2960DC, XC	COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V, MAX = 5.25V)
Am2960DM, FM, XM	MIL	T_C = −55 to +125°C	V_{CC} = 5.0V ± 10%	(MIN = 4.50V, MAX = 5.50V)

DC CHARACTERISTICS

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.8mA	COM'L	2.7			Volts
				MIL	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA				0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	$DATA_{0-15}$				−410	μA
			All Other Inputs				−360	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$DATA_{0-15}$				70	μA
			All Other Inputs				50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} MAX	$DATA_{0-15}$	V_O = 2.4			70	μA
				V_O = 0.5			−410	
			SC_{0-6}	V_O = 2.4			50	
				V_O = 0.5			−50	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = V_{CC} MAX +0.5V, V_O = 0.5V			−25		−85	mA
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX		T_A = 25°C		275	390	mA
			COM'L	T_A = 0 to +70°C			400	
				T_A = +70°C			365	
			MIL	T_C = −55 to +125°C			400	
				T_C = +125°C			345	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
5. "MIL" = Am2960XM, DM, FM. "COM'L" = Am2960XC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \leq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

1. Am2960 Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2960 over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960DC, XC.

A. Combinational Propagation Delays
C_L = 50pF

From Input \ To Output	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	32	65*	32	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	28	56	29	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	45	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	–	45	–	–
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASS THRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE IN (From latched to transparent)	39	72*	39	59
LE OUT (From latched to transparent)	–	31	–	–
LE DIAG (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE DIAG (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN	6	7
CB_{0-6}	LE IN	5	6
$DATA_{0-15}$	LE OUT	44	5
CB_{0-6} (CODE ID 000, 011)	LE OUT	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT	27	0
$\overline{GENERATE}$	LE OUT	42	0
CORRECT	LE OUT	26	1
DIAG MODE	LE OUT	69	0
PASS THRU	LE OUT	26	0
CODE ID_{2-0}	LE OUT	81	0
LE IN	LE OUT	51	5
$DATA_{0-15}$	LE DIAG	6	8

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$	30	30
$\overline{OE}$ SC	SC_{0-6}	30	30

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	15

7

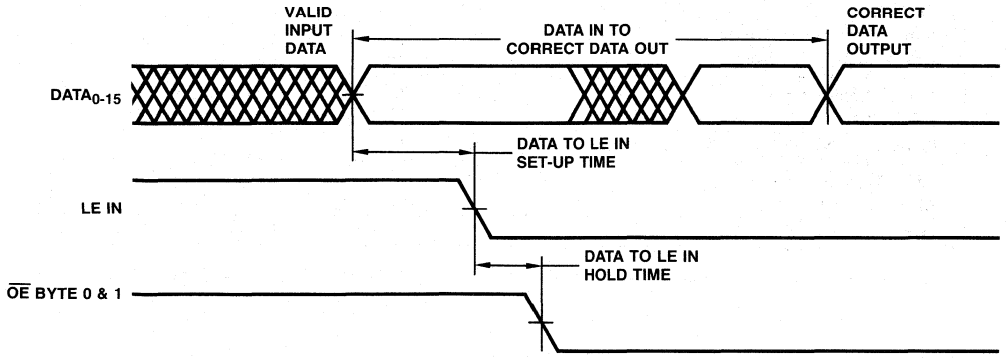


Figure D.

1. Am2960 Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2960 over the military operating range of −55 to +125°C case temperature, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960DM, FM, XM.

A. Combinational Propagation Delays
C_L = 50pF

From Input \ To Output	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	35	73*	36	56
CB_{0-6} ($CODE\ ID_{2-0}$ 000, 011)	30	61	31	50
CB_{0-6} ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111)	30	50	31	37
$\overline{GENERATE}$	38	69	41	62
CORRECT (Not Internal Control Mode)	–	49	–	–
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASS THRU (Not Internal Control Mode)	39	51	34	54
$CODE\ ID_{2-0}$	69	100	68	90
LE IN (From latched to transparent)	44	82*	43	66
LE OUT (From latched to transparent)	–	33	–	–
LE DIAG (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE DIAG (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN	7	7
CB_{0-6}	LE IN	5	7
$DATA_{0-15}$	LE OUT	50	5
CB_{0-6} (CODE ID 000, 011)	LE OUT	38	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT	30	0
$\overline{GENERATE}$	LE OUT	46	0
CORRECT	LE OUT	28	1
DIAG MODE	LE OUT	84	0
PASS THRU	LE OUT	30	0
$CODE\ ID_{2-0}$	LE OUT	89	0
LE IN	LE OUT	59	5
$DATA_{0-15}$	LE DIAG	7	9

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$	35	35
$\overline{OE}$ SC	SC_{0-6}	35	35

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	15

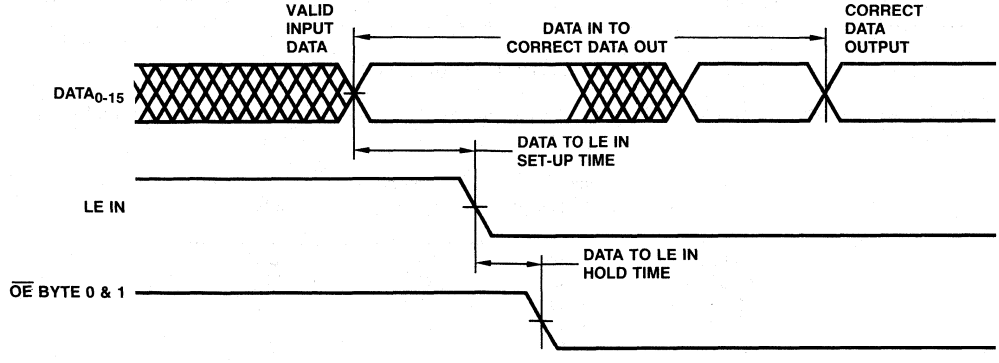
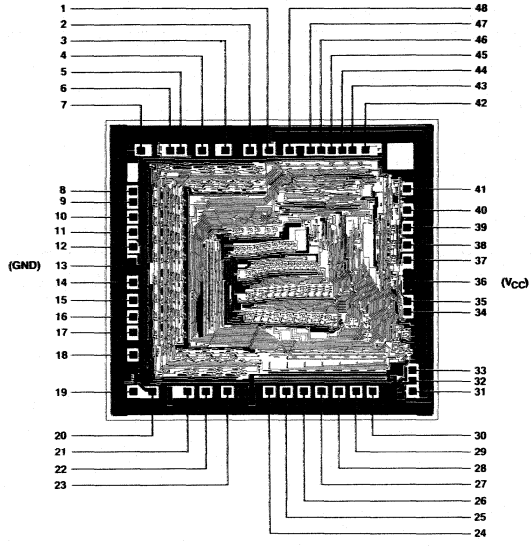


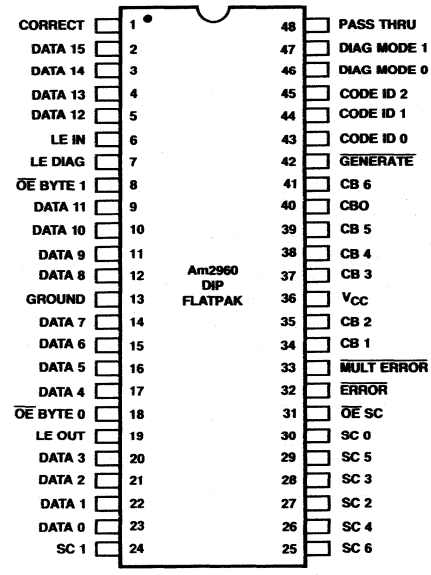
Figure D.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.200" X 0.183"

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2960 Order Number (Note 3)	Package Type Order Number	Operating Range (Note 1)	Screening Level (Note 2)
AM2960DC	D-48	C	C-1
AM2960DC-B	D-48	C	B-2 (Note 4)
AM2960DM	D-48	M	C-3
AM2960DM-B	D-48	M	B-3
AM2960FM	F-48	M	C-3
AM2960FM-B	F-48	M	B-3
AM2960XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2960XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

TEST OUTPUT LOAD CONFIGURATION FOR Am2960

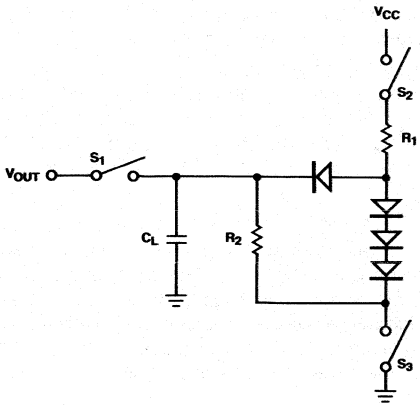


Figure 11. Three-State Outputs

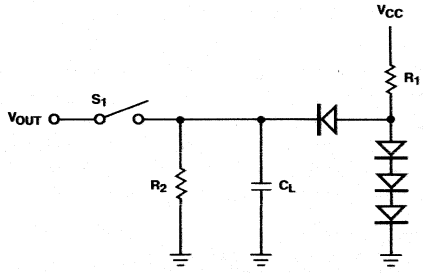


Figure 12. Normal Outputs

Notes:
1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function test and all A.C. tests, except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. R_2 = 1K for three-state output.
   R_2 is determined by the I_{OH} at V_{OH} = 2.4V for non-three-state outputs.
5. R_1 is determined by I_{OL} (MIL) with V_{CC} = 5.0V minus the current to ground through R_2.
6. C_L = 5.0 pF for output disable tests.

TEST OUTPUT LOADS

Pin #	Pin Label	Test Circuit	R_1	R_2
–	D_0-D_{15}	Fig. 11	430Ω	1kΩ
24-30	SC_0-SC_6	Fig. 11	430Ω	1kΩ
32	$\overline{\text{ERROR}}$	Fig. 12	470Ω	3kΩ
33	$\overline{\text{MULTERROR}}$	Fig. 12	470Ω	3kΩ

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS

Byte Write

Byte operations are increasingly common for 16 and 32-bit processors. These complicate memory operations because check bits are generated for a complete 16 or 32 or 64-bit memory word, not for a single byte.

To write a byte into memory with EDC requires the following steps:

- Latch the byte into the Am2961/62 bus buffers (Figure 13)
- Read the complete data word from memory (Figure 13)
- Correct the complete data word if necessary (Figure 13)
- Insert the byte to be written into the data word (Figure 14)
- Generate new check bits for the entire data word (Figure 14)
- Store the data word back into memory (Figure 14)

(In fact these steps must be taken for any piece of data being written into memory that is not as wide as a full memory word).

The Am2960 EDC is designed with the intent of keeping byte operations simple in EDC systems. The EDC has separate output enables for each byte in the Data Output Latch. As shown in figures 13 and 14, this allows the data word to be read from memory, the new byte to be inserted among the old, and new check bits to be generated using less time and less hardware than if separate byte enables were not available.

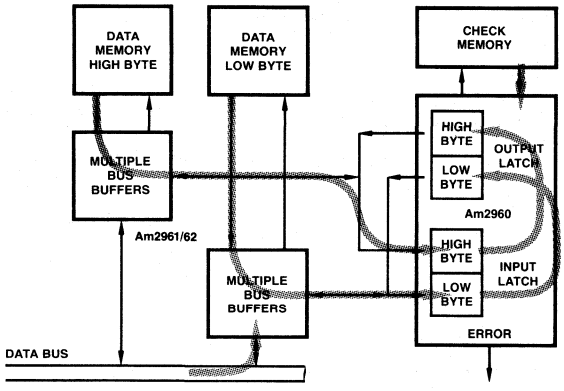


Figure 13. Byte Write, Phase 1: Read Out the Old Word and Correct

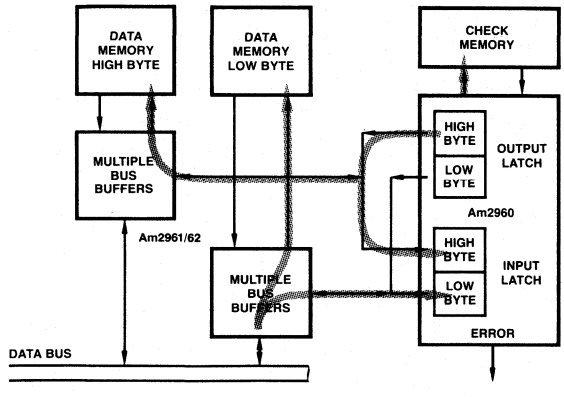


Figure 14. Byte Write, Phase 2: Insert the New Byte, Generate Checks and Write Into Memory

Diagnostics

EDC is used to boost the reliability of the overall system. It is necessary to also be able to check the operation of the EDC itself. For this reason the EDC has an internal control mode, a diagnostic latch, and two diagnostic modes.

To check that the EDC is functioning properly, the processor can put the EDC under software control by setting CODE ID_{2-0} to 001. This puts the EDC into Internal Control Mode. In Internal Control Mode the EDC is controlled by the contents of the Diagnostic Latch which is loaded from the DATA inputs under processor control.

The EDC is set into CORRECT Mode. The processor loads in a known set of check bits into the Diagnostic Latch, a known set of data bits into the Data In Latch, and forces data errors. The output of the EDC (syndromes, error flags, corrected data) is then compared against the expected responses. By exercising the EDC with a string of data/check combinations and comparing the output against the expected responses, the EDC can be fully checked out.

Eight Bit Data Word

Eight bit MOS microprocessors can use EDC too. Only five check bits are required. The EDC configuration for eight bits is shown in Figure 15. It operates as does the normal 16-bit configuration with the upper byte fixed at 0.

Check bit overhead for 8-bit data words can be reduced two ways. See the sections "Single Error Correction Only" and "Reducing Check Bit Overhead."

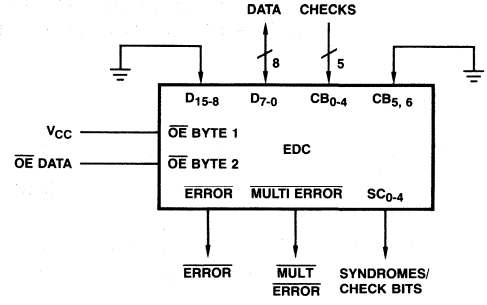


Figure 15. 8-Bit Configuration

Other Word Widths

EDC on data words other than 8, 16, 32, of 64 bits can be accomplished with the Am2960. In most cases the extra data bits can be forced to a constant, and EDC will procede as normal. For example a 24-bit data word is shown in Figure 16.

Single Error Correction Only

The EDC normally corrects all single bit errors *and* detects all double bit and some triple bit errors. To save one check bit per word the ability to detect double bit errors can be sacrificed – single errors are still detected and corrected.

Data Bits	Check Bits Required	
	Single Error Correction Only	Single Error Correct & Double Error Detect
8	4	5
16	5	6
32	6	7
64	7	8

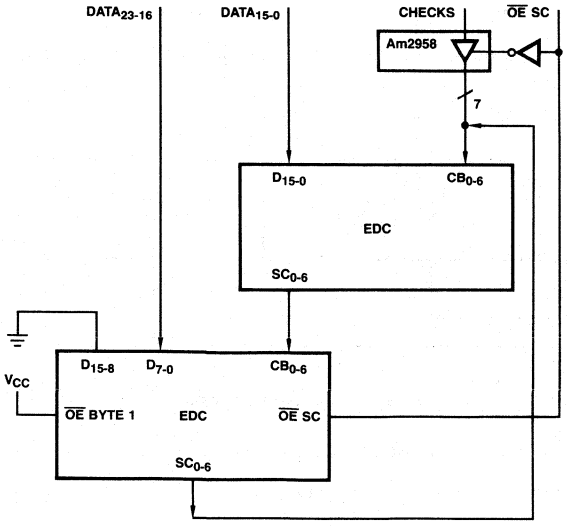


Figure 16. 24-Bit Configuration

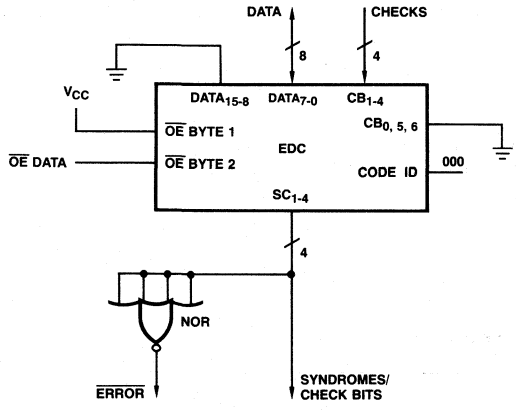


Figure 17. 8-Bit Single Error Correction Only

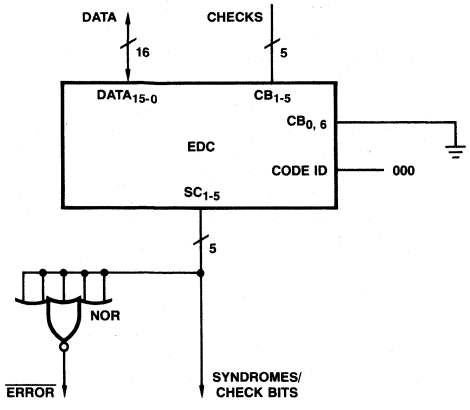
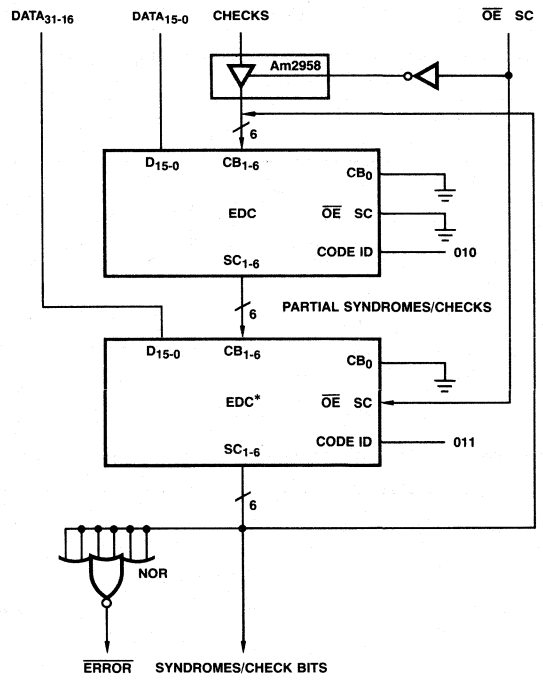


Figure 18. 16-Bit Single Error Correction Only



*The Code ID Combination for this Slice Forces the Check Bit Latch Transparent.

Figure 19. 32-Bit Single Correct Only

Figures 17, 18, 19, 20 show single error correction only configurations for 8, 16, 32, and 64-bit data words respectively.

Check Bit Correction

The EDC detects single bit errors whether the error is a data bit or a check bit. Data bit errors are automatically corrected by the EDC. To generate corrected check bits once a single check bit error is detected, the EDC need only be switched to GENERATE mode (data in the DATA INPUT LATCH is valid).

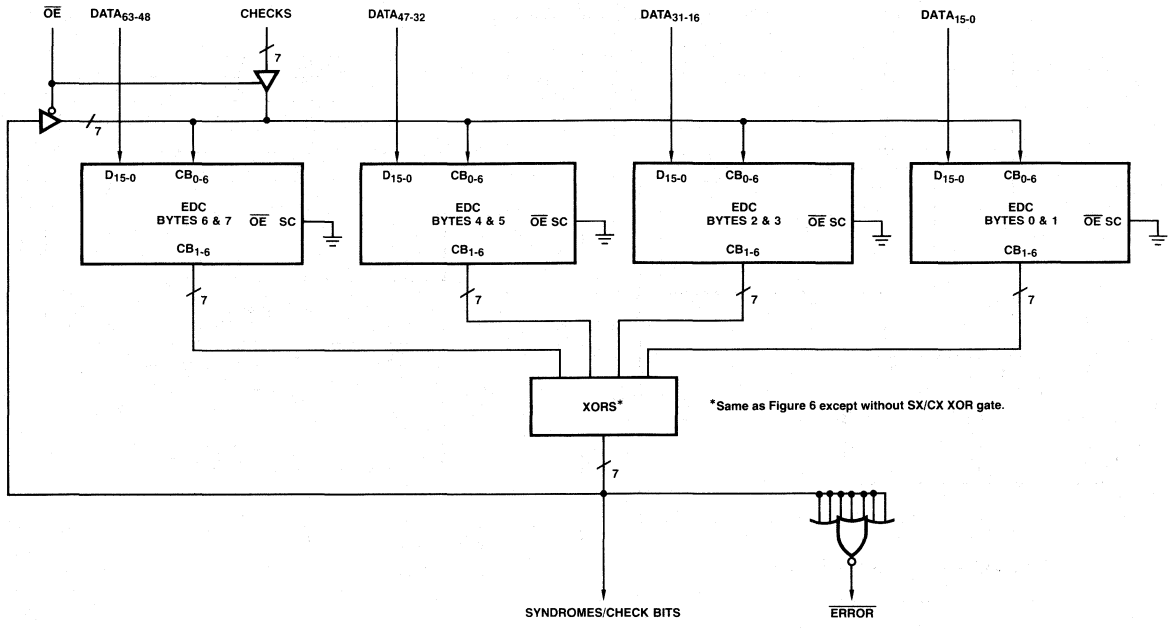
The syndromes generated by the EDC may be decoded to determine whether the single bit error is a check bit.

In many memory systems, a check bit error will be ignored on the memory read and corrected during a periodic "scrubbing" of memory (see section in System Design Considerations).

Multiple Errors

The bit-in-error decode logic uses syndrome bits S0 through S32 to correct errors, SX is only used in developing the multiple error signal. This means that some multiple errors will cause a data bit to be inverted.

For example, in the 16-bit mode if data bits 8 and 13 are in error the syndrome 111100 (SX, S0, S1, S2, S4, S8) is produced. This is flagged a double error by the error detection logic, but the bit-in-error decoder only receives syndrome 11100 (S0, S1, S2, S4, S8) which it decodes as a single error in data bit 0 and inverts that bit. If it is desired to inhibit this inversion, the multiple error output may be connected to the correct input as in Figure 21. This will inhibit correction when a multiple error occurs. Extra time delay may be introduced in the data to correct data path when this is done.



Notes: 1. In Pass Thru Mode the Contents of the Check Latch Appear on the XOR Outputs Inverted.
2. In Diagnostic Generate Mode the Contents of the Diagnostic Latch appear on the XOR Outputs Inverted.

Figure 20. 64-Bit Single Correct Only

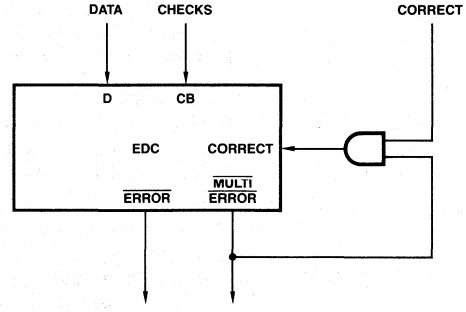


Figure 21. Inhibition of Data Modification

SYSTEM DESIGN CONSIDERATIONS

High Performance Parallel Operation

For maximum memory system performance the EDC should be used in the Check-Only configuration shown in Figure 22. With this configuration the memory system operates as fast with EDC as it would without.

On reads from memory, data is read out from the RAMs directly to the data bus (same as in a non-EDC system). At the same time, the data is read into the EDC to check for errors. If an error exists the EDC's error flags are used to interrupt the CPU and/or to stretch the memory cycle. If no error is detected, no slowdown is required.

If an error is detected, the EDC generates corrected data for the processor. At the designer's option the correct data may be written back into memory; error logging and diagnostic routines may also be run under processor control.

The Check-Only configuration allows data reads to proceed as fast with EDC as without. Only if an error is detected is there any slowdown. But even if the memory system had an error every hour this would mean only one error every 3-4 *billion* memory cycles. So even with a very high error rate, EDC in a Check-Only configuration has essentially zero impact on memory system speed.

On writes to memory, check bits must be generated before the full memory word can be written into memory. But using the Am2961/62 Data Bus Buffers allows the data word to be buffered on the memory board while check bits are generated. This makes the check bit generate time transparent to the processor.

EDC in the Data Path

The simplest configuration for EDC is to have the EDC directly in the data path as shown in Figure 23 (Correct-Always Configuration). In this configuration data read from memory is always corrected prior to putting the data on the data bus. The advantages are simpler operation and no need for mid-cycle interrupts. The disadvantage is that memory system speed is slowed by the amount of time it takes for error correction on ever cycle.

Usually the Correct-Always Configuration will be used with MOS microprocessors which have ample memory timing budgets. Most high performance processors will use the high performance parallel configuration shown in Figure 22. (Check-Only Configuration).

Scrubbing Avoids Double Errors

Single-bit errors are by far the most common in a memory system and are always correctable by the EDC.

Double bit memory errors are far less frequent than single bit (50 to 1, or 100 to 1) and are always detected by the EDC but not corrected.

In a memory system, soft errors occur only one at a time. A double bit error in a data word occurs when a single soft error is left uncorrected and is followed by another error in the data word hours, days, or weeks after the first.

"Scrubbing" memory periodically avoids almost all double-bit errors. In the scrubbing operation, every data word in memory is periodically checked by the EDC for single-bit errors. If one is found, it is corrected and the data word written back into memory. Errors are not allowed to pile up and so most double-bit errors are avoided.

The scrubbing operation is generally done as a background routine when the memory is not being used by the processor.

If memory is scrubbed frequently, errors that are detected and corrected during processor accesses need not be immediately written back into memory. Instead the error will be corrected in memory during scrubbing. This reduces the time delay involved in a processor access of an incorrect memory word.

Correction of Double-Bit Errors

In some cases, double-bit memory errors can be corrected! This is possible when one of the two bit errors is a hard error.

When a double bit error is detected the data word should be checked to determine if one of the errors is a hard error. If so the

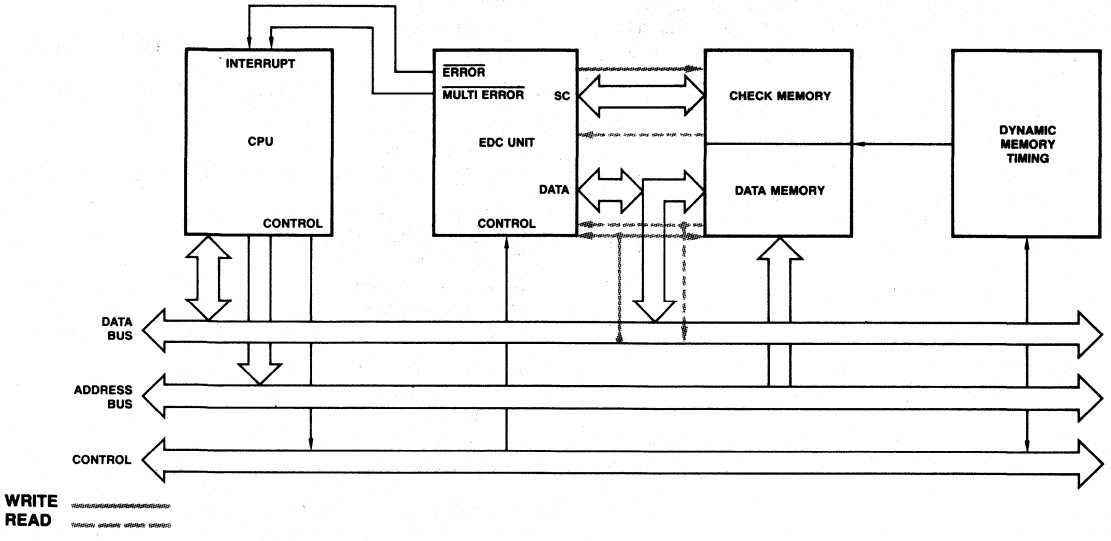


Figure 22. Check-Only Configuration

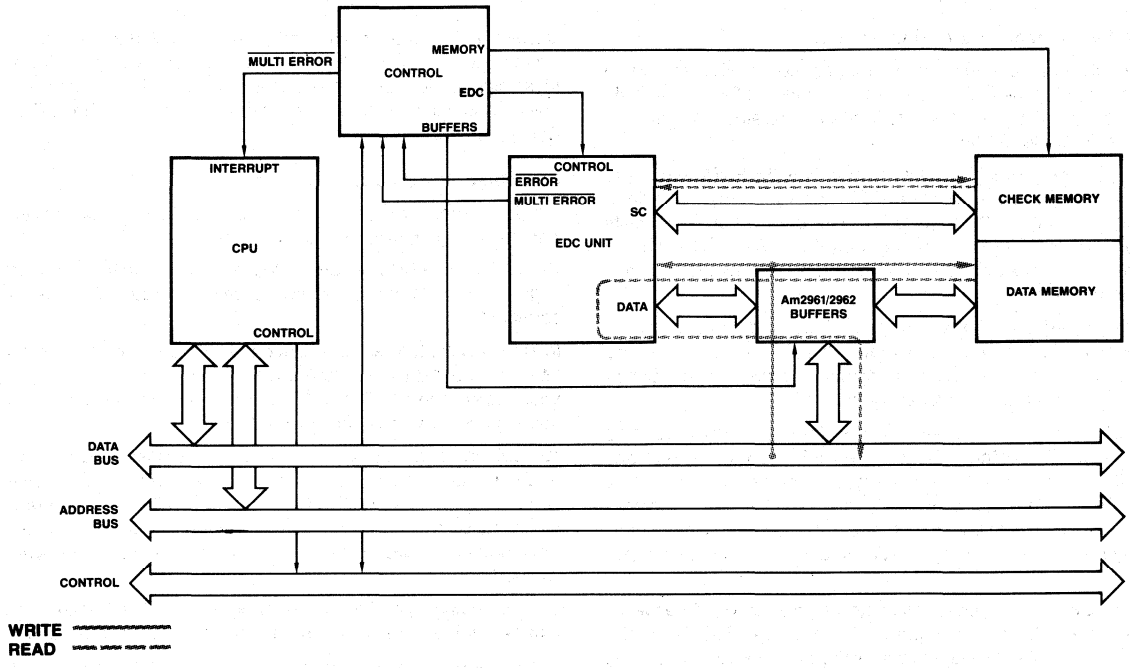


Figure 23. Correct-Always Configuration

hard error bit may be corrected by inverting it leaving only a single, correctable error. The time for this operation is negligible since it will occur infrequently.

The procedure after detection of a double error is as follows:

- Invert the data bits read from memory.
- Write the inverted data back into the same memory word.
- Re-read the memory location and XOR the newly read out value with the old. If there is no hard error then the XOR result will be all 1's. If there is a hard error, it will have the same bit value regardless of what was written in. So it will show as a 0 after the XOR operation
- Invert the hard error bit (this will "correct" it) leaving only one error in the data.
- The EDC can then correct the single bit error.
- Rewrite the correct data word into memory. This does not change the hard error but does eliminate the soft error. So the next memory access will find only a single-bit, correctable error.

An example helps to illustrate the procedure.

Example of Double Bit Error Correction When One is a Hard Error

1) Data Read from Memory (D_1)	1111111100000011 (16 data bits)	011010 (6 check bits)
2) EDC detects a multiple error. Syndromes:		011000
3) Syndrome decode indicates a double bit error.		
4) Invert the bits read from memory (D_1)	0000000011111100	100101
5) Write D_1 back to the same memory location		
6) Read back the memory location (D_2)	0000000011111101	100101
7) XOR D_1 and D_2	1111111111111110	111111
8) So the last data bit is the hard error. Use this to modify D_1	1111111100000010	011010
9) Pass the modified D_1 through the EDC. The EDC detects a single bit correctable error and outputs corrected data:	1111111100000000	011010
10) Write the corrected data back to memory to fix the soft error.		

Error Logging and Preventative Maintenance

The effectiveness of preventative maintenance can be increased by logging information on errors detected by the EDC. This is called error logging.

The EDC provides syndromes when errors are detected. The syndromes indicate which bit is in error. In most memory systems, each individual RAM supplies only one bit of the memory word. So the syndrome and data word address specify which RAM was in error.

Typically a permanent/hard RAM failure is preceded by a period of time where the RAM displays an increasing frequency of intermittent, soft errors. Error logging statistic can be used to detect an increasing intermittent error frequency so that the RAM can be replaced before a permanent failure occurs.

Error logging also records the location of already hard failed RAMs. With EDC a hard failure will not halt system operation. EDC always can correct single bit errors even if it is a hard error. EDC can also correct double bit errors where one is hard and one soft (see "Correction of Double Bit Errors" Section). The ability to continue operation despite hard errors can greatly reduce the need for emergency field maintenance. The hard-failed RAMs can be instead replaced at low cost during a regularly scheduled preventative maintenance session.

Reducing Check Bit Overhead

Memory word widths need not be the same as the data word width of the processor. There is a substantial reduction in check bit overhead if wider memory words are used:

Memory Word		Check Bit Overhead
# Data Bits	# Check Bits	
8	5	38%
16	6	27%
32	7	14%
64	8	11%

This reduction in check bit overhead lowers cost and increases the amount of data that can be packed on to each board.

The trade off is that when writing data pieces into memory that are narrower than the memory word width, more steps are required. These steps are exactly the same as those described in Byte Write in the Applications section. No penalty exists for reads from memory.

EDC Per Board vs EDC Per System

The choice of an EDC per system or per board depends on the economics and the architecture of the system.

Certainly the cheaper approach is to have only one EDC per system and this is a viable solution if only one memory location is accessed at at time.

This solution does require that the system has both data and check bit lines (see Figure 25). This makes retrofitting a system difficult and creates complications if static or ROM memory, which do not require check bits, are mixed in with dynamic RAM.

If the system has an advanced architecture it is quite likely that it is necessary to simultaneously access memory locations on different memory boards (see Figure 24). Architectural features that require this are interleaved memory, cache memory, and DMA that is done simultaneously with processor memory accesses. EDC per board is a simpler system from a design standpoint.

The EDC is designed to work efficiently in either the per system or per board configurations.

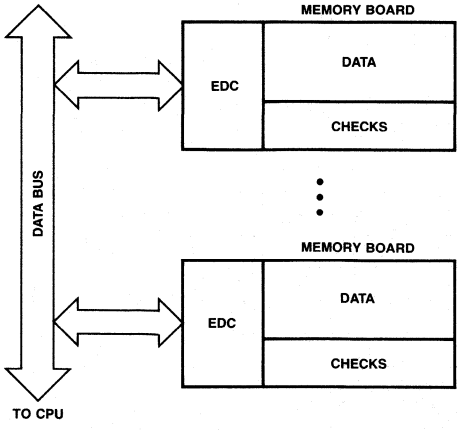


Figure 24. EDC Per Board

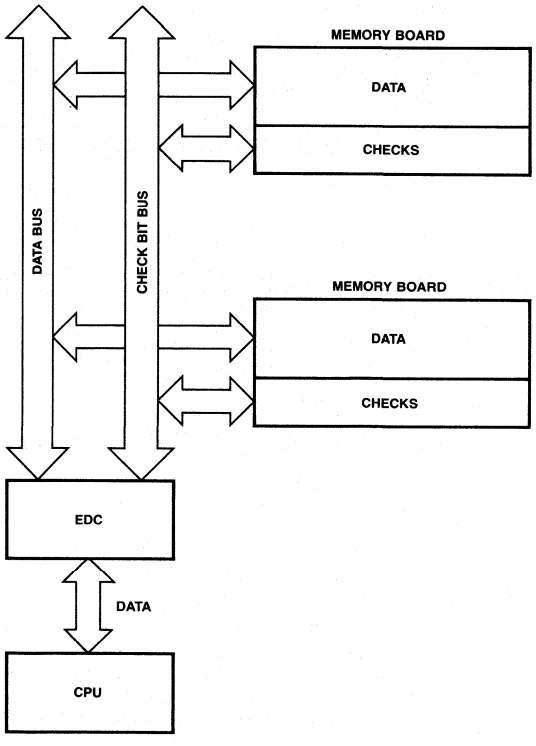


Figure 25. EDC Per System

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the Am2960 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

Definitions

D_i ← ($DATA_i$ if LE IN is HIGH or the output of bit i of the Data Input Latch if LE IN is LOW)
C_i ← (CB_i if LE IN is HIGH or the output of bit i of the Check Bit Latch if LE IN is LOW)
DL_i ← Output of bit i of the Diagnostic Latch
S_i ← Internally generated syndromes (same as outputs of SC_i if outputs enabled)

$$PA \leftarrow D0 \oplus D1 \oplus D2 \oplus D4 \oplus D6 \oplus D8 \oplus D10 \oplus D12$$
$$PB \leftarrow D0 \oplus D1 \oplus D2 \oplus D3 \oplus D4 \oplus D5 \oplus D6 \oplus D7$$
$$PC \leftarrow D8 \oplus D9 \oplus D10 \oplus D11 \oplus D12 \oplus D13 \oplus D14 \oplus D15$$
$$PD \leftarrow D0 \oplus D3 \oplus D4 \oplus D7 \oplus D9 \oplus D10 \oplus D13 \oplus D15$$
$$PE \leftarrow D0 \oplus D1 \oplus D5 \oplus D6 \oplus D7 \oplus D11 \oplus D12 \oplus D13$$
$$PF \leftarrow D2 \oplus D3 \oplus D4 \oplus D5 \oplus D6 \oplus D7 \oplus D14 \oplus D15$$
$$PG_1 \leftarrow D0 \oplus D4 \oplus D6 \oplus D7$$
$$PG_2 \leftarrow D1 \oplus D2 \oplus D3 \oplus D5$$
$$PG_3 \leftarrow D8 \oplus D9 \oplus D11 \oplus D14$$
$$PG_4 \leftarrow D10 \oplus D12 \oplus D13 \oplus D15$$

Error Signals

$$\overline{ERROR} \leftarrow \overline{(S6 \cdot (ID_1 + ID_2))} \cdot \overline{S5} \cdot \overline{S4} \cdot \overline{S3} \cdot \overline{S2} \cdot \overline{S1} \cdot \overline{S0} + GENERATE + INITIALIZE + PASSTHRU$$

$$\overline{MULT\ ERROR}\ (16\text{ and }32\text{-Bit Modes}) \leftarrow \overline{((S6 \cdot ID_1) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)\,(\overline{ERROR})} + TOME + GENERATE + PASSTHRU + INITIALIZE$$

$$\overline{MULT\ ERROR}\ (64\text{-Bit Modes}) \leftarrow TOME + GENERATE + PASSTHRU + INITIALIZE$$

TOME (Three or More Errors)*

S1	S2	S3 \ S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
		**S6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		**S5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0
0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

*S6, S5, . . . S0 are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes the syndromes are input over the Check-Bit lines. S6 ← C6, S5 ← C5, . . . S1 ← C1, S0 ← C0.

**The S6 internal syndrome is always forced to 0 in CODE ID 000.

SC Outputs

Tables XV, XVI, XVII, XVIII, XIX show how outputs SC_{0-6} are generated in each control mode for various CODE IDs (internal control mode not applicable).

TABLE XV.

GENERATE Mode (Check Bits) / CODE ID_{2-0}	000	010	011	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	PA	PA	PA	PA	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD}$	$\overline{PD}$	PD	$\overline{PD}$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE}$	$\overline{PE}$	PE	$\overline{PE}$	PE	PE	PE
$SC_4 \leftarrow$	PF	PF	PF	PF	PF	PF	PF
$SC_5 \leftarrow$	PC	PC	PC	PC	PC	PC	PC
$SC_6 \leftarrow$	1	PB	PC	PB	PB	PB	PB

TABLE XVI.

Detect and Correct Modes (Syndromes) / CODE ID_{2-0}	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus C0$	$PG_1 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus C1$	$PA \oplus C1$	$PA \oplus CB_1$	$PA \oplus C1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus C2$	$\overline{PD} \oplus C2$	$PD \oplus CB_2$	$\overline{PD} \oplus C2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus C3$	$\overline{PE} \oplus C3$	$PE \oplus CB_3$	$\overline{PE} \oplus C3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus C4$	$PF \oplus C4$	$PF \oplus CB_4$	$PF \oplus C4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus C5$	$PC \oplus C5$	$PC \oplus CB_5$	$PC \oplus C5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus C6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C6$	$PB \oplus C6$

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent, the Data Latch operates normally.

TABLE XVII.

Diagnostic Read Mode / CODE ID_{2-0}	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent, the Data Latch operates normally.

TABLE XVIII.

CODE ID_{2-0} / Diagnostic Write Mode	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	DL_0	DL_0	CB_0	DL_0	1	1	1
$SC_1 \leftarrow$	DL_1	DL_1	CB_1	DL_1	1	1	1
$SC_2 \leftarrow$	DL_2	DL_2	CB_2	DL_2	1	1	1
$SC_3 \leftarrow$	DL_3	DL_3	CB_3	DL_3	1	1	1
$SC_4 \leftarrow$	DL_4	DL_4	CB_4	DL_4	1	1	1
$SC_5 \leftarrow$	DL_5	DL_5	CB_5	DL_5	1	1	1
$SC_6 \leftarrow$	1	DL_6	CB_6	1	1	DL_6	DL_7

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Input Latch operates normally.

TABLE XIX.

CODE ID_{2-0} / PASS THRU Mode	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	C0	C0	CB_0	C0	1	1	1
$SC_1 \leftarrow$	C1	C1	CB_1	C1	1	1	1
$SC_2 \leftarrow$	C2	C2	CB_2	C2	1	1	1
$SC_3 \leftarrow$	C3	C3	CB_3	C_3	1	1	1
$SC_4 \leftarrow$	C4	C4	CB_4	C4	1	1	1
$SC_5 \leftarrow$	C5	C5	CB_5	C5	1	1	1
$SC_6 \leftarrow$	1	C6	CB_6	1	1	C6	C6

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Input Latch operates normally.

Data Correction

Tables XX to XXVI shows which data output bits are corrected (inverted) depending upon the syndromes and the CODE ID position. Note that the syndromes that determine data correction are in some cases syndromes input externally via the CB inputs and in some cases syndromes generated internally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

The tables show the number of data bit inverted (corrected) if any for the CODE ID and syndrome combination.

TABLE XX. CODE ID_{2-0} = 000*

	S5	0	0	0	0	1	1	1	1
	S4	0	0	1	1	0	0	1	1
	S3	0	1	0	1	0	1	0	1
S2	S1								
0	0	–	–	–	5	–	11	14	–
0	1	–	1	2	6	8	12	–	–
1	0	–	–	3	7	9	13	15	–
1	1	–	0	4	–	10	–	–	–

*Unlisted S combinations are no correction.

TABLE XXI. CODE ID_{2-0} = 010*

	CB_6	0	0	0	0	1	1	1	1
	CB_5	1	1	1	1	0	0	0	0
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2	CB_1								
0	0	–	11	14	–	–	–	–	5
0	1	8	12	–	–	–	1	2	6
1	0	9	13	15	–	–	–	3	7
1	1	10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction.

TABLE XXII. CODE ID_{2-0} = 011*

S6	0	0	0	0	1	1	1	1
S5	0	0	0	0	1	1	1	1
S4	0	0	1	1	0	0	1	1
S3	0	1	0	1	0	1	0	1
S2 S1								
0 0	–	–	–	5	–	11	14	–
0 1	–	1	2	6	8	12	–	–
1 0	–	–	3	7	9	13	15	–
1 1	–	0	4	–	10	–	–	–

*Unlisted S combinations are no correction.

TABLE XXIII. CODE ID_{2-0} = 100*

CB_0	0	0	0	0	1	1	1	1
CB_6	0	0	0	0	1	1	1	1
CB_5	1	1	1	1	0	0	0	0
CB_4	0	0	1	1	0	0	1	1
CB_3	0	1	0	1	0	1	0	1
CB_2 CB_1								
0 0	–	11	14	–	–	–	–	5
0 1	8	12	–	–	–	1	2	6
1 0	9	13	15	–	–	–	3	7
1 1	10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction

TABLE XXIV. CODE ID_{2-0} = 101*

CB_0	0	0	0	0	1	1	1	1
CB_6	0	0	0	0	1	1	1	1
CB_5	0	0	0	0	1	1	1	1
CB_4	0	0	1	1	0	0	1	1
CB_3	0	1	0	1	0	1	0	1
CB_2 CB_1								
0 0	–	–	–	5	–	11	14	–
0 1	–	1	2	6	8	12	–	–
1 0	–	–	3	7	9	13	15	–
1 1	–	0	4	–	10	–	–	–

*Unlisted CB combinations are no correction.

TABLE XXV. CODE ID_{2-0} = 110*

CB_0	0	0	0	0	1	1	1	1
CB_6	1	1	1	1	0	0	0	0
CB_5	0	0	0	0	1	1	1	1
CB_4	0	0	1	1	0	0	1	1
CB_3	0	1	0	1	0	1	0	1
CB_2 CB_1								
0 0	–	–	–	5	–	11	14	–
0 1	–	1	2	6	8	12	–	–
1 0	–	–	3	7	9	13	15	–
1 1	–	0	4	–	10	–	–	–

*Unlisted CB combinations are no correction.

TABLE XXVI. CODE ID_{2-0} = 111*

CB_0	0	0	0	0	1	1	1	1
CB_6	1	1	1	1	0	0	0	0
CB_5	1	1	1	1	0	0	0	0
CB_4	0	0	1	1	0	0	1	1
CB_3	0	1	0	1	0	1	0	1
CB_2 CB_1								
0 0	–	11	14	–	–	–	–	5
0 1	8	12	–	–	–	1	2	6
1 0	9	13	15	–	–	–	3	7
1 1	10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction.

7

ADVANCED MICRO DEVICES

TECHNICAL REPORT

Am2960 BOOSTS MEMORY RELIABILITY

ABSTRACT

Memory error frequency will increase due to the use of larger memory systems and the use of 16K and 64K RAMs, which are more susceptible to soft errors because of their smaller memory cell geometry.

At the same time, the need for reliability is increasing, both for the user and the system manufacturer. EDC (Error Detection and Correction) can reduce system downtime, can reduce field maintenance expenses and can provide manufacturers a marketing advantage due to increased reliability.

The Am2960 implements EDC using a modified Hamming code, and so boosts memory reliability by a factor of 60 or better. It slashes package count and adds initialization, byte-write and diagnostic features. It is fast and flexible enough to handle word widths from 8 to 64 bits.

The Am2960 is one of a series of Memory Support devices designed for use with dynamic MOS RAM memory systems.

Prepared by: Advanced Micro Devices, Bipolar Microprocessor.

Am2960 BOOSTS MEMORY RELIABILITY

The Am2960 is a 16-bit, expandable Error Detection and Correction (EDC) unit. It is used in conjunction with system main memories to boost memory reliability.

The Am2960 can correct *all* single-bit memory errors in a data word. It detects all double-bit errors and even some triple-bit errors. The gross error conditions of all 0s or all 1s are always detected.

Memory error and detection using the Am2960 boosts system reliability by a factor of 60 or better. System crashes will occur far less frequently and maintenance costs can be slashed.

MEMORY ERRORS

Memory Error Frequency

Memory errors are becoming *more* frequent due to two general trends:

1. Total system memory size is growing, and,
2. The geometry of individual memory cells in dynamic RAMs is shrinking, making them more susceptible to "soft" errors.

There are two basic types of memory errors. Hard errors are permanent physical failures of either the whole RAM, a row, a column, or a single bit. Hard errors are caused by power shorts, open leads, and various other factors. Initial testing and burn-in will reduce but not eliminate hard error failures in RAMs during system operation.

Soft errors are non-repeating, single-bit errors where there is no permanent damage. A soft error occurs when the charge state of a bit incorrectly shifts from 0 to 1 or from 1 to 0. This can be caused by system noise, pattern sensitivity, power surges[6] or alpha particles. The new 16K and 64K dynamic RAMs, with their smaller memory cell geometries are especially susceptible to soft errors induced by alpha particles. (The smaller the memory cell geometry, the less energy is required to cause the cell to change state.)

A paper given at Wescon, 1979[1] presented these failure rates for dynamic RAMs of increasing size (see Table 1). This table reflects only soft errors due to alpha particles.

Undetected Memory Failures are Expensive

Memory failures will occur in a system. When they do they will result either in a system crash or in loss of data integrity, unless memory error detection schemes are used. Either situation is expensive and inconvenient for the system users. Either situation can result in maintenance calls to the system manufacturer.

If the memory error occurs in an instruction word and the instruction is executed without being corrected, then a system crash will almost certainly occur. For example, an "Add" instruction could be changed to a "Jump" instruction with only a one-bit change – if the error is undetected, the jump would take place to essentially a random location.

If the error occurs in a word that is used for storing data, then data integrity is lost. In typical applications this could mean that bank account balances would be altered, blood diagnosis would be incorrect, or cooling water valves could be closed instead of opened.

System failures of any kind will often result in unscheduled maintenance requests to the system manufacturers. Maintenance calls are expensive for the system manufacturer and are to be avoided by preventative means if at all possible.

Strategies for Memory Errors

For reliability and maintenance cost reduction, memory errors must be dealt with by the system designer.

A common scheme is to use parity. But parity schemes cannot correct errors and can detect only single-bit errors. If a double-bit error occurs in a word, the parity is unchanged and so the error goes undetected. Parity cannot correct errors.

Error detection and correction (EDC) is implemented by the Am2960 using a modified Hamming code. The Hamming code scheme involves generating several check bits that contain enough redundant information to correct *all* single-bit errors and to detect all double-bit errors and some triple-bit errors. Also, the EDC modified Hamming code detects the gross error conditions of all 0s and all 1s.

Table 2 demonstrates that EDC is the superior strategy for both the system user and the system manufacturer.

TABLE 1. ERRORS ARE INCREASING.

Density Bits/Chip	Typical Error Rate (% per 1,000 Hours)	
	Soft*	Hard**
1K	.001	.0001
4K	.02	.002
16K	.10	.011
64K	.5***	.016

*Reflects alpha particles only. Does not include errors due to noise, power, patterns.
**After infant mortality.
***Based on initial customer evaluation.
Note: 0.1% per 1000 hours equals 1 failure in 10^6 hours.

TABLE 2. COMPARISON OF ERROR STRATEGIES.

Error Type	No Checking	Parity	EDC Using Am2960
Single-Bit Error	System crash.	System halt.	Correctable. System runs.
Double-Bit Error	System crash.	System crash.	System halt.
Entire RAM Failure	System crash.	System halt.	Correctable. System runs.

With EDC, the incidence of maintenance calls is significantly reduced. Even the failure of an entire RAM chip will not necessarily result in a system failure. Double-bit errors are not corrected but are detected so that the system may be halted and the user informed of a memory error and the exact location of it. A controlled system halt is far more desirable than an uncontrolled system crash.

EDC Improves MTTF

Error detection and correction as implemented on the Am2960 significantly improves the MTTF (mean time to failure) of memory systems.

A paper presented at Wescon, 1979[1] used the dynamic RAM error rates shown previously to calculate the following MTTFs for a 16 Megabyte system using 64K RAMs (see Table 3).

TABLE 3.

Error Type	MTTF*
Correctable Soft Error (Single-Bit)	13 days
Correctable Hard Error (Single-Bit)	110 days
Non-Correctable Soft Error (Double-Bit)	864 days
Non-Correctable Hard Error (Double-Bit)	7,021 days

*Based on 64K RAM alpha error rate of 0.13% per 1000 hours.

The MTTF improves by a factor of at least 60 with EDC. This improvement factor has been noted by others[2].

Another paper [3,4] calculated that with EDC, RAM errors would become a small factor in memory based failures relative to failures of other board components such as MSI, capacitors and resistors. The same paper[4] discusses how frequently preventative maintenance should be done so that a hard-failed RAM is replaced prior to a second RAM experiencing a hard-failure. The Am2960 has features that allow easy logging of data errors – this aids the maintenance engineer in quickly pinpointing hard-failed RAMs and RAMs displaying excessive soft error rates.

Memory Reliability is a Competitive Edge

EDC boosts memory reliability and gives you two competitive advantages:

1. Your system is more reliable.
2. Your field maintenance costs are reduced.

The demand for reliable system performance is increasing steadily. Reliability is a must for applications in aerospace, medical, banking, process control and on-line systems. Applications such as word-processors, small business systems and telecommunications also need memory reliability, as their users do not have the technical staff to handle system failures and are willing to pay for the convenience of smooth, error-free operation.

REFERENCES

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6. "Power-Line Disturbances Scorecard," Electronic Design, February 15, 1979.
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8. "Analyzing Computer Technology Costs," Computer Design, October, 1978.
9. "Alphas Cause Rift at ECC," Electronic Engineering Times, May 28, 1979.
10. Ernst L. Wall, ITT, "Applying the Hamming Code to Microprocessor-Based Systems," Electronics, November 22, 1979.

These devices are also characterized as:
AmZ8161
AmZ8162

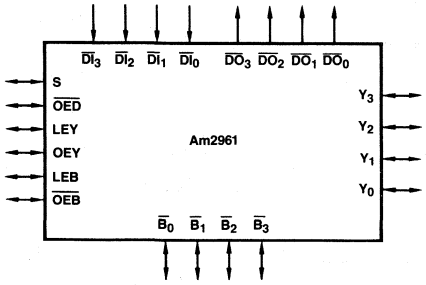
Am2961 • Am2962

4-Bit Error Correction Multiple Bus Buffers

DISTINCTIVE CHARACTERISTICS

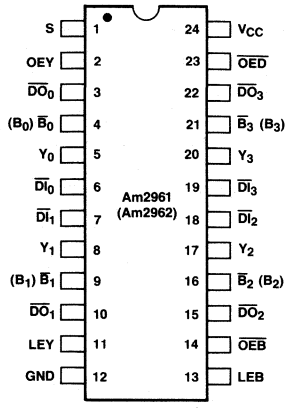
- Quad high-speed LSI bus-transceiver
- Provides complete data path interface between the Am2960 Error Detection and Correction Unit, the system data bus and dynamic RAM memory
- Three-state 24mA output to data bus
- Three-state data output to memory
- Inverting data bus for Am2961 and noninverting for Am2962
- Data bus latches allow operation with multiplexed buses
- Space saving 24-pin 0.3" package
- 100% MIL-STD-883 reliability assurance testing

LOGIC SYMBOL



B-Bus is noninverting for Am2962.

CONNECTION DIAGRAM
Top View



24 pin slim (0.3")

Note: Pin 1 is marked for orientation.

BLI-122

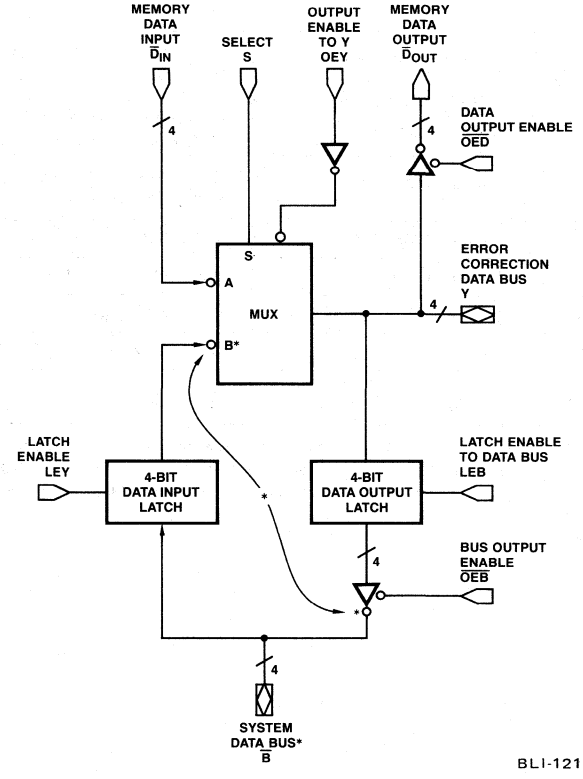
FUNCTIONAL DESCRIPTION

The Am2961 and Am2962 are high-performance, low-power Schottky multiple bus buffers that provide the complete data path interface between the Am2960 Error Detection and Correction Unit, dynamic RAM memory and the system data bus. The Am2961 provides an inverting data path between the data bus (B_i) and the Am2960 error correction data input (Y_i) and the Am2962 provides a noninverting configuration (B_i to Y_i). Both devices provide inverting data paths between the Am2960 and memory data bus thereby optimizing internal data path speeds.

The Am2961 and Am2962 are 4-bit devices. Four devices are used to interface each 16-bit Am2960 Error Detection and Correction Unit with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction.

Data latches between the error correction data bus and the system data bus facilitate byte writing in memory systems wider than 8-bits. They also provide a data holding capability during single-step system operation.

LOGIC DIAGRAM



BLI-121

*Am2962 is the same function but noninverting to the system data bus, B.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (MIN = 4.75V MAX = 5.25V)

MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE – Y BUS

Parameters	Description	Test Conditions (Note 1)			Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA			0.3	0.45	Volts
			I_{OL} = 16mA			0.35	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		OEY = LOW			−2.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		OEY = LOW			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		OEY = LOW			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−130	mA

DC CHARACTERISTICS OVER OPERATING RANGE – B BUS

Parameters	Description	Test Conditions (Note 1)			Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA		2.4			Volts
			I_{OH} = −15mA		2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA			0.3	0.45	Volts
			I_{OL} = 24mA			0.35	0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		$\overline{OEB}$ = HIGH			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		$\overline{OEB}$ = HIGH			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		$\overline{OEB}$ = HIGH			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−50		−150	mA

Notes: 1. For conditions as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

DC CHARACTERISTICS OVER OPERATING RANGE – DO OUTPUTS

Parameters	Description	Test Conditions (Note 1)		Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL I_{OH} = −50μA	2.5			Volts
			COM'L I_{OH} = −100μA	2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.4	Volts
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−50		−150	mA
I_O	Off-State Out Current	V_{CC} = MAX	V_O = 0.4V			−100	μA
			V_O = 2.4V			+100	

DC CHARACTERISTICS OVER OPERATING RANGE – DI INPUTS AND CONTROLS

Parameters	Description	Test Conditions (Note 1)		Min	Typ. (Note 2)	Max	Units
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_C	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	DI Inputs			−1.0	mA
			Controls			−1.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA

DC CHARACTERISTICS OVER OPERATING RANGE – POWER SUPPLY

Parameters	Description	Test Conditions (Note 1)	Min	Typ. (Note 2)	Max	Units
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX		110	155	mA

Note 4:

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} MAX
DC Input Voltage	5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

Am2961
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Min	COM'L Max	MIL T = −55 to +125°C, V_{CC} = 5.0V ±10% Min	MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay $\overline{B}$ to Y (Latch Transparent, OEY = LEY = HIGH)		25		28	ns	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ
t_{PHL}			25		28	ns	
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)		15		18	ns	
t_{PHL}			15		18	ns	
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)		25		28	ns	
t_{PHL}			25		28	ns	
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)		25		30	ns	
t_{PHL}			35		40	ns	
t_{PZH}	Y Bus Output Enable Time OEY to Y		18		21	ns	
t_{PZL}			18		21	ns	
t_{PHZ}	Y Bus Output Disable Time OEY to Y		18		21	ns	
t_{PLZ}			18		21	ns	
t_{PLH}	Propagation Delay LEB to $\overline{B}$ ($\overline{OEB}$ = LOW)		25		30	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			35		40	ns	
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		18		21	ns	
t_{PHL}			20		23	ns	
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		26		30	ns	Figure 1, C_L = 300pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			31		35	ns	
t_{PZH}	$\overline{B}$ Bus Output Enable Time $\overline{OEB}$ to $\overline{B}$		18		21	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PZL}			18		21	ns	
t_{PLZ}	$\overline{B}$ Bus Output Disable Time $\overline{OEB}$ to $\overline{B}$		18		21	ns	
t_{PHZ}			18		21	ns	
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)		15		18	ns	Figure 2, C_L = 50pF, R = 2kΩ
t_{PHL}			20		23	ns	
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$		28		30	ns	S = 2; Figure 3, C_L = 50pF, R = 680Ω
t_{PZL}			28		30	ns	S = 1
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$		16		18	ns	S = 2
t_{PLZ}			24		28	ns	S = 1
t_S	$\overline{B}$ to LEY Set-up Time ($\overline{OEB}$ = HIGH)	6		6		ns	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ
t_H	$\overline{B}$ to LEY Hold Time ($\overline{OEB}$ = HIGH)	9		10		ns	
t_S	Y to LEB Set-up Time (OEY = LOW)	6		6		ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_H	Y to LEB Hold Time (OEY = LOW)	9		10		ns	

*AC perfomance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

SWITCHING TEST CIRCUITS

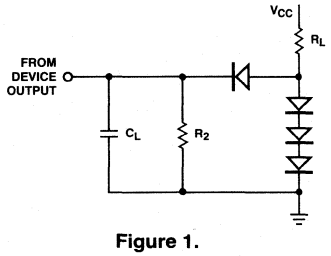


Figure 1.

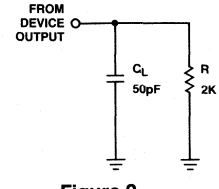


Figure 2.

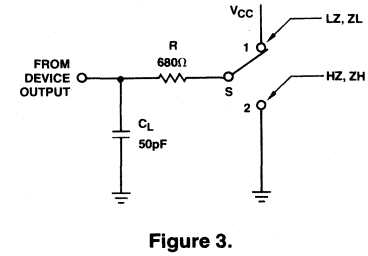


Figure 3.

Am2962
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Min	COM'L Max	MIL T = −55 to +125°C, V_{CC} = 5.0V ±10% Min	MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay B to Y (Latch Transparent, OEY = LEY = HIGH)		27		28	ns	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ
t_{PHL}			27		28	ns	
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)		15		18	ns	
t_{PHL}			15		18	ns	
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)		25		28	ns	
t_{PHL}			25		28	ns	
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)		25		30	ns	
t_{PHL}			35		40	ns	
t_{PZH}	Y Bus Output Enable Time OEY to Y		18		21	ns	
t_{PZL}			18		21	ns	
t_{PHZ}	Y Bus Output Disable Time OEY to Y		18		21	ns	
t_{PLZ}			18		21	ns	
t_{PLH}	Propagation Delay LEB to B ($\overline{OEB}$ = LOW)		25		30	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			35		40	ns	
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		20		23	ns	
t_{PHL}			21		24	ns	
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		28		32	ns	Figure 1, C_L = 300pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			32		36	ns	
t_{PZH}	B Bus Output Enable Time $\overline{OEB}$ to B		18		21	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PZL}			18		21	ns	
t_{PLZ}	B Bus Output Disable Time $\overline{OEB}$ to B		18		21	ns	
t_{PHZ}			18		21	ns	
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)		15		18	ns	Figure 2, C_L = 50pF, R = 2kΩ
t_{PHL}			20		23	ns	
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$		28		30	ns	S = 2
t_{PZL}			28		30	ns	S = 1
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$		16		18	ns	S = 2
t_{PLZ}			24		28	ns	S = 1
							Figure 3, C_L = 50pF, R = 680Ω
t_S	B to LEY Set-up Time ($\overline{OEB}$ = HIGH)	8		8		ns	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ
t_H	B to LEY Hold Time ($\overline{OEB}$ = HIGH)	8		9		ns	
t_S	Y to LEB Set-up Time (OEY = LOW)	8		8		ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_H	Y to LEB Hold Time (OEY = LOW)	8		9		ns	

*AC perfomance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

7

DEFINITION OF FUNCTIONAL TERMS

B_0, B_1 B_2, B_3 The four bidirectional system data bus inputs/outputs. The B-to-Y path is inverting for the Am2961 ($\overline{B}_i$) and noninverting for the Am2962 (B_i).

$\overline{OEB}$ The three-state Output Enable for the system data bus output drivers. When $\overline{OEB}$ is LOW data from the Data Output Latch is output to the system data bus. When $\overline{OEB}$ is HIGH the bus drivers are in the high-impedance state and the Data Input Latch can receive input data from the system data bus.

LEB Latch Enable for the Data Output Latch. When LEB is HIGH the latch is transparent and Y-Bus data is output to the B-Bus. When LEB goes LOW, Y-Bus data meeting the latch set-up and hold time requirements is latched for output to the B-Bus.

Y_0, Y_1, Y_2, Y_3 The four bidirectional EDC data inputs/outputs for connection to the EDC data I/O port.

LEY The Latch Enable control for the Data Input Latch for the data input from the system data bus (B). When LEY is HIGH the latch is transparent and B input data is available at the MUX input for selection to the Y outputs. When LEY goes LOW, B input data meeting the latch set-up and hold time requirements is latched for subsequent selection to the Y outputs.

OEY Output Enable for the Y (EDC) Bus outputs. When OEY is HIGH data selected by the input data multiplexer is output to the Y-bus. When OEY is LOW the MUX output is in the high-impedance state and the Y-Bus can receive input data from the EDC Unit.

S The Select input for the input data multiplexer. A LOW input selects data from the memory data input, $\overline{DI}$, for output to the EDC bus (Y). A HIGH input selects data from the system data bus Data Input Latch (B or $\overline{B}$).

$\overline{DO}_0$, $\overline{DO}_1$, $\overline{DO}_2$, $\overline{DO}_3$ The Data Outputs to the memory data inputs. The $\overline{DO}$ outputs are inverted with respect to the EDC Bus (Y). These outputs are "RAM Driver" outputs with a collector resistor in the lower output driver to protect against undershoot on the HIGH-to-LOW transition.

$\overline{OED}$ Output Enable for the $\overline{DO}$ outputs. An active LOW input causes the $\overline{DO}$ outputs to output inverted data from the EDC (Y) Bus and a HIGH input puts the $\overline{DO}$ outputs in the high-impedance state.

$\overline{DI}_0$, $\overline{DI}_1$, $\overline{DI}_2$, $\overline{DI}_3$ The Data Inputs from memory. $\overline{DI}$ inputs are selected by the data input MUX for output to the EDC (Y) Bus (controlled by S and OEY) and/or output to the system data bus (B) (controlled by LEB and $\overline{OEB}$).

FUNCTION TABLES

Y-BUS OUTPUT

LEY	$\overline{DI_i}$	$\overline{B_i}$* Am2961	B_i* Am2962	S	OEY	Y
X	X	X	X	X	L	Z
X	L	X	X	L	H	H
X	H	X	X	L	H	L
H	X	L	H	H	H	H
H	X	H	L	H	H	L
L	X	X	X	H	H	NC

*$\overline{OEB}$ = HIGH for B data input

B-BUS OUTPUT

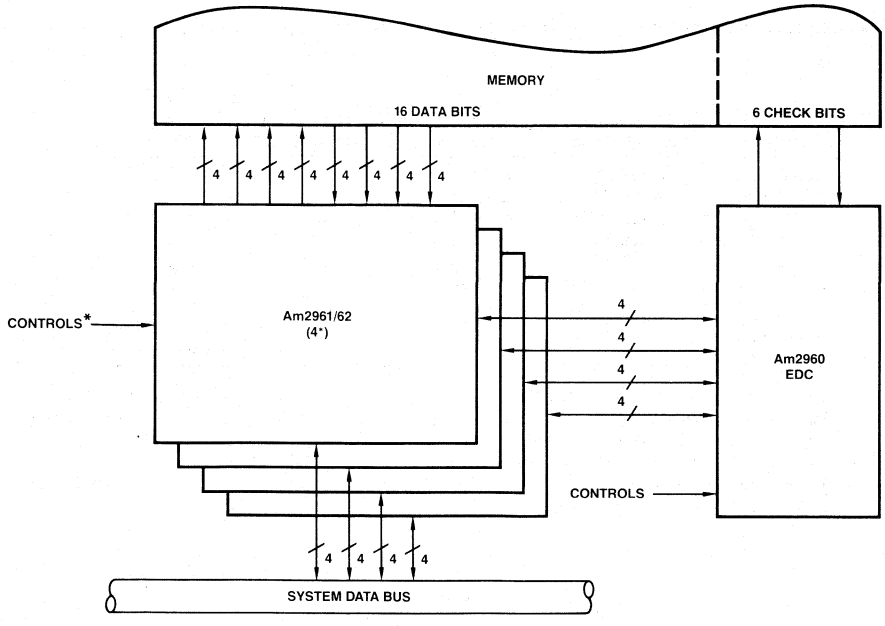
Y* Input	LEB	$\overline{OEB}$	$\overline{B}$ Am2961	B Am2962
X	X	H	Z	Z
L	H	L	H	L
H	H	L	L	H
X	L	L	NC	NC

*OEY = LOW for B data input

$\overline{DO}$ PORT OUTPUT

Y	$\overline{OED}$	$\overline{DO}$
X	H	Z
L	L	H
H	L	L

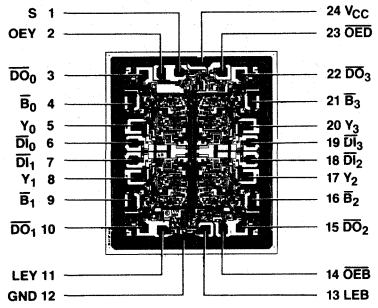
APPLICATION



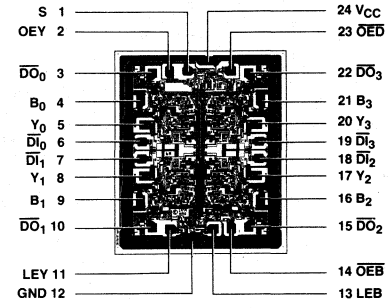
*Since the EDC Data Bus Buffers are four-bit wide devices, controls can be paired to device inputs to provide byte level controls (for any data width).

METALLIZATION AND PAD LAYOUTS

Am2961



Am2962



DIE SIZES .102" X .087"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2961 Order Number	Am2962 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2961DC	AM2962DC	D-24-SLIM	C	C-1
AM2961DC-B	AM2962DC-B	D-24-SLIM	C	B-2 (Note 4)
AM2961DM	AM2962DM	D-24-SLIM	M	C-3
AM2961DM-B	AM2962DM-B	D-24-SLIM	M	B-3
AM2961FM	AM2962FM	F-24	M	C-3
AM2961FM-B	AM2962FM-B	F-24	M	B-3
AM2961XC	AM2962XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B
AM2961XM	AM2962XM	Dice	M	

Notes: 1. D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

This device is also characterized as:
AmZ8164B

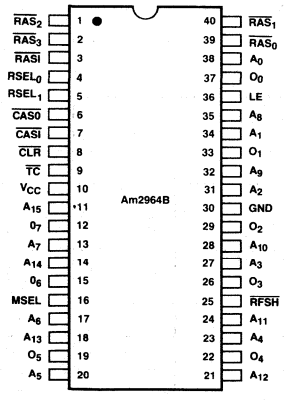
Am2964B
Dynamic Memory Controller

DISTINCTIVE CHARACTERISTICS

- Dynamic Memory Controller for 16K and 64K MOS dynamic RAMs
- 8-Bit Refresh Counter for refresh address generation, has clear input and terminal count output
- Refresh Counter terminal count selectable at 256 or 128
- Latch input $\overline{RAS}$ Decoder provides 4 $\overline{RAS}$ outputs, all active during refresh
- Dual 8-Bit Address Latches plus separate $\overline{RAS}$ Decoder Latches
- Grouping functions on a common chip minimizes speed differential or skew between address, $\overline{RAS}$ and $\overline{CAS}$ outputs
- 3-Port, 8-Bit Address Multiplexer with Schottky speed
- Burst mode, distributed refresh or transparent refresh mode determined by user
- Non-inverting address, $\overline{RAS}$ and $\overline{CAS}$ paths
- 100% MIL-STD-883 reliability assurance testing

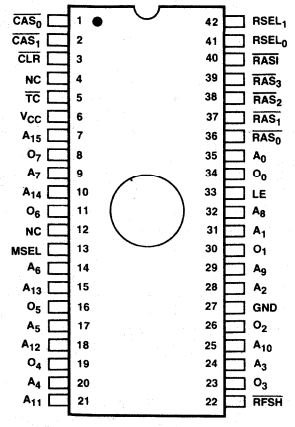
CONNECTION DIAGRAMS
Top Views

DIP



BLI-124

Flatpack



Note: Pin 1 is marked for orientation.

FUNCTIONAL DESCRIPTION

The Am2964B Dynamic Memory Controller (DMC) replaces a dozen MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX, for output to the dynamic RAM address lines.

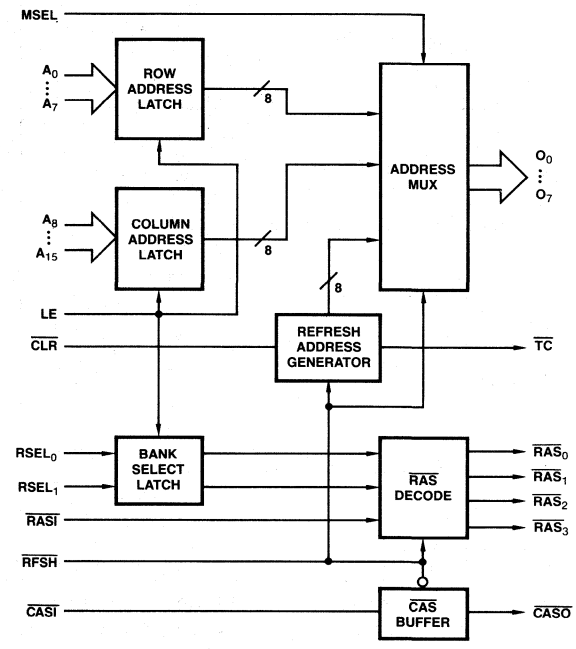
The same silicon chip also includes a special $\overline{RAS}$ decoder and $\overline{CAS}$ buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore, allows a faster memory cycle time by the amount of skew eliminated.

The $\overline{RAS}$ Decoder allows upper addresses to select one-of-four banks of RAM by determining which bank receives a $\overline{RAS}$ input. During refresh ($\overline{RFSH}$ = LOW) the decoder mode is changed to four-of-four and all banks of memory receive a $\overline{RAS}$ input for refresh in response to a $\overline{RASI}$ active LOW input. $\overline{CAS}$ is inhibited during refresh.

Burst mode refresh is accomplished by holding $\overline{RFSH}$ LOW and toggling $\overline{RASI}$.

A_{15} is a dual function input which controls the refresh counter's range. For 64K RAMs it is an address input. For 16K RAMs it can be pulled to +12V through 1KΩ to terminate the refresh count at 128 instead of 256.

LOGIC DIAGRAM



BLI-123

7

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	+0.5V to +V_{CC} MAX
DC Input Voltage	−0.5 to 5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

(Group A, Subgroups 1, 2 and 3)

Am2964XC T_A = 0 to + 70°C — V_{CC} + 5.0V ± 5% (Com'l) — MIN + 4.75V MAX = 5.25V

Am2964XM T_C = −55 to +125°C — V_{CC} = 5.0V ± 10% (MIL) — MIN = 4.50V MAX = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min	TYP (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −1mA	$\overline{TC}$	2.5			Volts
			Others	3.0			Volts
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −15mA	All outputs except $\overline{TC}$	2.0			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	All outputs except $\overline{TC}$, I_{OL} = 16mA			0.5	Volts
			$\overline{TC}$, I_{OL} = 8mA			0.5	Volts
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{RASI}$			−3.2	mA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			−1.6	mA
			A_0 − A_{15}, $\overline{CLR}$, $RSEL_{0,1}$, LE			−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{RASI}$			100	μA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			50	μA
			A_0-A_{15}, $\overline{CLR}$, $RSEL_{0,1}$, LE			20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} − 5.5V	$\overline{RASI}$			2.0	mA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			1.0	mA
		V_{CC} = MAX, V_{IN} = 7.0V	A_0-A_{15}, $\overline{CLR}$, $RSEL_{0,1}$, LE			0.1	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX (Note 3)		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	25°C, 5V			122		mA
		0 to 70°C	COM'L			173	mA
		70°C				165	mA
		−55 to +125°C	MIL			165	mA
		+125°C				150	mA
I_T	A_{15} Enable Current	A_{15} connected to +12V through 1KΩ ± 10%				5	mA

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is worst case when the Address inputs are latched HIGH, the refresh counter is at terminal count (255), $\overline{RASI}$ and $\overline{CASI}$ are HIGH and all other inputs are LOW.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR C_L = 50pF

(Notes 5, 6)

Parameter		Description	T_A = +25°C, V_{CC} = 5.0V	COM'L: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		MIL: T_C = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
			Typ.	Min.	Max.	Min.	Max.		
1	t_{PD}	A_i to O_i Delay	14		19		23	ns	C_L = 50pF
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)	14		20		23	ns	
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)	14		20		23	ns	
4	t_{PD}	MSEL to O_i	17	9		9		ns	
5	t_{PD}	MSEL to O_i	17		21		25	ns	
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)	12		17		19	ns	
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)	15		20		24	ns	
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)	30		40		50	ns	
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)	25		35		40	ns	
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)	10	50		50		ns	
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)	10	50		50		ns	
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)	17		21		25	ns	
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)	19		26		29	ns	
14	t_{PW}	$\overline{CLR}$ = L	10	30		35		ns	
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)	16		21		25	ns	
16	t_{PD}	LE to O_i	25		35		40	ns	
17	t_{PHL}	LE to $\overline{RAS_i}$	30		40		45	ns	
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$	35		45		56	ns	
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)	31		44		54	ns	
20	t_S	A_i to LE Set-up Time	0	5		5		ns	
21	t_H	A_i to LE Hold Time	5	12		15		ns	
22	t_S	$RSEL_i$ to LE Set-up Time	0	5		5		ns	
23	t_H	$RSEL_i$ to LE Hold Time	10	17		25		ns	
24	t_S	$\overline{CLR}$ Recovery Time	5	12		15		ns	
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)	2		5		6	ns	
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)	4		6		8	ns	
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)	6		8		10	ns	
28	t_{SKEW}	O_i to $\overline{RAS_i}$ (MSEL = ↿, Note 10)	1		5		5	ns	

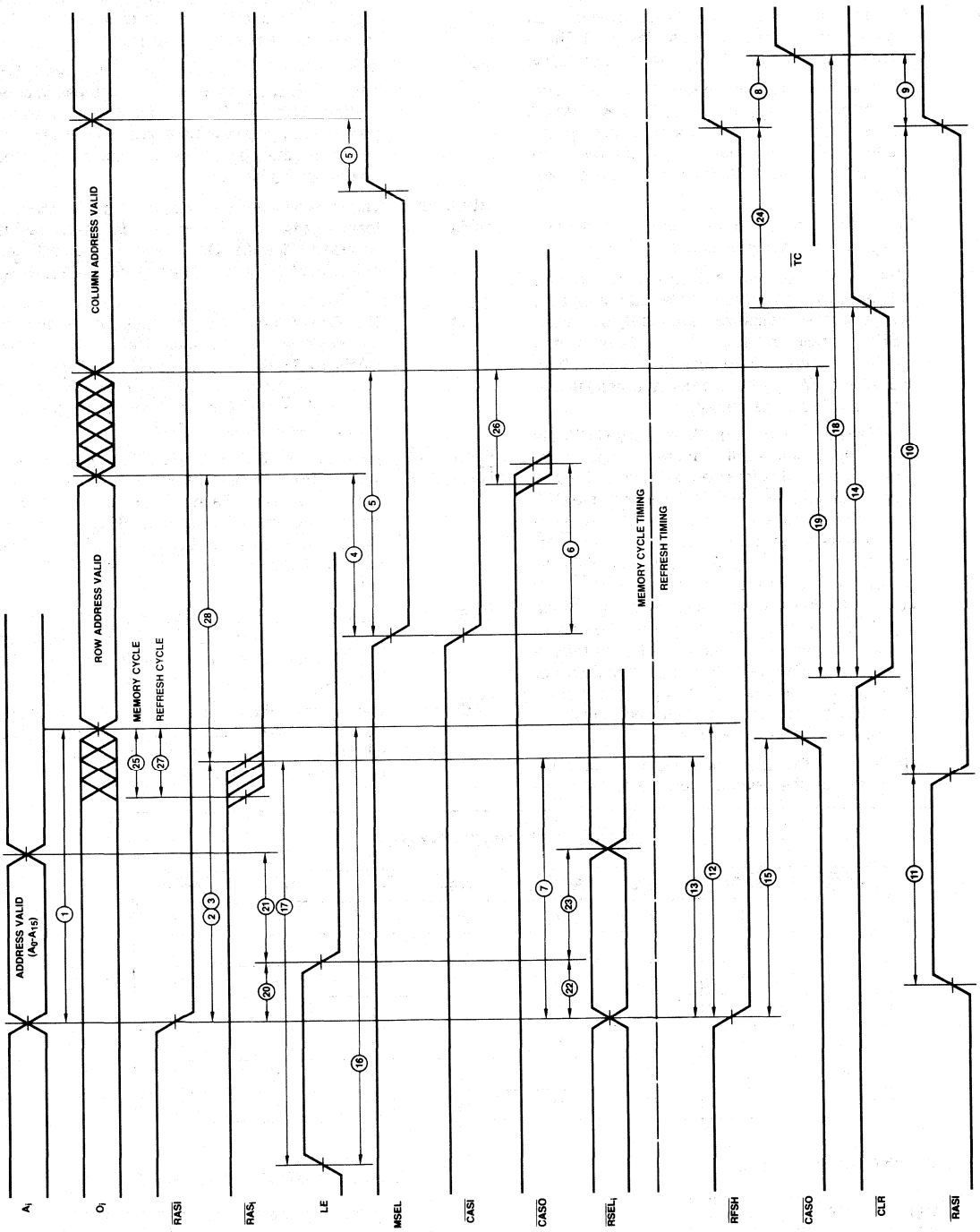
Notes:
5. Minimum spec limits for t_{PW}, t_S and t_H are minimum system operating requirements. Limits for t_{SKEW} and t_{PD} are guaranteed test limits for the device.
6. All AC parameters are specified at the 1.5V level.
7. $\overline{RFSH}$ inhibits $\overline{CASO}$ during refresh. Specification is for $\overline{CASO}$ inhibit time.
8. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = HIGH) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest A_i to O_i delay within a single device. O_i to $\overline{CASO}$ skew is maximum difference between fastest $\overline{CASI}$ to $\overline{CASO}$ delay and slowest MSEL to O_i delay within a single device. See application section entitled Memory Cycle Timing for correlation to System Timing requirements.
9. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = LOW) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest $\overline{RFSH}$ to O_i delay within a single device. See application section on Refresh Timing for correlation to system refresh timing requirements.
10. O_i to $\overline{RAS_i}$ (MSEL = ↿) skew is guaranteed maximum difference between fastest MSEL ↿ to O_i delay and slowest $\overline{RASI}$ to $\overline{RAS_i}$ delay within a single device.

7

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR C_L = 150pF

(Notes 5, 6)

				COM'L		MIL			
			T_A = +25°C, V_{CC} = 5.0V	T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		T_C = −55°C to +125°C, V_{CC} = 5.0V ± 10%			Test
Parameter		Description	Typ.	Min.	Max.	Min.	Max.	Units	Conditions
1	t_{PD}	A_i to O_i Delay	20		25		30	ns	C_L = 150pF
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)	18		24		27	ns	
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)	18		24		27	ns	
4	t_{PD}	MSEL to O_i	23	12		12		ns	
5	t_{PD}	MSEL to O_i	23		27		31	ns	
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)	17		24		26	ns	
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)	19		27		30	ns	
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)	34		45		55	ns	
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)	32		45		55	ns	
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)	10	50		50		ns	
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)	10	50		50		ns	
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)	21		27		30	ns	
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)	25		33		36	ns	
14	t_{PW}	$\overline{CLR}$ = L	0	30		35		ns	
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)	21		27		31	ns	
16	t_{PD}	LE to O_i	30		40		50	ns	
17	t_{PHL}	LE to $\overline{RAS_i}$	34		45		54	ns	
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$	39		55		60	ns	
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)	38		50		62	ns	
20	t_S	A_i to LE Set-up Time	0	5		5		ns	
21	t_H	A_i to LE Hold Time	5	12		12		ns	
22	t_S	$RSEL_i$ to LE Set-up Time	0	5		5		ns	
23	t_H	$RSEL_i$ to LE Hold Time	10	17		25		ns	
24	t_S	$\overline{CLR}$ Recovery Time	5	12		15		ns	
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)	3		6		7	ns	
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)	4		7		8	ns	
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)	6		9		10	ns	
28	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{MSEL}$ = ↯, Note 10)	1		5		5	ns	



Am2964B Dynamic Memory Controller Timing

7

DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 The low order Address inputs are used to latch eight Row Address inputs for the RAM. These inputs drive the outputs 0_0-0_7 when MSEL is HIGH.

A_8-A_{15} The high order Address inputs are used to latch eight Column Address inputs for the RAM. These inputs drive the outputs 0_0-0_7 when MSEL is LOW.

A_{15} A_{15} is a dual input. With normal TTL level inputs A_{15} acts as address input A_{15} for 64K RAMs. If A_{15} is pulled up to +12V through a 1KΩ resistor, the terminal count output, $\overline{TC}$, will go LOW every 128 counts (for 16K RAMs) instead of every 256 counts.

0_0-0_7 The RAM address outputs. The eight-bit width is designed for dynamic RAMs up to 64K.

MSEL The Multiplexer-SELect input determines whether low order or high order address inputs appear at the multiplexer outputs 0_0-0_7. When MSEL is HIGH the low order address latches (A_0-A_7) are connected to the outputs. When MSEL is LOW the high order address latches are connected to the outputs.

$\overline{RFSH}$ The Refresh control input. When active LOW the $\overline{RFSH}$ input switches the address output multiplexer to output the inverted contents of the 8-bit refresh counter. $\overline{RFSH}$ LOW also inhibits the $\overline{CAS}$ buffer and changes the mode of the $\overline{RAS}$ decoder from one-of-four to four-of-four so that all four $\overline{RAS}$ decoder outputs, $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ and $\overline{RAS_3}$, go LOW in response to a LOW input at $\overline{RASI}$. This action refreshes one row address in each of the four $\overline{RAS}$ decoded memory banks. The refresh counter is advanced at the end of each refresh cycle by the LOW-to-HIGH transition of $\overline{RFSH}$ or $\overline{RASI}$ (whichever occurs first). In burst mode refresh, $\overline{RFSH}$ may be held LOW and refresh accomplished by toggling $\overline{RASI}$.

$\overline{TC}$ The Terminal Count output. A LOW output at $\overline{TC}$ indicates that the refresh counter has been sequenced through either 128 or 256 refresh addresses depending on A_{15}. The $\overline{TC}$ output remains active LOW until the refresh counter is advanced by the rising edge of $\overline{RASI}$ or $\overline{RFSH}$.

$\overline{CLR}$ The refresh counter Clear input. An active LOW input at $\overline{CLR}$ resets the refresh counter to all LOW (refresh address output to all HIGH).

LE The address latch enable input. An active HIGH input at LE causes the two 8-bit address latches and the 2-bit $\overline{RAS}$ Select input latch to go transparent, accepting new input data. A LOW input on LE latches the input data which meets set-up and hold time requirements.

$RSEL_0$ and $RSEL_1$ The $\overline{RAS}$ decoder Select inputs. Data (latched) at these inputs (normally higher order addresses) is decoded by the $\overline{RAS}$ Decoder to "$\overline{RAS}$ Select" one of four banks of memory with $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ or $\overline{RAS_3}$.

$\overline{RASI}$ The Row Address Strobe Input. During normal memory cycles the selected $\overline{RAS}$ Decoder output $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ or $\overline{RAS_3}$ will go active LOW in response to an active LOW input at $\overline{RASI}$. During refresh ($\overline{RFSH}$ = LOW), all $\overline{RAS}$ outputs go LOW in response to $\overline{RASI}$ = LOW.

$\overline{RAS_0}$, $\overline{RAS_1}$ $\overline{RAS_2}$, $\overline{RAS_3}$ Row Address Strobe outputs ($\overline{RAS_i}$). Each provides a Row Address Strobe for one of the four banks of memory. Each will go active LOW only when selected by $RSEL_0$ and $RSEL_1$ and only when $\overline{RASI}$ goes active LOW. All $\overline{RAS_{0\text{-}3}}$ outputs go active low in response $\overline{RASI}$ when $\overline{RFSH}$ goes LOW.

$\overline{CASI}$ The Column Address Strobe. An active LOW input at $\overline{CASI}$ will result in an active LOW output at $\overline{CASO}$, unless a refresh cycle is in progress ($\overline{RFSH}$ = LOW).

$\overline{CASO}$ The Column Address Strobe output. The active LOW $\overline{CASO}$ output strobes the Column Address into the dynamic RAM. $\overline{CASO}$ is inhibited during refresh ($\overline{RFSH}$ = LOW).

$\overline{RAS}$ OUTPUT FUNCTION TABLE

$\overline{RFSH}$	$\overline{RASI}$	$RSEL_1$	$RSEL_0$	$\overline{RAS_0}$	$\overline{RAS_1}$	$\overline{RAS_2}$	$\overline{RAS_3}$
L	H	X	X	H	H	H	H
L	L	X	X	L	L	L	L
H	H	X	X	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	H	H	L	H	H
H	L	H	L	H	H	L	H
H	L	H	H	H	H	H	L

$\overline{CASO}$ FUNCTION TABLE

$\overline{RFSH}$	$\overline{CASI}$	$\overline{CASO}$
H	L	L
H	H	H
L	X	H

ADDRESS OUTPUT FUNCTION TABLE

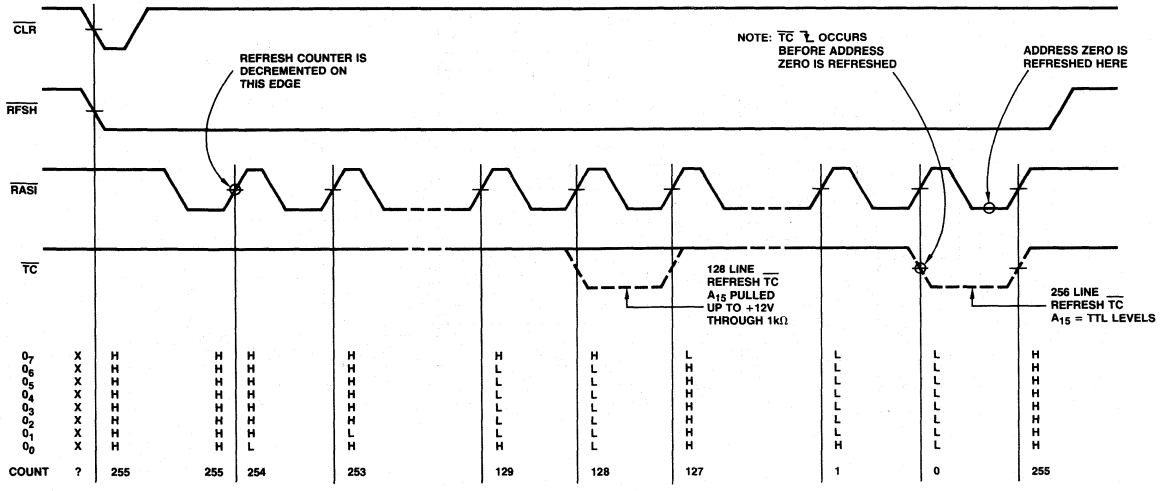
MSEL	$\overline{RFSH}$	0_0-0_7
H	H	A_0-A_7
L	H	A_8-A_{15}
X	L	Refresh Address

REFRESH ADDRESS COUNTER FUNCTION TABLE

A_{15}	$\overline{CLR}$	$\overline{RFSH}$	$\overline{RASi}$	$\overline{TC}$	REFRESH COUNT	FUNCTION
X	L	X	X	X	FF_H	Clear Counter
X	H	↓	X	X	NC	Output Refresh Address No Change for Counter
X	H	↓	L	X	Count – 1	Return to Memory Cycle Mode and Decrement Counter
X	H	L	↓	X	NC	Output all RAS_i to RAM No Change for Counter
X	H	L	↓	X	Count – 1	Return RAS_i to HIGH and Decrement Counter
L or H	H	X	X	L	00_H	Terminal Count for 256 Line Refresh
+12V*	H	X	X	L	00_H and 80_H	Terminal Count for 128 Line Refresh

*Through 1 kΩ resistor.

BURST REFRESH TIMING



The timing shown assumes that burst mode applications may power-down the Am2964B with the RAM. Therefore the counter is cleared prior to executing the refresh sequence.

APPLICATION

ARCHITECTURE

The Dynamic Memory Controller (DMC) provides address multiplexing, refresh address generation and $\overline{RAS}/\overline{CAS}$ control for the MOS dynamic RAM memories of any data width. The eight bit address path is designed for 64K RAMs and can be used with 16K RAMs.

Sixteen address input latches and two $\overline{RAS}$ Select latches (for higher order addresses) allow the DMC to control up to 256K words of memory (with 64K RAMs) by using the internal $\overline{RAS}$ decoder to select from one-of-four banks of RAMs.

SPEED WITH MINIMUM SKEW

The DMC provides Schottky speed in all of the critical paths. In addition, time skew between the Address, $\overline{RAS}$ and $\overline{CAS}$ paths is minimized (and specified) by placing these functions on the same chip. The inclusion of the $\overline{CAS}$ buffer allows matching of its propagation delay, plus provides the $\overline{CAS}$ inhibit function during $\overline{RAS}$ – only refresh.

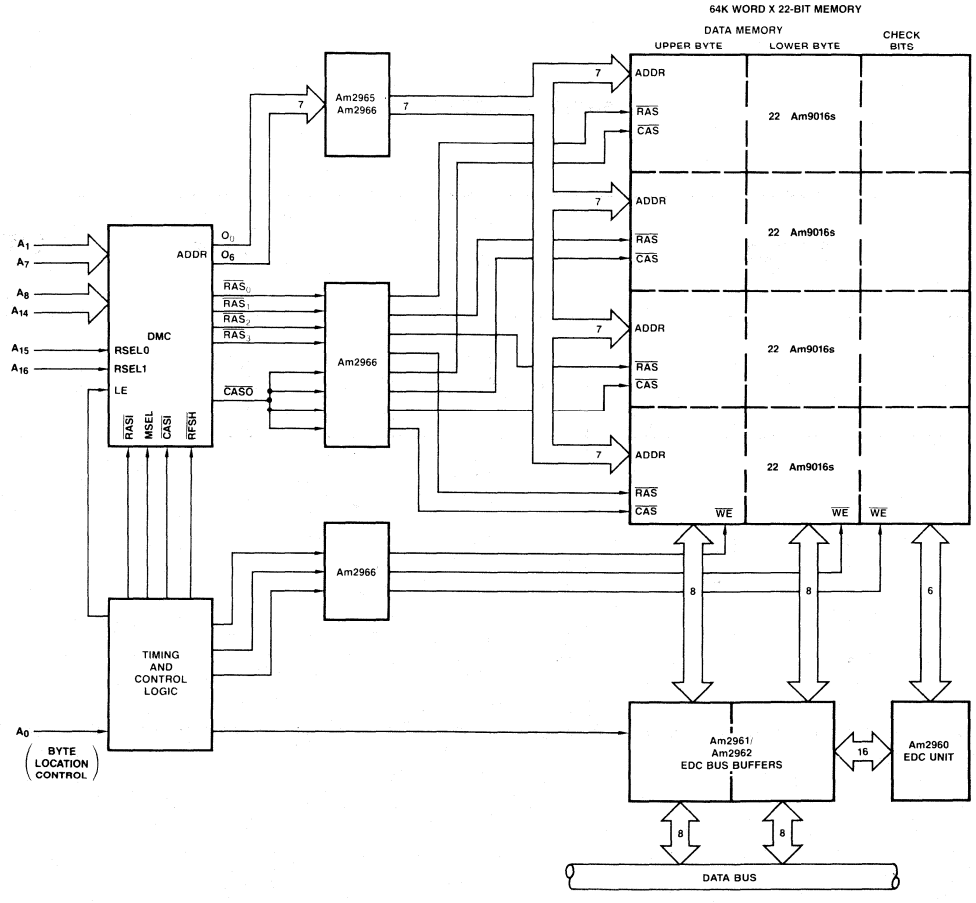
INPUT LATCHES

The eighteen input latches are transparent when LE is HIGH and latch the input data meeting set-up and hold time requirements when LE goes LOW. In systems with separate address and data buses, LE may be permanently enabled HIGH.

REFRESH COUNTER

The 8-bit refresh counter provides both 128 and 256 line refresh capability. Refresh control is external to allow maximum user flexibility. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counter is advanced at the LOW-to-HIGH transition of $\overline{RFSH}$ (or $\overline{RASI}$). This assures a stable counter output for the next refresh cycle. The counter will continue to cycle through 256 addresses unless reset to zero by $\overline{CLR}$. This actually causes all outputs to go HIGH since the output MUX is inverting. (Address inputs to outputs are non-inverting since both the input latches and output MUX are inverting).



*Address and $\overline{RAS}/\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}/\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

Figure 1. Dynamic Memory Control with Error Detection and Correction

REFRESH TERMINAL COUNT

The refresh counter also provides a Terminal Count output for burst mode refresh applications. $\overline{TC}$ normally occurs at count 255 (0_7 to 0_7 all LOW when $\overline{RFSH}$ is LOW). $\overline{TC}$ can be made to occur at count 127 for 128 line burst mode refresh by pulling A_{15} up to +12V through a 1KΩ ± 10% resistor. The counter actually cycles through 256 with $\overline{TC}$ determined by A_{15}. Otherwise A_{15} functions as an address input when driven at normal TTL levels.

THREE INPUT 8-BIT ADDRESS MULTIPLEXER

The address MUX is 8-bits wide (for 64K RAMs) and has three data sources, the lower address input latch (A_0 to A_7), the upper address input latch (A_8 to A_{15}) and the internal refresh counter. The lower address latch is selected when MSEL is HIGH. This is normally the Row address. The upper address latch is selected when MSEL is LOW. This is normally the Column address. The third source – the refresh counter is selected when $\overline{RFSH}$ is LOW and overrides MSEL.

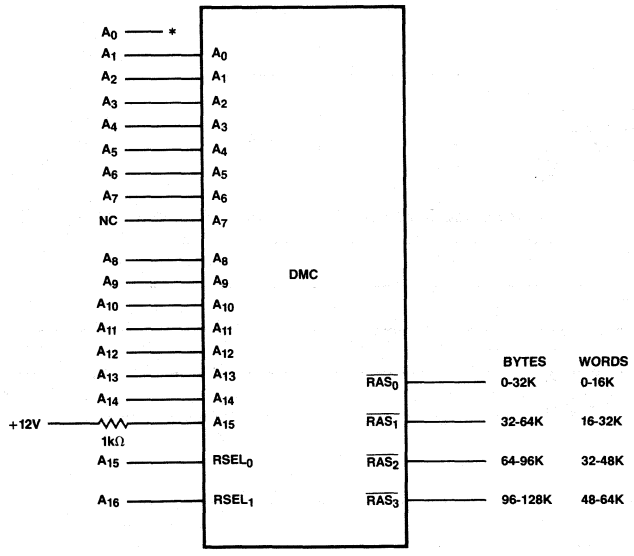
When $\overline{RFSH}$ goes LOW, the MUX selects the refresh counter address and $\overline{CASO}$ is inhibited. Also, the $\overline{RAS}$ Decoder function is changed from one-of-four to four-of-four so all $\overline{RAS}$ outputs $\overline{RAS_0}$-$\overline{RAS_3}$ go LOW to refresh all banks of memory when $\overline{RASI}$ goes LOW. When $\overline{RFSH}$ is HIGH only one $\overline{RAS}$ output goes low, determined by the $\overline{RAS}$ Select inputs, $RSEL_0$ and $RSEL_1$. In either case the $\overline{RAS}$ Decoder output timing is controlled by $\overline{RASI}$ to make sure the refresh count appears at 0_0-0_7 before $\overline{RAS_0}$-$\overline{RAS_3}$ go LOW. This assures meeting Row address Set-up time requirement of the RAM (t_{ASR}).

MAXIMUM PERFORMANCE SYSTEM

The typical organization of a maximum performance 16-bit system including Error Detection and Correction is shown in Figure 1. Delay lines provide the most accurate timing and are recommended for $\overline{RAS}$/MSEL/$\overline{CAS}$ timing in this type of system.

CONTROLLING 16K RAMS OR SMALLER SYSTEMS

16K RAMs require seven address inputs and 128 line refresh. Also, A_0 is often used to designate upper or lower byte transactions in 16-bit systems. These modifications are shown in Figure 2.



*A_0 Controls Byte Select Logic

Figure 2. Word Organized Memory Using 16K RAMs

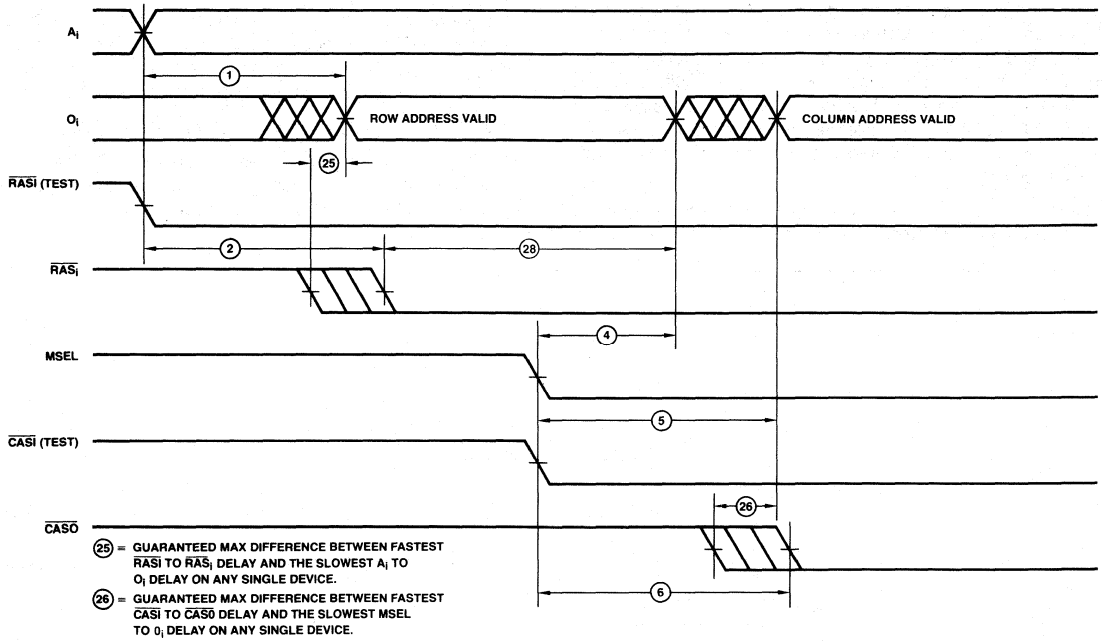
MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 3. T_1, T_2 and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that RAM timing requirements are met and that maximum system performance is achieved.

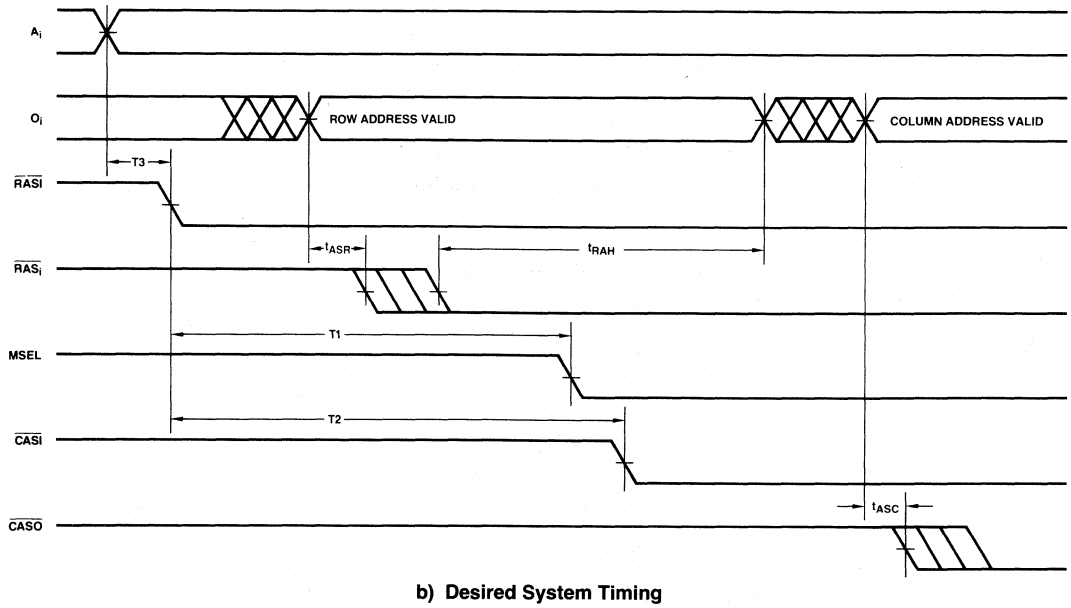
The minimum requirement for T_1, T_2, and T_3 are as follows:

$T_1MIN = t_{RAH} + t_{28}$
$T_2MIN = T_1 + t_{26} + t_{ASC}$
$T_3MIN = t_{ASR} + t_{25}$

See RAM data sheet for applicable values for t_{RAH}, t_{ASC} and t_{ASR}.



a) Specifications Applicable to Memory Cycle Timing



b) Desired System Timing

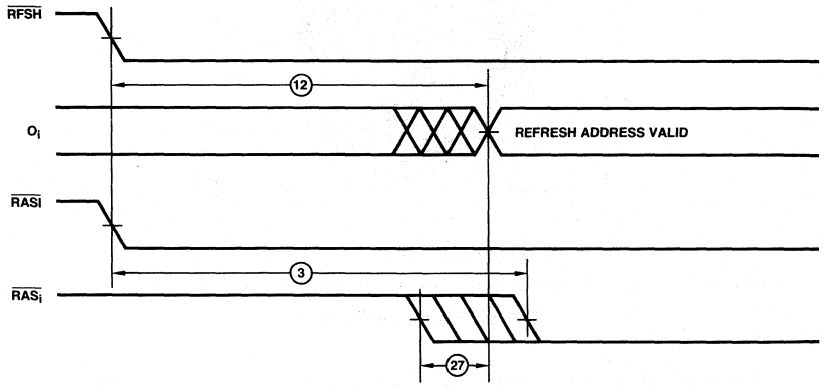
Figure 3. Memory Cycle Timing

REFRESH CYCLE TIMING

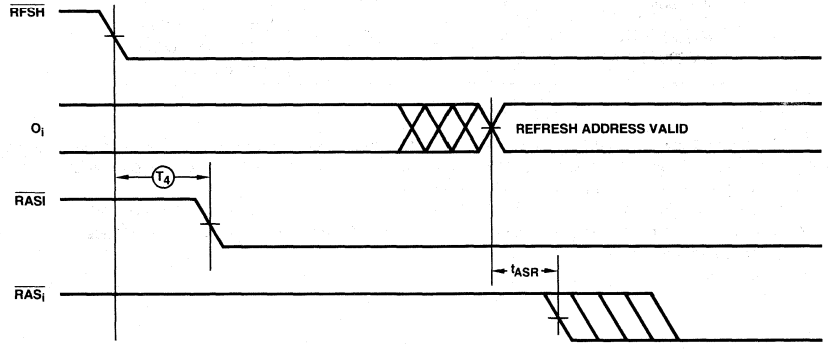
The timing relationships for refresh are shown in Figure 4.

T_4 minimum is calculated as follows:

$T_4 = t_{ASR} + t_{27}$



a) Test Waveforms

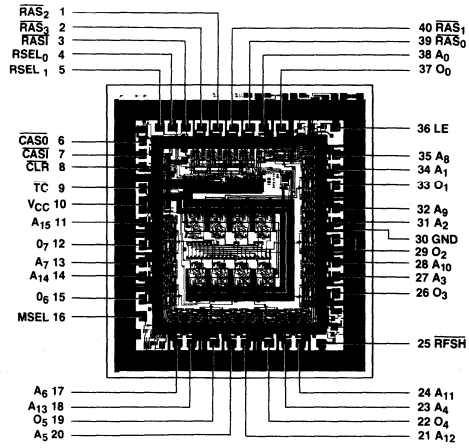


(27) = GUARANTEED MAX DIFFERENCE BETWEEN FASTEST $\overline{RASI}$ TO $\overline{RAS_i}$ DELAY AND SLOWEST $\overline{RFSH}$ TO O_i DELAY ON ANY SINGLE DEVICE.

b) Desired System Timing

Figure 4. Refresh Timing

Metallization and Pad Layout



DIE SIZE 0.156" X 0.143"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2964B Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2964BPC	P-40	C	C-1
AM2964BDC	D-40	C	C-1
AM2964BDC-B	D-40	C	B-2 (Note 4)
AM2964BDM	D-40	M	C-3
AM2964BDM-B	D-40	M	B-3
AM2964BFM	F-42	M	C-3
AM2964BFM-B	F-42	M	B-3
AM2964BXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B
AM2964BXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

This device is also characterized as:
AmZ8165
AmZ8166

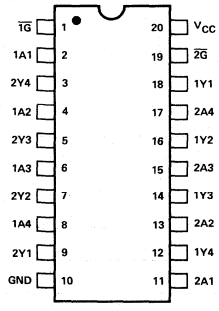
Am2965 • Am2966

Octal Dynamic Memory Drivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- **Controlled rise and fall characteristics**
  Internal resistors provide symmetrical drive to HIGH and LOW states, eliminating need for external series resistor.
- **Output swings designed to drive 16K and 64K RAMs**
  V_{OH} guaranteed at V_{CC} −1.15V. Undershoot going LOW guaranteed at less than 0.5V.
- **Large capacitive drive capability**
  35mA min source or sink current at 2.0V. Propagation delays specified for 50pF and 500pF loads.
- **Pin-compatible with 'S240 and 'S244**
  Non-inverting Am2966 replaces 74S244; inverting Am2965 replaces 74S240. Faster than 'S240/244 under equivalent load.
- **No-glitch outputs**
  Outputs forced into OFF state during power up and down. No glitch coming out of three-state.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-125

FUNCTIONAL DESCRIPTION

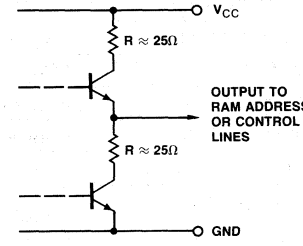
The Am2965 and Am2966 are designed and specified to drive the capacitive input characteristics of the address and control lines of MOS dynamic RAMs. The unique design of the lower output driver includes a collector resistor to control undershoot on the HIGH-to-LOW transition. The upper output driver pulls up to V_{CC} − 1.15V to be compatible with MOS memory and is designed to have a rise time symmetrical with the lower output's controlled fall time. This allows optimization of Dynamic RAM performance.

The Am2965 and Am2966 are pin-compatible with the popular 'S240 and 'S244 with identical 3-state output enable controls. The Am2965 has inverting drivers and the Am2966 has non-inverting drivers.

The inclusion of an internal resistor in the lower output driver eliminates the requirement for an external series resistor, therefore reducing package count and the board area required. The internal resistor controls the output fall and undershoot without slowing the output rise.

These devices are designed for use with the Am2964 Dynamic Memory Controller where large dynamic memories with highly capacitive input lines require additional buffering. Driving eight address lines or four $\overline{RAS}$ and four $\overline{CAS}$ lines with drivers on the same silicon chip also provides a significant performance advantage by minimizing skew between drivers. Each device has specified skew between drivers to improve the memory access worst case timing over the min and max t_{PD} difference of unspecified devices.

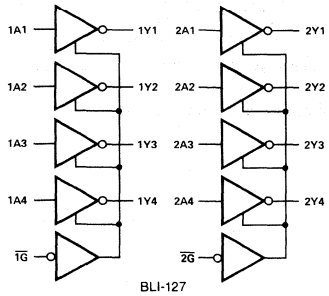
TYPICAL OUTPUT DRIVER



BLI-126

LOGIC DIAGRAMS

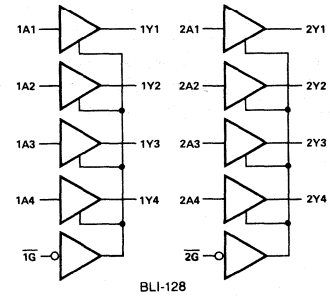
Am2965



BLI-127

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am2966



BLI-128

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +7.0V
DC Output Current, into Outputs	200mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2965/66XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V	MAX = 5.50V)
Am2965/66XM, DM	T_A = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V	MAX = 5.50V)
Am2965/66FM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V	MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1mA	V_{CC}−1.15	V_{CC}−0.7V		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.5	Volts
			I_{OL} = 12mA			0.8	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	DATA			−200	μA
			$\overline{1G}$, $\overline{2G}$			−400	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZH}	Off-State Current	V_O = 2.7V				100	μA
I_{OZL}	Off-State Current	V_O = 0.4V				−200	μA
I_{OL}	Output Sink Current	V_{OL} = 2.0V		50			mA
I_{OH}	Output Source Current	V_{OH} = 2.0V		−35			mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−60 (see I_{OH})		−200	mA
I_{CC}	Supply Current	Am2965	All Outputs HIGH	V_{CC} = MAX, Outputs Open		24	50	mA
			All Outputs LOW			86	125	
			All Outputs Hi-Z			86	125	
		Am2966	All Outputs HIGH	V_{CC} = MAX, Outputs Open		53	75	
			All Outputs LOW			92	130	
			All Outputs Hi-Z			116	150	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2965 • Am2966
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

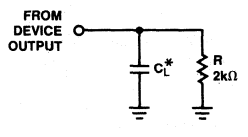
Parameters	Description	Test Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time from LOW-to-HIGH Output	Figure 1 Test Circuit Figure 3 Voltage Levels and Waveforms	C_L = 0pF		6	(Note 4)	ns
			C_L = 50pF	6	9	15	
			C_L = 500pF	18	22	30	
t_{PHL}	Propagation Delay Time from HIGH-to-LOW Output		C_L = 0pF		4	(Note 4)	ns
			C_L = 50pF	5	7	15	
			C_L = 500pF	18	22	30	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4, S = 1			11	20	ns
t_{PHZ}		Figures 2 and 4, S = 2			6.5	12	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4, S = 1			12	20	ns
t_{PZH}		Figures 2 and 4, S = 2			12	20	
t_{SKEW}	Output-to-Output Skew	Figures 1 and 3, C_L = 50pF			±0.5	±3.0 (Note 5)	ns
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			0	−0.5	Volts

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Note 6)

Parameters	Description	Test Conditions		COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±10% Min	COM'L Max	MIL (Note 7) T_A = −55 to +125°C V_{CC} = 5.0V ±10% Min	MIL Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	Figures 1 and 3	C_L = 50pF	4	17	4	20	ns
			C_L = 500pF	18	35	18	40	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output	Figures 1 and 3	C_L = 50pF	4	17	4	20	ns
			C_L = 500pF	18	35	18	40	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4	S = 1		24		24	ns
t_{PHZ}			S = 2		16		16	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4	S = 1		28		28	ns
t_{PZH}			S = 2		28		28	
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			−0.5		−0.5	Volts

Notes: 4. Typical time shown for reference only – not tested.
5. Time Skew specification is guaranteed by design but not tested.
6. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
7. T_C = −55 to +125°C for Flatpak versions.

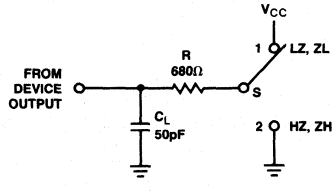
SWITCHING TEST CIRCUITS



BLI-129

*t_{pd} specified at C = 50 and 500pF.

Figure 1. Capacitive Load Switching.

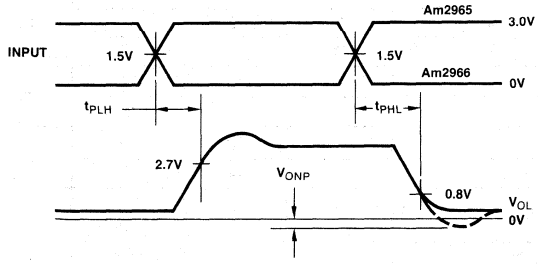


BLI-130

Figure 2. Three-State Enable/Disable.

TYPICAL SWITCHING CHARACTERISTICS

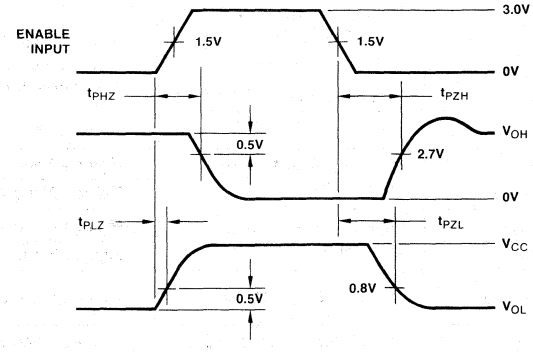
VOLTAGE WAVEFORMS



BLI-131

$t_r = t_f = 2.5ns$
$f = 2.5MHz$
$t_{pw} = 200ns$

Figure 3. Output Drive Levels.



BLI-132

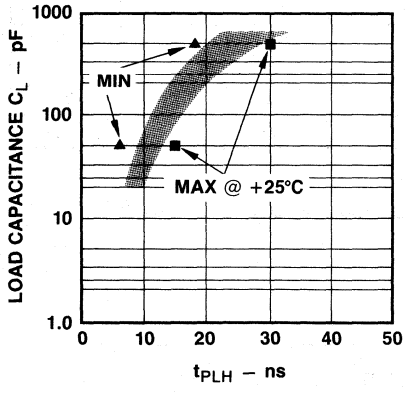
$t_r = t_f = 2.5ns$
$f = 1MHz$
$t_{pw} = 800ns$

Figure 4. Three-State Control Levels.

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈25Ω both HIGH and LOW), and by pulling up to MOS V_{OH} levels (V_{CC} − 1.5V). External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.

The curves shown below provide performance characteristics typical of both the inverting (Am2965) and non-inverting (Am2966) RAM Drivers.



BLI-133

Figure 5. t_{PLH} for V_{OH} = 2.7 Volts vs. C_L.

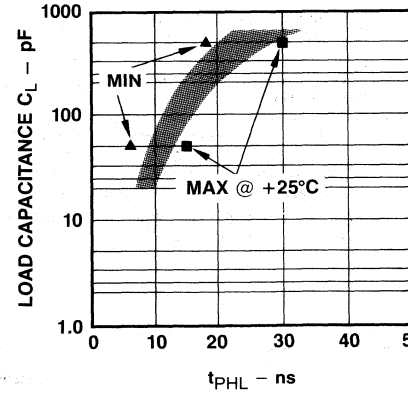
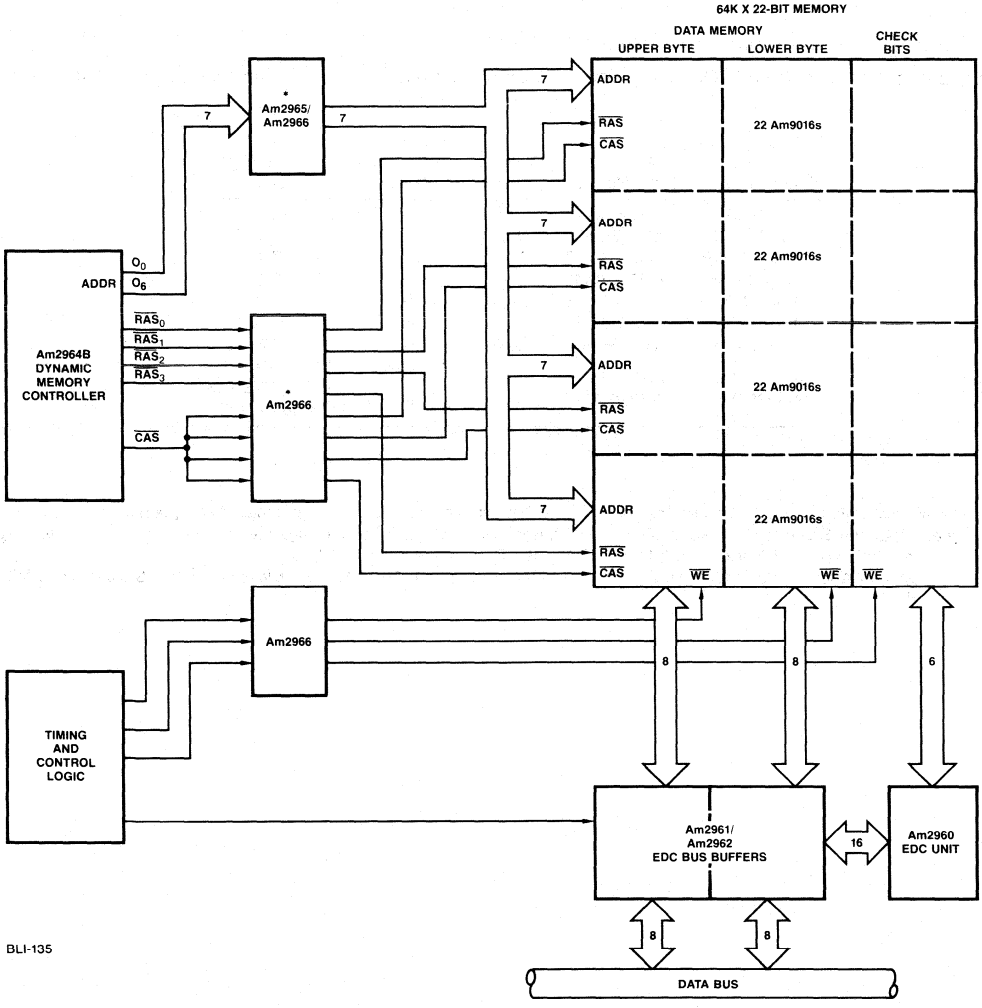


Figure 6. t_{PHL} for V_{OL} = 0.8 Volts vs. C_L.

The curves above depict the typical tPLH and tPHL for the RAM Driver outputs as a function of load capacitance. The minimums and maximums are shown for worst case design. The typical band is provided as a guide for intermediate capacitive loads.

APPLICATION

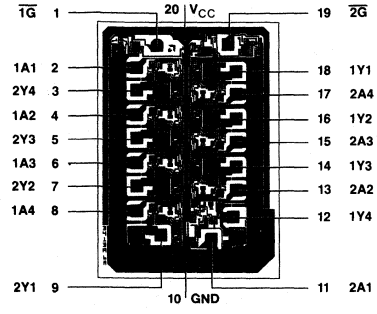


*Address and $\overline{RAS}$/$\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}$/$\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

DYNAMIC MEMORY CONTROL WITH ERROR DETECTION AND CORRECTION

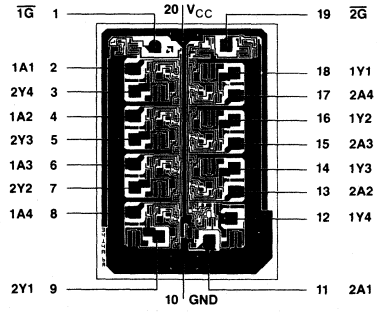
Metallization and Pad Layouts

Am2965



DIE SIZE 0.094" X 0.060"

Am2966



DIE SIZE 0.094" X 0.066"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2965 Order Number	Am2966 Order Number	Package Type	Temperature Range	Screening Level
AM2965PC	AM2966PC	P-20	C	C-1
AM2965DC	AM2966DC	D-20	C	C-1
AM2965DCB	AM2966DCB	D-20	C	B-1
AM2965DM	AM2966DM	D-20	M	C-3
AM2965DMB	AM2966DMB	D-20	M	B-3
AM2965FM	AM2966FM	F-20	M	C-3
AM2965FMB	AM2966FMB	F-20	M	B-3
AM2965XC	AM2966XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2965XM	AM2966XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless othewise specified.
2. C = 0 to 70°C, V_{CC} = 4.50V to 5.50V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2965 • Am2966

DYNAMIC MEMORY DRIVERS IMPROVE MEMORY PERFORMANCE

By John Mick and Roy Levy

OVERVIEW

The Am2965 and Am2966 are bipolar octal drivers for 16K and 64K dynamic RAMs. The devices offer a guaranteed maximum undershoot of −0.5V without requiring external resistors. The Am2965 and Am2966 feature a t_{PD} minimum and maximum specified at 50pF and 500pF. The V_{OH} is guaranteed at V_{CC} −1.15V minimum, and I_{OH} and I_{OL} are specified at +2.0V for minimum guarantee of charging capacitance. There are glitch-free three-state outputs during power-up and power-down as well as symmetrical, controlled rise time and fall time.

While the Am2965 and Am2966 have low-power Schottky input characteristics and are pin-compatible replacement for design using the 'S240 and 'S244 (plus external resistors), the Am2965/2966 offer improved performance. The cost of the components is also comparable to Schottky buffer/external resistor systems.

To assure product quality, the Am2965 and Am2966 are specified for COM'L and MIL-STD-883.

INTRODUCTION

In the past, memory system designers have used Schottky devices such as the Am74S240 or Am74S244 to drive the highly capacitive inputs of MOS Dynamic RAMs. However, because of the distributed inductance and distributed capacitance associated with many dynamic RAMs on printed circuit board, resistors are usually placed in series with the Schottky TTL outputs to minimize undershoot and dampen the ringing that occurs when driving the inductive/capacitive load.

To achieve maximum performance in today's memory systems, the designer should use the Am2965 or the Am2966 to drive large arrays of MOS Dynamic RAMs. These devices increase system speed by providing high-capacity drive and optimizing the drive characteristic time constant. They provide a new system solution for solving these problems that eliminates the external resistor and guarantees the maximum undershoot will not exceed −0.5V.

The address lines on most dynamic RAMs are specified at 5pF maximum while the $\overline{RAS}$, write enable ($\overline{WE}$) and $\overline{CAS}$ inputs can be as high as 10pF. Thus the RAM driver's output must drive extremely high capacitive levels with good speed and without undershoot. When several dynamic RAMs are put onto a printed circuit board, the traces look inductive, so the result resembles a transmission line with distributed inductance and capacitance.

More than 0.5V of undershoot at the RAM inputs can create serious memory system problems by causing internal breakdown and loss of data in RAM chips and possibly damaging the RAM.

System designers must also maintain voltage levels at the RAM inputs. Specifications require the data lines to exceed 2.4V, and the $\overline{RAS}$ and $\overline{CAS}$ lines actually have to exceed 2.7V. Speed must then be maintained while driving all of that capacity.

THE RAM DRIVING PROBLEM

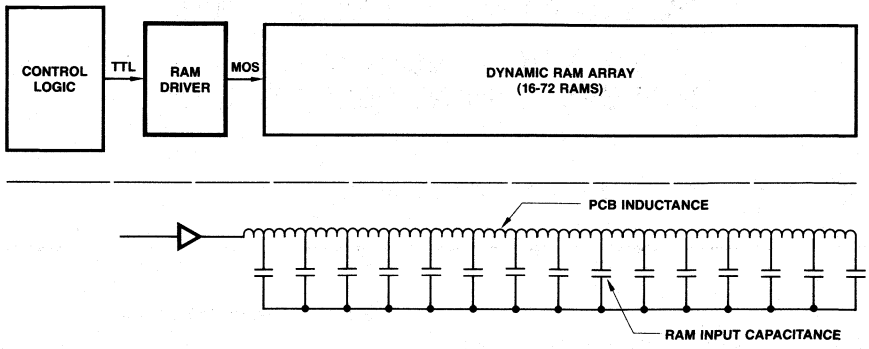
The situation can be pinpointed to an inductor/capacitance driving problem (Figure 1a). There is some inductance in series with the capacitance associated with each RAM input. In a simplified circuit, the inductance is being driven from a voltage having source impedance marked as R_S on Figure 1b. If the transition is LOW-to-HIGH, the voltage goes from LOW-to-HIGH with ringing at the HIGH state (Figure 2). Only above the 2.7V or 2.4V levels, depending upon the type of input, can a steady-state HIGH level be guaranteed on the RAM input. The rise time of the signal is a design consideration, recognizing the amount of capacitance being driven.

Conversely, when the signal drops from HIGH-to-LOW again, ringing can occur. If the ringing causes the voltage to go below ground, it is called undershoot. Figure 3a shows the signal falling to zero volts more quickly than the signal in Fig. 3b, resulting in a severe undershoot that takes longer to settle at the LOW steady state voltage. This delay time associated with the RC time constant is independent of the specification for the HIGH-to-LOW propagation delay time, t_{PHL}. It is a hidden delay that must be compensated for.

VOLTAGE SWING CONSIDERATIONS

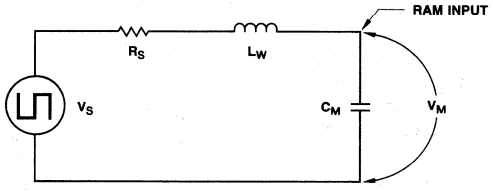
Recognizing that some ringing will occur, the system designer must determine how quickly the signal can be stabilized within the threshold limits of 0.5V below ground and 0.8V above ground. The best way to predict what happens with overshoot and undershoot is to examine the method of driving RAMs. Typically, it is done using one of several Schottky TTL devices connected directly to the RAM. Figure 4a shows an output transistor/resistor structure of a Schottky TTL device. When Q_1 is off and Q_2 is on, the LOW source impedance is about 3 ohms. When Q_2 is off and Q_1 is on, the HIGH impedance is that of the Q_1 transistor and the short circuit R_1. R_1 typically represents about 30-ohm source impedance, so that the source impedance HIGH and source impedance LOW represent a 10-to-1 difference with respect to each other (Figure 4b).

Other TTL devices can be driven in this way, but it is unacceptable for driving RAMs with this type of source impedance for several reasons. First, low source impedance in the LOW states causes ringing by turning on so fast that undershoot results at the RAM inputs. The impedance, however, drives well in the HIGH state. However, to solve the HIGH-to-LOW transition and undershoot problems a resistor is usually placed in series externally between the Schottky TTL gate and the RAM (Figure 4c). The resistor, of about 30 ohms, virtually eliminates undershoot by raising the source impedance in the LOW state to 33 ohms (Q_1 plus R_2).



Objective: Drive the load
- Avoid undershoot
- At MOS voltage levels
- Faster than Schottky

a) The RAM Driver Interface



V_S = the signal driving the chip
R_S = the output resistance of the driving source
L_W = the inductance of the circuit wiring between driving source and memory
C_M = input capacitance of memory chip
V_M = input signal to memory and voltage developed across capacitor

b) Model of Circuit Driving a Memory Chip

Figure 1.

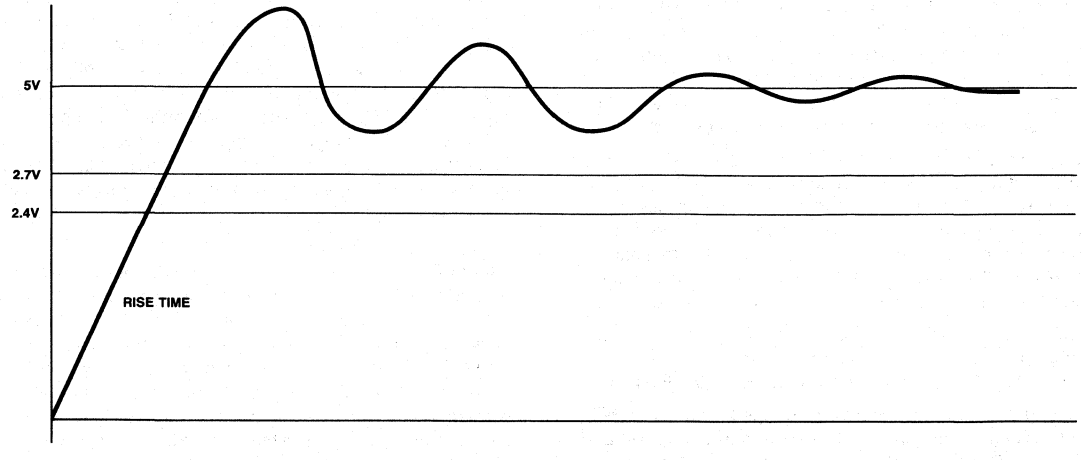


Figure 2. Overshoot in a Rising Signal

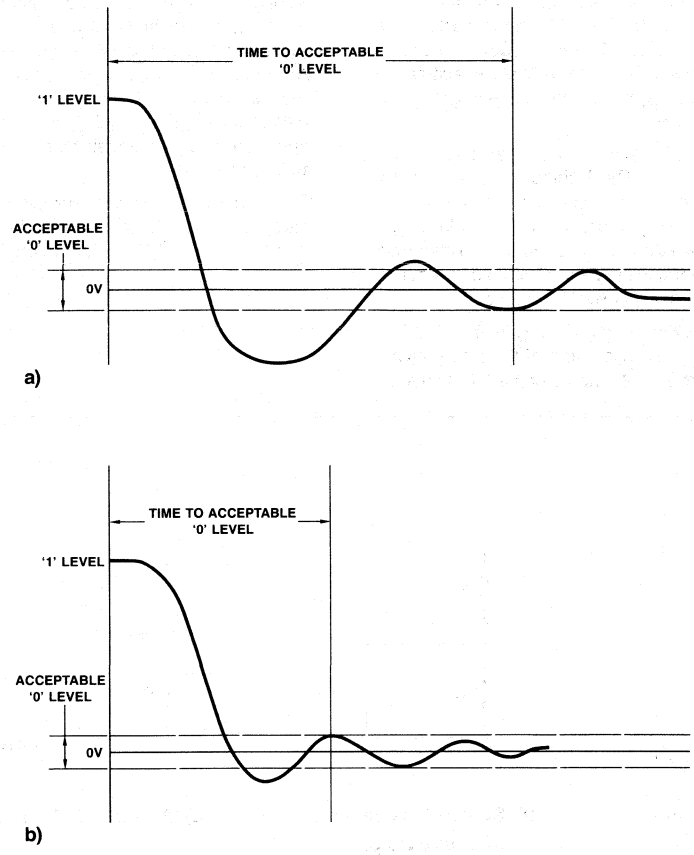


Figure 3. Undershoot in Falling Signals

When the HIGH state is turned on, the 30-ohm external resistor added to the 30-ohm terminal resistor in series totals 60 ohms of source impedance – an amount double of what is needed. While adding the external resistor in series solves undershoot, it causes the rise time (i.e., LOW-to-HIGH transition) to be slowed considerably – probably by a factor of two because resistance is doubled, so the RC time constant is doubled.

The ideal RAM driver source impedance is about 30 ohms in the HIGH state and 20 to 30 ohms in the LOW state (Figure 4d). The Am2965/2966 achieves the ideal RAM driver configuration by having approximately a 20- to 25-ohm source impedance in the LOW state and 25- to 30-ohm source impedance in the HIGH state. This ideal configuration is achieved by including a resistor (R_2) inside the Am2965/66 in series with the collector of Q_2. R_2 adds approximately a 15- to 20-ohm series resistance that has a source impedance in the LOW state of about 20 to 25 ohms and a source impedance in the HIGH state of about 25 to 30 ohms.

Remember, these figures are very nearly what was previously defined as the ideal RAM driver. What results is $R_1 + Q_1$ equivalent resistance in the HIGH state and $R_2 + Q_2$ resistance in the LOW state. The AMD family of RAM driver parts places the resistor inside and only increases the source impedance in the LOW state to achieve the ideal RAM driver configuration shown in Figures 4d and 4e. Now no resistor is needed outside the RAM driver as is typically used with today's Schottky devices.

APPLICATION

Figures 5a and 5b show typical overall memory subsystems for AmZ8000 and 2900 Family CPUs. The subsystems consist of the RAM drivers surrounding the RAMs almost directly; a dynamic memory controller; and interface, timing and controls required to drive the RAMS. There may also be an error detection and correction device as the figure shows.

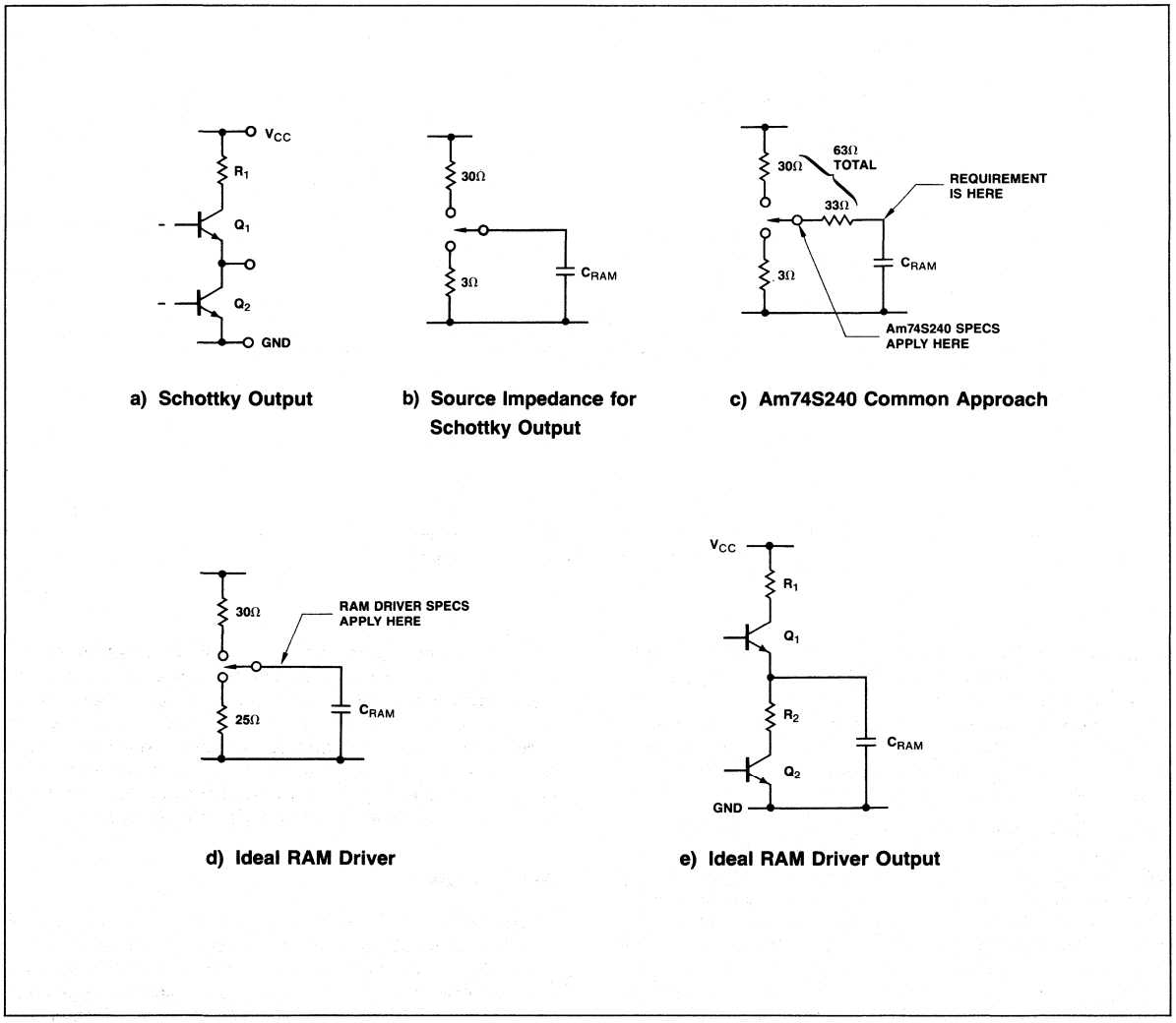
The objective of the memory subsystem is to drive the capacitive RAM inputs as rapidly as possible while meeting all the requirements for the undershoot and threshold levels. Figure 6 shows typical locations for RAM drivers to achieve this goal. Since a majority of the propagation delay times is an RC consideration, design flexibility allows the number of RAM input loads to be chosen for each RAM driver output. The best tradeoff includes fan-out choice and skew consideration. The skew specification for the Am2965 and Am2966 applies across the eight driver outputs but not between different devices.

The memory configuration of Figure 6 consists of an array of four rows by 16 columns of dynamic RAM chips for a total of 64 devices (Figure 7). The address drivers in Figure 6 have 16 x 4 x 5pF maximum = 320 pF (ignoring board capacitance) loading if one RAM driver drives all 64 RAM address inputs. Splitting this load with two RAM drivers reduces the capacitive load for each to 160pF and typically reduces the t_{PD} by 6 to 8nsec.

One of the unique aspects of the design in Figure 7 is the balanced number of loads on the $\overline{RAS}$ outputs of the RAM drivers and the number on loads of the $\overline{CAS}$ outputs of the RAM drivers.

Each driver drives the same number of RAMs. To balance the $\overline{CAS}$ line, the $\overline{CAS}$ inputs of four of the eight buffers are tied together on the RAM driver. Each RAM $\overline{RAS}$ and $\overline{CAS}$ input is 10pF maximum, so the $\overline{RAS}$ and $\overline{CAS}$ loading is 160pF at each RAM driver. The $\overline{CAS}$ inputs of each row are spread across four outputs to match the RAS loading and are shown using the same driver to reduce skew between the $\overline{RAS}$ and the $\overline{CAS}$ signals. The $\overline{WE}$ inputs are organized into upper and lower byte $\overline{WE}$ drive for each of the four rows. This amounts to 8 inputs x 10pF maximum = 80pF loading. By fanning out a full driver to the $\overline{WE}$ lines, four inputs are tied in parallel, balanced loading on the outputs are maintained.

If a full error detection and correction scheme shown in Figure 5 is used, all 22 bits in the row must be written simultaneously so a slightly different $\overline{WE}$ configuration would be used.



a) Schottky Output

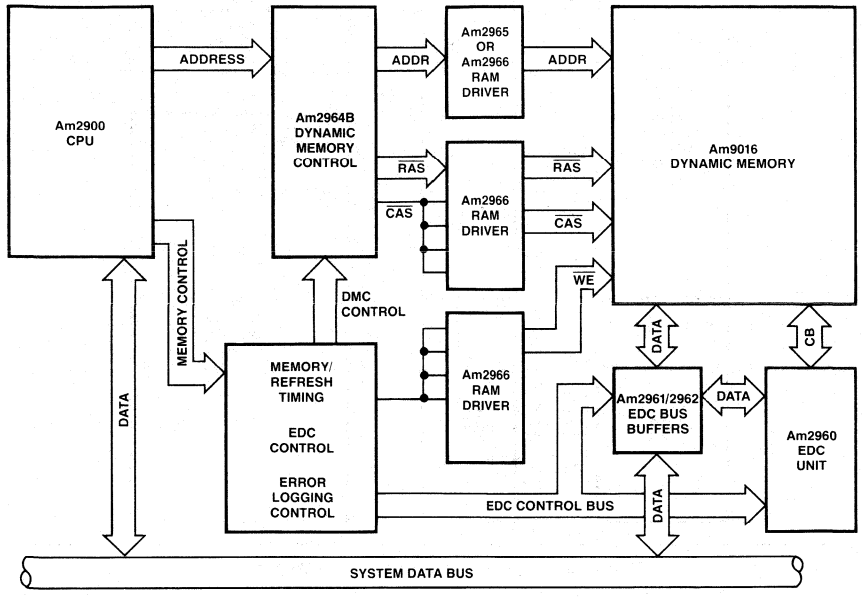
b) Source Impedance for Schottky Output

c) Am74S240 Common Approach

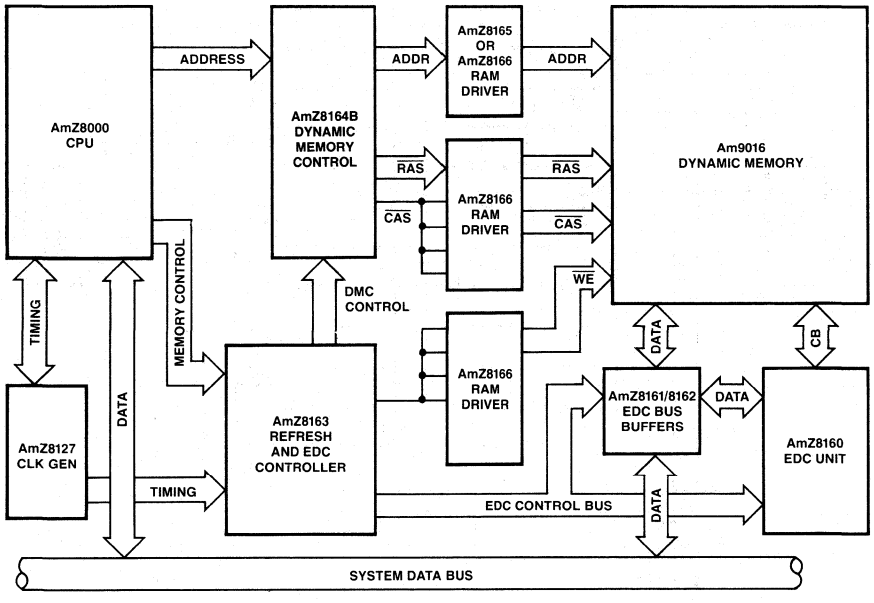
d) Ideal RAM Driver

e) Ideal RAM Driver Output

Figure 4. RAM Drivers vs. Schottky Output



a) High Performance Computer Memory



b) MOS Microcomputer Memory System

Figure 5. Overall Memory Subsystems for the Am2900 and AmZ8000 Family CPUs

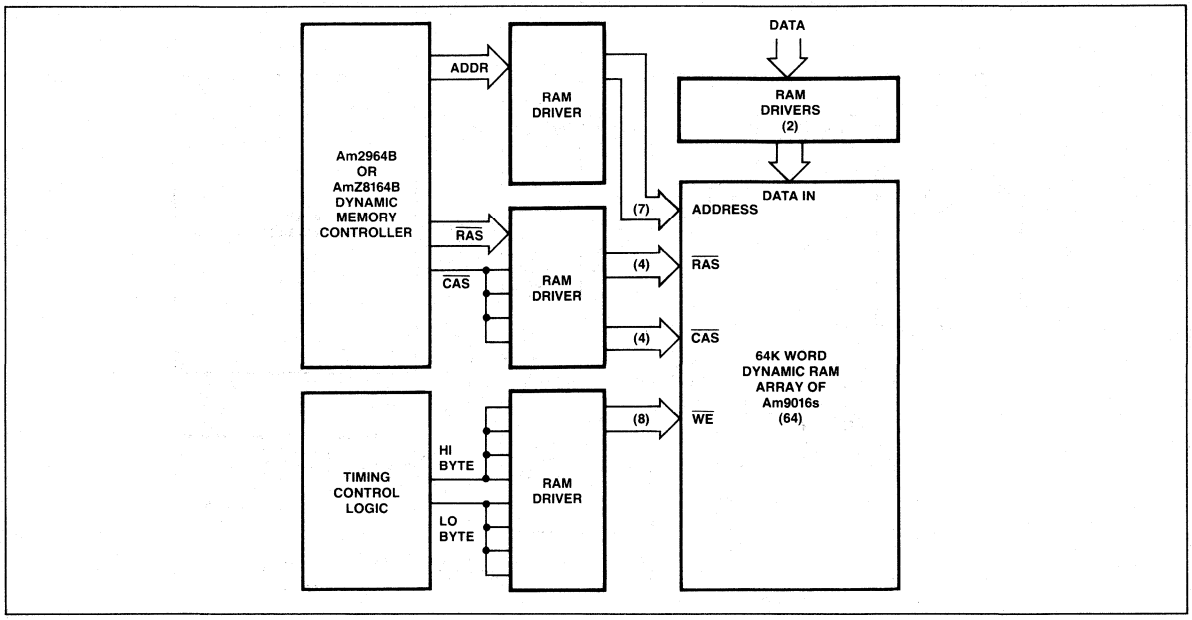


Figure 6. Typical Locations for RAM Drivers

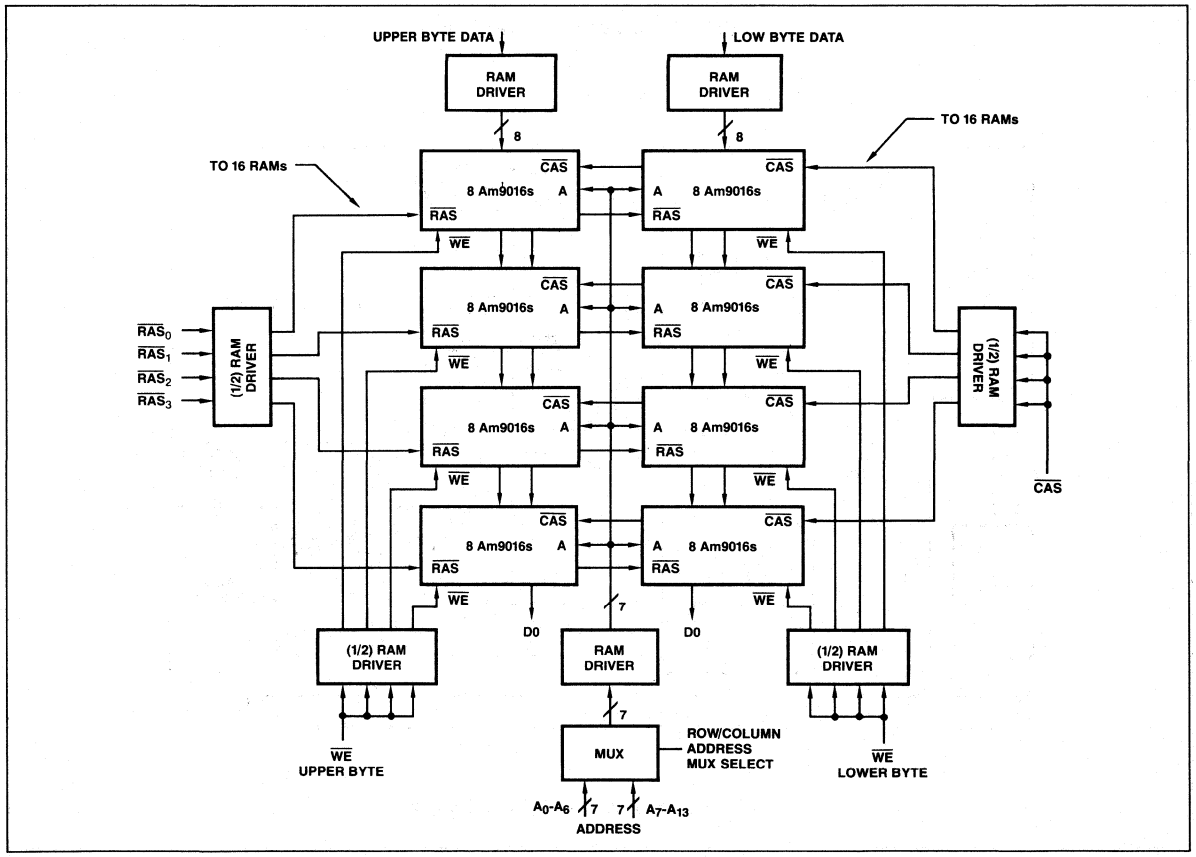


Figure 7. Typical 64K Word by 16-Bit Memory System

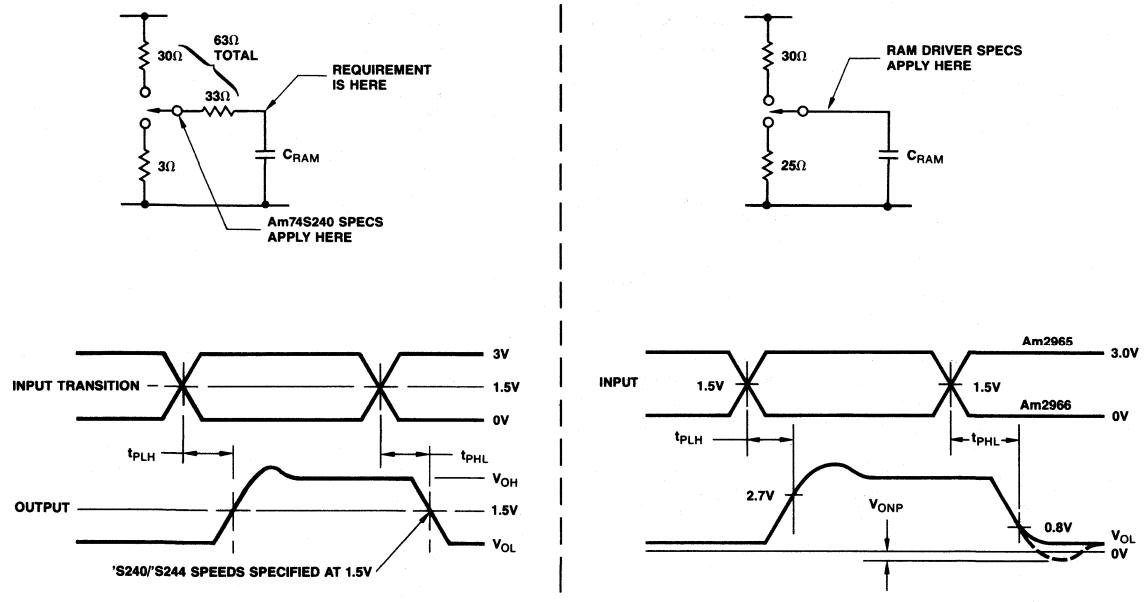
DESIGN ADVANTAGES OF THE Am2965/2966

Compared with Schottky parts such as the Am74S240 or Am74S244, which are used as RAM drivers today, the Am2965/66 RAM drivers offer more advantages than just a RAM driver having no external source resistor.

First, as Figure 8a shows, propagation delays for the Schottky Am74S240 or Am74S244 are measured at 1.5V, which is not where the RAM thresholds are. They are at 0.8V, 2.4V and 2.7V as shown in Figure 8b.

On the Am2965 and Am2966, the LOW-to-HIGH transition voltage propagation delay speeds are measured at 2.7V. Going from HIGH-to-LOW, speed is measured at 0.8V, which is where the actual RAM thresholds are.

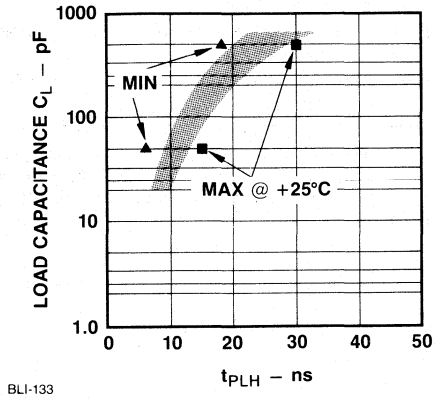
Propagation delays are specified differently, which also makes the Am2965/66 unique (Figure 9). Both minimum and maximum propagation delays are specified at 25°C and 5V. This enables the design engineer to do a worst-case design using both minimum and maximum numbers for the drivers to determine the skew between various drivers. A specified t_{PD} minimum of 50pF and an unusual maximum of 500pF provide a full range of capacitance specifications for both LOW-to-HIGH and HIGH-to-LOW transitions.



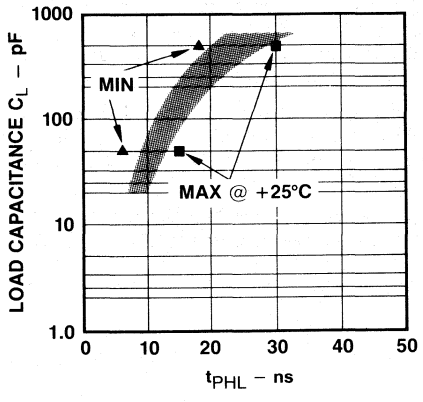
a) Am74S240 Common Approach

b) Ideal RAM Driver

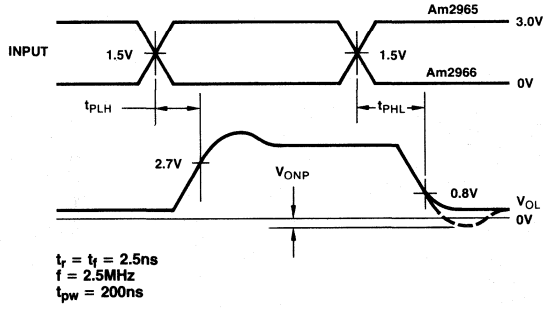
Figure 8. Am2965/66 • AmZ8165/66 Comparison with Am74S240



a) t_{PLH} for V_{OH} = 2.7 Volts vs. C_L



b) t_{PHL} for V_{OL} = 0.8 Volts vs. C_L



c) Output Drive Levels

Figure 9. RAM Driver Propagation Delays

Am2900
Controller Family Products Index

Design Aids

Am2900 HIGH PERFORMANCE CONTROLLER PRODUCTS

A BETTER WAY IS COMING

A new family of products from Advanced Micro Devices makes high-performance controller design a snap.

MICROPROGRAMMING: BEST FOR COMPUTERS, BEST FOR CONTROLLERS

Microprogramming, long the preferred approach for computer design, offers lots of advantages in controllers as well. The ease with which the functions of a microprogrammed controller can be enhanced and modified made the original 2900 Family popular for many disk, printer and communications controllers. The high speed operation of these microprogrammed systems makes it possible to handle higher data rates from newer peripheral devices and to build intelligence into the controller.

But the original 2900 products are architecturally oriented toward computers, with design features optimized for arithmetic functions and short sequences of microinstructions. MOS processors are good choices for many low speed applications, but when the demand for speed and inteligence goes up, they cannot keep pace. Controllers need something better.

Something better has been added to our 2900 Family: New products especially for controllers. Through 1981 and 1982, we'll be bringing you new products whose architectural features are optimized for bit manipulation, character handling, data communication and long, sophisticated microprograms.

FAST LIKE YOU'VE NEVER HAD

The central element of our new high speed controller family is the Am29116 – a 16-bit bipolar microprocessor. It's not a "bit slice" – it's a complete 16-bit processor, with ALU, working registers and status register. It can do computer instructions like add and subtract, but it's more than a computer. The Am29116 has instructions just for controllers – instructions not available in any other microprocessor. And it's fast – designed to execute all instructions in 100 nanoseconds, to keep up with the needs of today's high-performance peripherals and tomorrow's high speed communication channels.

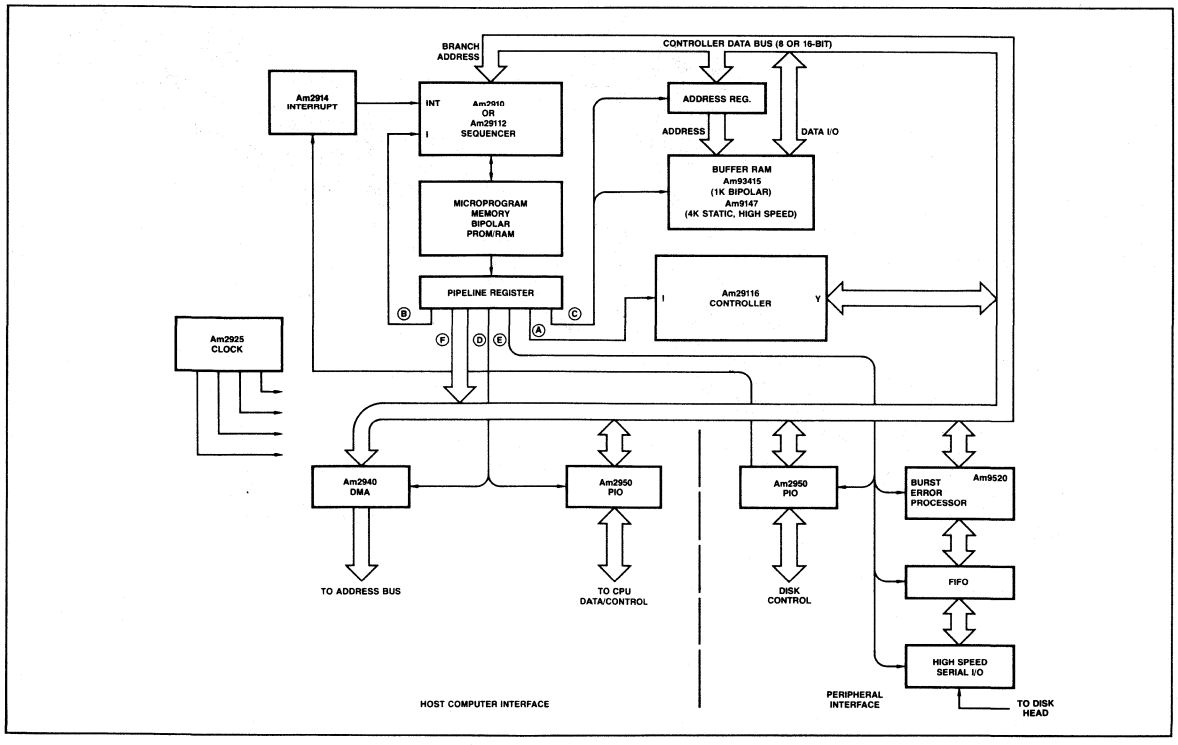
A WHOLE FAMILY OF FAST LSI CONTROLLER PARTS

There's more to our controller family than just the Am29116. A new sequencer, the Am29112, has been expressly designed for 10MHz microprogram control, with features like real-time interrupt servicing and deep subroutining. Rapid internal data transfer is handled by the Am2940 DMA Address Generator and by the Am2950 handshaking I/O port. The Am9520 Burst Error Processor will provide a solution for error correction on disk reads. Now, more than ever, the 2900 Family is the better solution for high data rate and highly intelligent control problems.

TYPICAL CONFIGURATION USING THE 2900 CONTROLLER FAMILY

A typical intelligent controller configuration is shown below. The basic controller consists of the Am29116, a microprogram control unit and a high speed buffer memory. Each microinstruction includes: A) a 16-bit instruction field to the Am29116, B) next-microinstruction selection bits, C) control for the buffer memory, D and E) control for the interface circuits and F) possibly an 8 or 16-bit data field.

Interface circuits like the Am2940 and Am2950 are used to provide DMA and to pass data between the controller and the host computer. Other circuits are used to interface to the peripheral. In this example, a disk interface is shown with a serial-parallel converter, a FIFO and a burst error processor. Controllers for other peripherals use identical hardware except for the peripheral interface itself.



Intelligent Controller Configuration

8

Am29112

Interruptable 8-Bit Microprogram Sequencer

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- **FAST**
  Designed to operate in 10MHz microprogrammed systems.
- **Expandable**
  One Am29112 directly addresses up to 256 words of microcode. Two Am29112's can directly address up to 64K words of microcode.
- **Interruptable**
  The Am29112 may be interrupted at the completion of a microcycle. Internal states are saved on the stack and the Am29112 branches automatically to the interrupt service routine.
- **Many Addressing Modes**
  Immediate, relative, and N-Way addressing are all possible with the Am29112.
- **31-Level Stack**
  On-chip 31-level stack is used for subroutines, interrupts and loops.
- **Single or Double Pipeline**
  The Am29112 may be configured for either single-level pipeline or double-level pipeline operation.
- **40-Pin Dual-in-Line Package**

Note: Am2900 High Performance Controller Products Family.

For information on using the Am29112 with other Am2900 High Performance Controller Products, refer to page 2-339.

BLOCK DIAGRAM

Am29116

16-Bit Bipolar Microprocessor

ADVANCE INFORMATION

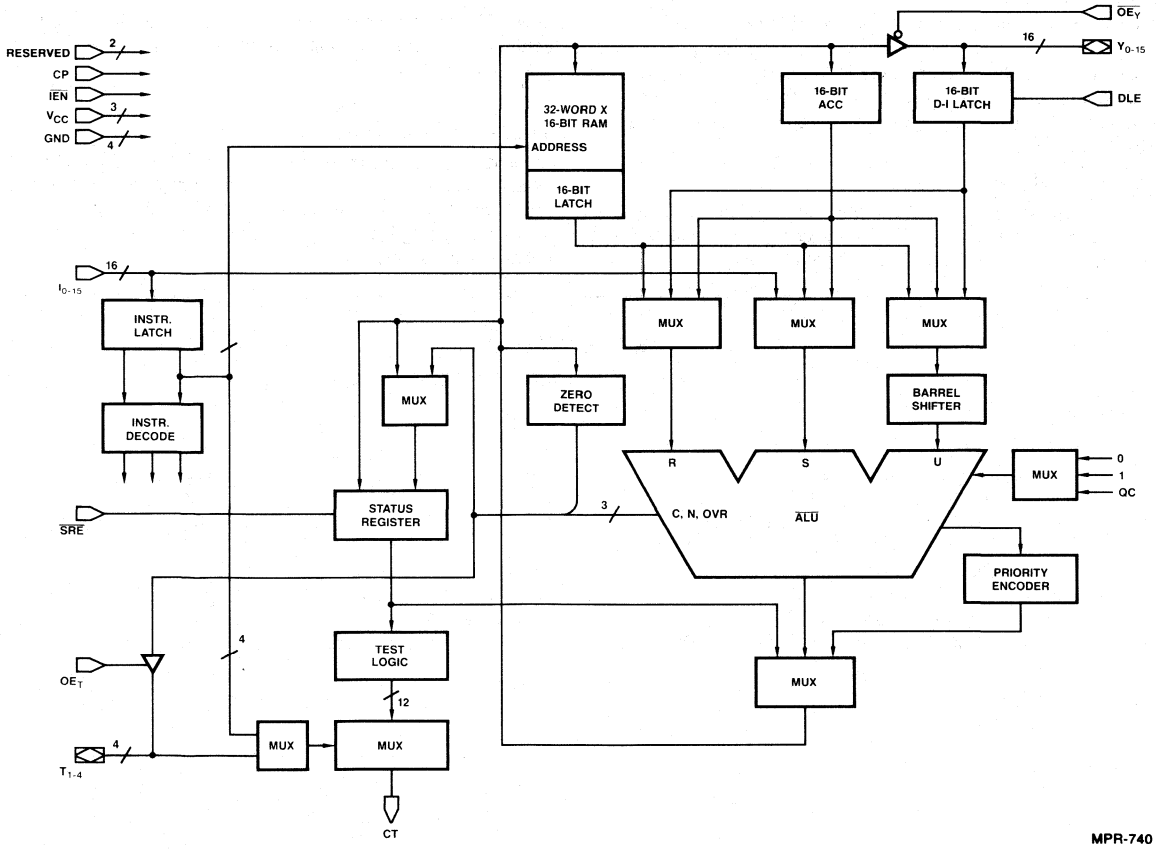
DISTINCTIVE CHARACTERISTICS

- **Designed for Controller Applications**
  Instruction set designed for high performance peripheral controllers, communications controllers, industrial controllers and digital modems . . . but general purpose, too. Excellent solution for applications requiring speed and bit-manipulation power.
- **FAST**
  Design objective of 100ns maximum microcycle time for all instructions. Allows a 10MHz clock rate.
- **Powerful Instruction Set**
  All instructions executable in single cycle on full 16-bit word or on 8-bit byte:
  - Add, Subtract
  - N-bit Rotate
  - Shift-Up/Shift-Down
  - Set-Bit/Reset-Bit
  - Add/Subtract 2^N
  - Rotate & Merge
  - Rotate & Compare
  - CRC Generation
  - Priority Encode
- **Powerful Data Manipulation**
  Full 16-bit data path. 32 registers on chip. Direct data input for immediate mode instructions.
- **52-Pin Hermetic DIP**

Note: Am2900 High Performance Controller Products Family.

Refer to the following page for more information on the Am2900 High Performance Controller Products Family.

BLOCK DIAGRAM



MPR-740

Am29116

A HIGH-PERFORMANCE 16-BIT BIPOLAR MICROPROCESSOR

INTRODUCTION

The Am29116 is a high-performance 16-bit bipolar microprocessor intended for use in microprogrammed systems, particularly peripheral controllers, although it is also suitable for use in communication controllers, industrial controllers and digital modems. The chip can also be used in microprogrammed processor applications. In adition to its complete arithmetic and logic instruction set, the Am29116 instruction set contains functions particularly useful in controller applications; bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation.

OUTSTANDING FEATURES

16-Bit Data Path

The Am29116 contains a 16-bit data path with full carry lookahead over all 16 bits in the ALU during arithmetic operation. In order to facilitate interfacing the device to other circuits, the Am29116 has the ability to execute all instructions in either the 16-bit word or 8-bit byte mode.

32 Working Registers

In order to provide adequate on-chip storage, the Am29116 contains 32 working registers arranged in a single port RAM architecture. With the use of an external multiplexer, it is possible to select separate read and write addresses for the same instruction. The device also contains a 16-bit Accumulator and a 16-bit Data Latch.

16-Bit Barrel Shifter

A 16-bit Barrel Shifter which can rotate an input up to 15 positions is also included in the device. Like the ALU, the barrel shifter can work in either the word or byte mode.

Status Register and Condition-Code Generator/Multiplexer

The Am29116 contains an 8-bit Status Register and a Condition-Code Generator/Multiplexer. The Status Register stores the four ALU status outputs, Z, C, N, OVR, as well as a Link bit for shifting and three user-definable Flag bits. The Condition-Code Generator/Multiplexer allows testing of 12 different test conditions. The output of the Condition-Code Generator/Multiplexer can be connected directly to the conditional-test input of a microprogram sequencer.

Immediate Instruction Capability

Immediate instructions can be executed by the Am29116. These are two-microcycle instructions. The first instruction contains information necessary to perform the instruction. The second instruction contains immediate data, which is entered via the 16 Instruction Inputs.

CRC Generation

The Am29116 has instructions which perform CRC, (Cyclic-Redundancy Check), calculations for any CRC polynomial of 16 bits or less.

Powerful Instruction Set

The instruction set of the Am29116 is very powerful. In addition to the normal single- and two-operand logical and arithmetic instructions, the Am29116 can also execute the following instructions in a single microcycle: rotate and merge, rotate and compare, and prioritize.

TABLE OF CONTENTS

ARCHITECTURE OF THE Am29116

The Am29116 is a high-performance, microprogrammable 16-bit bipolar microprocessor. This 52-pin device is designed internally with ECL (emitter-coupled logic) circuitry and has TTL to ECL and ECL to TTL converters on all inputs and outputs respectively.

All data paths within the device are 16-bits wide. As shown in the Block Diagram, the device consists of the following:

1. 32-Word by 16-Bit RAM
2. Accumulator
3. Data Latch
4. Barrel Shifter
5. ALU
6. Priority Encoder
7. Status Register
8. Condition-Code Generator/Multiplexer
9. Three-State Output Buffers
10. Instruction Latch and Decoder

The following paragraphs describe each of the blocks in detail.

32-Word by 16-Bit RAM

The 32-Word by 16-Bit RAM is a single-port RAM with a 16-bit latch at its output. The RAM latches are transparent when the clock input (CP) is HIGH and latched when the clock input is LOW. Data is written into the RAM while the clock is LOW if the IEN input is also LOW and if the instruction being executed defines the RAM as the destination of the operation. For byte instructions, only the lower eight RAM bits are written into; for word instructions, all 16 bits are written into. With the use of an external multiplexer on five of the instruction inputs, it is possible to select separate read and write addresses for the same instruction.

Accumulator

The 16-bit Accumulator is an edge-triggered register. The Accumulator accepts data on the LOW-to-HIGH transition of the clock input if the IEN input is LOW and if the instruction being executed defines the RAM as the destination of the operation. For byte instructions, only the lower eight bits of the Accumulator are written into; for word instructions, all 16 bits are written into.

Data Latch

The 16-bit Data Latch holds the data input to the Am29116 on the bi-directional Y-bus. The latch is transparent when the DLE input is HIGH and latched when the DLE input is LOW.

Barrel Shifter

A 16-bit Barrel Shifter is used as one of the ALU inputs. This permits rotating data from either the RAM, the Accumulator or the Data Latch up to 15 positions. In the word mode, the Barrel Shifter rotates a 16-bit word; in the byte mode, it rotates only the lower eight bits.

Arithmetic Logic Unit

The Am29116 contains a 16-bit ALU with full carry Look-Ahead across all 16 bits in the arithmetic mode. The ALU is capable of operating on either one, two or three operands, depending upon the instruction being executed. It has the ability to execute all conventional one and two operand operations, such as move, complement, two's complement, add, subtract, AND, NAND, OR, NOR, EXOR, and EX-NOR. In addition, the ALU can also execute three-operand instructions such as Rotate and Merge and Rotate and Compare with mask. The ALU can also utilize Immediate Data as coming from the instruction inputs as one of the operands. All ALU operations can be performed on either a word or byte basis, byte operations being performed on the lower eight bits only. The ALU can also perform CRC (Cyclic Redundancy Check) calculations using any polynominal of 16 bits or less. Only the word mode is meaningful for the CRC functions.

The ALU produces three status outputs, OVR (overflow), N (negative) and C (carry). The appropriate flags are generated at the byte or word level, depending upon whether the device is executing in the byte or word mode. The Z (zero) flag, although not generated by the ALU, detects zero at both the byte and word level.

The carry input to the ALU is generated by the Carry Multiplexer which can select an input of zero, one, or the stored carry bit from the Status Register, QC. Using QC as the carry input allows execution of multiprecision addition and subtraction.

Priority Encoder

The Priority Encoder produces a binary-weighted code to indicate the locations of the highest order ONE at its input. The input to the Priority Encoder is generated by the ALU which performs an AND operation on the operand to be prioritized and a mask. The mask determines which bit locations to eliminate from prioritization. In the word mode, if no bit is HIGH, the output is a binary zero. If bit 15 is HIGH, the output is a binary one. Bit 14 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 16 is produced.

In the byte mode, bits 8 thru 15 do not participate. If none of bits 0 thru 7 are HIGH, the output is a binary zero. If Bit 7 is HIGH a binary one is produced. Bit 6 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 8 is produced.

Status Register

The Status Register holds the 8-bit status word. With the Status-Register Enable, SRE, input LOW and the IEN input LOW, the Status Register is updated at the end of all instructions except NO-OP, Save-Status and Test-Status instructions. SRE going HIGH or IEN going HIGH inhibits the Status Register from changing.

The lower four bits of the Status Register contain the ALU status bits of (OVR) overflow, (N) negative, (C) carry (Z) zero. The upper four bits contain a Link bit and three user-definable status bits (Flag 3, Flag 2, Flag 1).

With SRE LOW and IEN LOW, the lower four status bits are updated after each instruction except those mentioned above, NO-OP, Save Status, Status Test and the Status Set/Reset instruction for the upper four bits. Under the same conditions, the upper four status bits are changed only during their respective Status Set/Reset instructions and during Status Load instruction in the word mode. The Link-Status bit is also updated after each shift instruction.

The Status Register can be loaded from the internal Y-bus, and can also be selected as a source for the internal Y-bus. When the Status Register is loaded in the word mode, all 8-bits are updated; in the byte mode, only the lower 4 bits (OVR, N, C, Z) are updated.

When the Status Register is selected as a source in the word mode, all eight bits are loaded into the lower byte of the destination; the upper byte of the destination is loaded with all zeros. In the byte mode, the Status Register again loads into the lower byte of the destination, but the upper byte remains unchanged. This Store and Load combination allows saving and restoring the Status Register for interrupt and subroutine processing. The four lower status bits (OVR, N, C, Z) can be read directly via the bidirectional T Bus. These four bits are available as outputs on the T_{1-4} outputs whenever OE_T is HIGH.

Condition-Code Generator/Multiplexer

The Condition-Code Generator/Multiplexer contains the logic necessary to develop the 12 condition-code test signals. The condition code multiplexer can select one of these test signals and place it on the CT output for use by the microprogram sequence. The multiplexer may be addressed in two different ways: One way is through the Test Instruction. This instruction specifies the test condition to be placed in the CT output, but does not allow an ALU operation at the same time. The second method uses the bidirectional T bus as an input. This requires extra microcode, but provides the ability to simultaneously test and execute.

Three-State Output Buffers

There are two sets of Three-State Output Buffers in the Am29116. One set controls the bidirectional, 16-bit Y-bus. These outputs are enabled by placing a LOW on the OEY input. A HIGH puts the Y outputs in the high-impedance state, allowing data to be input to the Data latch from an external source.

The second set of Three-State Output Buffers control the bidirectional 4-bit T bus and is enabled by placing a HIGH on the OE_T input. This allows storing the four internal ALU status bits (OVR, N, C, Z) externally. A LOW OE_T input forces the T outputs into the high-impedance state. External devices can then drive the T bus to select a test condition for the CT output.

Instruction Latch and Decoder

The 16-bit Instruction Latch is normally transparent to allow decoding of the Instruction Inputs by the Instruction Decoder into the internal control signals for the Am29116. All instructions except Immediate Instructions are executed in a single clock cycle.

Immediate instructions require two clock cycles for execution. During the first clock cycle, the Instruction Decoder recognizes that an Immediate Instruction is being specified and captures the data on the Instruction Inputs in the Instruction Latch. During the second clock cycle, the data on the Instruction Inputs is used as one of the operands for the function specified during the first clock cycle. At the end of the second clock cycle, the Instruction Latch is returned to its transparent state.

PIN DEFINITIONS

$\overline{OE_Y}$ Output Enable. When OE_Y is HIGH, the 16-bit Y outputs are disabled (high-impedance); when OE_Y is LOW, the 16-bit Y outputs are enabled (HIGH or LOW).

OE_T Output Enable. When OE_T is LOW, the 4-bit T outputs are disabled (high-impedance); when OE_T is HIGH, the 4-bit T outputs are enabled (HIGH or LOW).

I_0-I_{15} Sixteen Instruction Inputs. Used to select the operations to be performed in the Am29116. Also used as data inputs while performing Immediate instructions.

DLE Data Latch Enable. When DLE is HIGH, the 16-bit data latch is transparent and is latched when DLE is LOW.

Y_0-Y_{15} Sixteen Input/Output Lines. When OE_Y is HIGH, Y_0-Y_{15} are used as external data inputs which allow data to be directly loaded into the 16-bit data latch. Having OE_Y LOW allows the ALU data to be output on Y_0-Y_{15}.

$\overline{SRE}$ Status Register Enable. When SRE and IEN are both LOW, the Status Register is updated at the end of all instructions with the exception of NO-OP, Save Status, and Test Status. Having either SRE or IEN HIGH will inhibit the Status Register from changing.

CT Conditional Test. The condition code multiplexer selects one of the twelve condition code signals and places them on the CT output. A HIGH on the CT output indicates a passed condition and a LOW indicates a failed condition.

CP Clock Pulse. The clock input to the Am29116. The RAM latch is transparent when the clock is HIGH. When the clock goes LOW, the RAM output is latched. Data is written into the RAM during the low period of the clock provided IEN is LOW and if the instruction being executed designates the RAM as the destination of operation. The Accumulator and Status Register will accept data on the LOW-HIGH transition of the clock if IEN is also LOW. The instruction latch becomes transparent when it exits an immediate instruction mode during a LOW-HIGH transition of the clock.

T_1-T_4 Input/Output Pin. Under the control of OE_T, the four lower status bits OVR, N, C, Z become outputs on T_1-T_4 when OE_T goes HIGH. When OE_T is LOW, T_1-T_4 are used as inputs to generate the CT output.

$\overline{IEN}$ Instruction Enable. With IEN LOW, data can be written into the RAM when the clock is LOW and the Accumulator can accept data during the LOW-HIGH transition of the clock. Having IEN LOW, the Status Register can be updated when SRE is LOW. With IEN HIGH, the conditional test output, CT, is disabled as a function of the instruction inputs. IEN should be LOW for the first half of the first cycle of an Immediate instruction.

INSTRUCTION SET

The Am29116 Instruction Set can be divided into 11 types of instructions. These are:

- Single Operand
- Two Operand
- Single Bit Shift
- Rotate n Bits
- Bit Oriented
- Rotate and Merge
- Rotate and Compare
- Prioritize
- Cyclic Redundancy Check
- No-op
- Status

The instruction set of the Am29116 is very powerful. In addition to the normal single and two operand logical and arithmetic instructions, the Am29116 instruction set contains functions particularly useful in controller applications; bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation. The complex instructions like rotate and merge, rotate and compare, and prioritize are executed in a single microcycle. Three data types are supported by the Am29116.

- Bit
- Byte
- Word (16-Bit)

In the byte mode data is written into the lower half of the word and the upper half is undefined. The special case is when the status register is specified as the destination. In the byte mode the LSH (OVR, N, C, Z) of the status register is updated and in the word mode all eight bits of the status register are updated. The status register does not change for save status and test status instructions. In the test status instructions CT output has the result and the Y-bus is don't care.

The following pages describe each of the instruction types in detail. Throughout the description OE_Y is assumed to be LOW allowing ALU outputs on the Y-bus.

SINGLE OPERAND INSTRUCTIONS (Figure 1)

The Single Operand instructions contain four indicators; byte or word mode, opcode, source and destination. They are further subdivided into two types. The first type uses the RAM as a source and /or destination, and the second type does not use the RAM as a source or destination. Both types have different instruction formats as shown in Table I, operand combinations. Under the control of the instruction inputs, the desired function is performed on the source and the result is either stored in the specified destination or placed on the Y-bus or both. The least significant four bits of the status register (OVR, N, C, Z) are effected by the function performed in this category. The most significant bits of status register (FLAG1, FLAG2, FLAG3, LINK) are not effected.

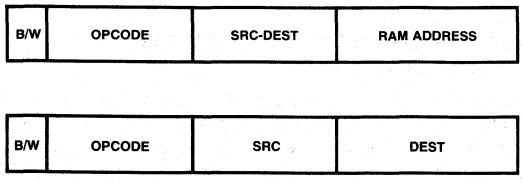


Figure 1. Single Operand Instructions

TWO OPERAND INSTRUCTIONS (Figure 2)

The Two Operand Instructions contain five indicators; byte or word mode, opcode, R source, S source, and destination. It is further subdivided into two types. The first type uses the RAM as one of the sources and/or destination and the second type does not use RAM as source or destination. Under the control of instruction inputs, the desired function is performed on the specified sources and the result is stored in the specified destination and/or placed on the Y-bus. The least significant four bits of the status register (OVR, N, C, Z) are affected by the arithmetic functions performed and only the N and Z bits are affected by the logical functions performed. The OVR and C bits of the status register are forced to ZERO for logical functions.

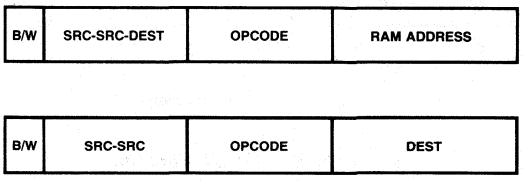


Figure 2. Two Operand Instructions

SINGLE BIT SHIFT INSTRUCTIONS (Figures 3, 4, 5)

The Single Bit Shift instructions contain four indicators; byte or word mode, direction and shift linkage, source and destination. It is further subdivided into two types. The first type uses the RAM as the source and/or destination and the second type does not use RAM as source or destination. Under the control of instruction inputs, the desired shift function is performed on the specified source and the result is stored in the specified destination and/or placed on the Y-bus. A shift linkage and direction indicator defines the direction of the shift (up and down) as well as what will be shifted into the vacant bit. On a shift-up instruction, the LSB may be loaded with ZERO, ONE, or the Link-Status bit (QLINK). The MSB is loaded into the Link-Status Bit as shown in Figure 4. On a shift-down instruction, the MSB may be loaded with ZERO, ONE, the contents of the Status Carry flip-flop, (QC), the Exclusive-OR of the Negative-Status bit and the Overflow-Status bit (QNOQOVR) or the Link-Status bit. The LSB is loaded into the Link-Status bit as shown in Figure 5. The N and Z bits of the status register are affected but the OVR and C bits are forced to ZERO.

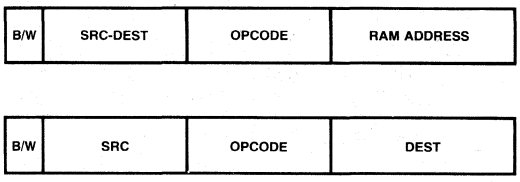


Figure 3. Single Bit Shift Instructions

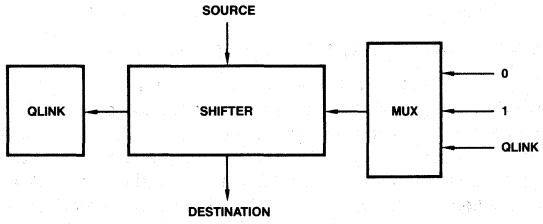


Figure 4. Shift Up Function

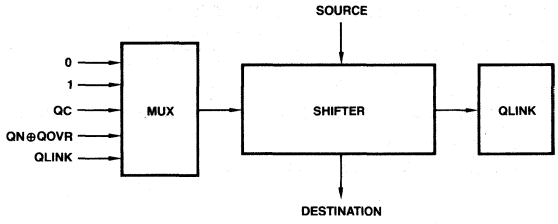


Figure 5. Shift Down Function

ROTATE BY n BITS INSTRUCTIONS (Figures 6, 7)

The Rotate by n bits instructions contain four indicators; byte or word mode, source, destination and the number of places the source is to be rotated. It is further subdivided into two types. The first type uses the RAM as a source and/or a destination and the second type does not use the RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in the table. Under the control of the instruction inputs, the n indicator specifies the number of bit positions the source is to be rotated up (0 to 15) and the result is stored in the specified destination and/or placed on the Y-bus. An example of this instruction is given in Figure 6. In the word mode, all 16-bits are rotated up while in the byte mode, only lower 8-bits (0 to 7) are rotated up. In the word mode, a rotate up by n bits is equivalent to a rotate down by (16-n) bits. Similarly, in the byte mode a rotate by n bits is equivalent to a rotate down by (8-n) bits. The N and Z bits of the status register are affected and OVR and C bits are forced to ZERO.

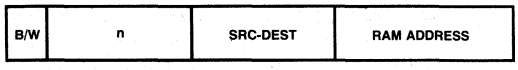


Figure 6. Rotate by 17 Bits

EXAMPLE:	N =, Word Mode			
Source	0001	0011	0111	1111
Destination	0011	0111	1111	0001
EXAMPLE:	N = 4, Byte Mode			
Source	0001	0000	0111	1111
Destination			1111	0111

Figure 7. Rotate by n Example

BIT ORIENTED INSTRUCTIONS

The Bit Oriented instructions contain four indicators; byte or word mode, operation, source/destination, and the address of the bit to be operated on. It is further subdivided into two types. The first type uses the RAM as both source and destination. The second type does not use the RAM as a source or a destination. Under the control of instruction inputs, the desired function is performed on the specified source and the result is stored in the specified destination and/or placed on the Y-bus. The operations which can be performed are: set bit n which forces the n^{th} bit to a ONE leaving other bits unchanged; reset bit n which forces the n^{th} bit to ZERO leaving the other bits unchanged; test bit n, which sets the ZERO Status Bit depending on the state of bit n leaving all the bit unchanged; load 2^n, which loads ONE in bit position n and ZERO in all other bit positions; load 2^n, which loads ZERO in bit position n and ONE in all other bit positions; increment by 2^n, which adds 2^n to the operand; and decrement by 2^n, which subtracts 2^n from the operand. For all the Set, Reset and Test instructions, the N and Z bits are affected and OVR and C bits of the status register are forced to ZERO. For all the load and arithmetic instructions the LSH (OVR, C, N, Z bits) of the status register is affected.

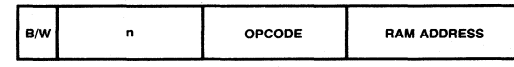


Figure 8. Bit Oriented Instruction

ROTATE AND MERGE INSTRUCTIONS (Figures 9, 10, 11)

The Rotate and Merge instructions contain five indicators; byte and word mode, rotated source, non-rotated source/destination, mask and the number of bit positions the rotated source is to be rotated. The function performed by the Rotate and Merge instruction is illustrated in Figure 10. The rotated source, U, is rotated up by the Barrel Shifter n places. The mask input then selects, on a bit-by-bit basis, the rotated U input or R input. A ZERO in bit i of the mask will select the i^{th} bit of the R input as the i^{th} output bit, while ONE in bit i will select the i^{th} rotated U input as the output bit. The output word is stored in the non-rotated operand location. The N and Z bits are effected. The OVR and C bits of the status register are forced to ZERO. An example of this instruction is given in Figure 11.

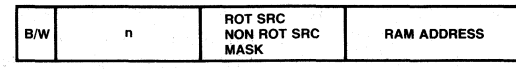


Figure 9. Rotate and Merge Instruction

ROTATE AND COMPARE INSTRUCTIONS (Figures 12, 13, 14)

The Rotate and Compare instructions contain five indicators; byte or word mode, rotated source, non-rotated source, mask, and number of bit positions the rotated source is to be rotated up. The function performed by the Rotate and Compare instruction is illustrated in Figure 13. The rotated operand is rotated by the Barrel Shifter n places. The mask is inverted and ANDed on a bit-by-bit basis with the output of the Barrel Shifter and R input.

Thus, a ONE in the mask input eliminates that bit from comparison. A ZERO allows the comparison. If the comparison passes, the Zero flag is set. If it fails, the Zero flag is reset. The N and Z bit are affected. The OVR and C bits of the status register are forced to ZERO. An example of this instruction is given in Figure 14.

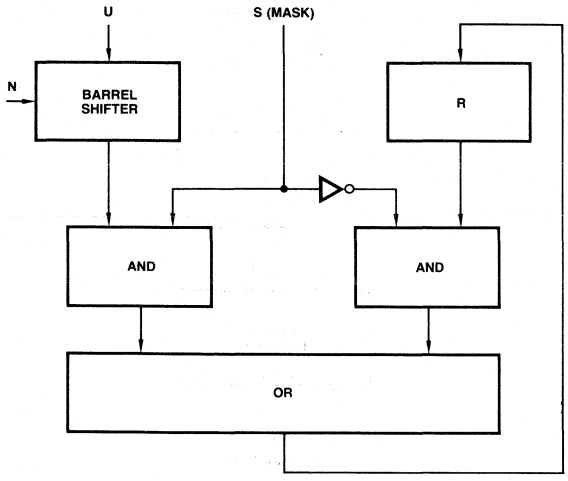


Figure 10. Rotate and Merge Function

EXAMPLE:	N = 4, Word Mode			
U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	1010	1010	1010	1010
Mask (S)	0000	1111	0000	1111
Destination	1010	0101	1010	0011

Figure 11. Rotate and Merge Example

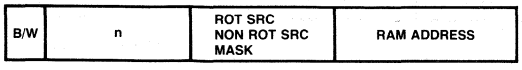


Figure 12. Rotate and Compare Instruction

PRIORITIZE INSTRUCTION (Figures 15, 16, 17)

The prioritize instructions contain four indicators; byte or word mode, R source, mask source (S) and destination. It is further subdivided into two types. The first types use the RAM as the source and destination as shown in Figure 15. The second type does not use the RAM as a source or a destination. The function performed by the Prioritize instruction is illustrated in Figure 16. The R operand is ANDed with the complement of the Mask operand. A ZERO in the Mask operand allows the corresponding bit in the R operand to participate in the priority encoding function.

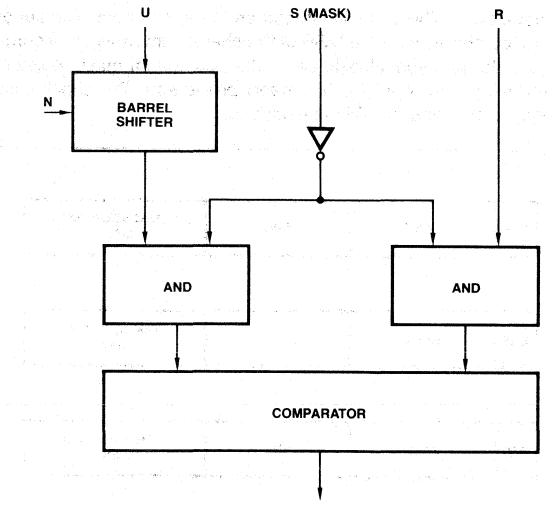


Figure 13. Rotate and Compare Function

EXAMPLE:	N =, Word Mode			
U	0011	0001	0101	0110
U Rotated	0001	0101	0110	0011
R	0001	0101	1111	0000
Mask (S)	0000	0000	1111	1111
Z (status)	= 1			

Figure 14. Rotate and Compare Examples

A ONE in the Mask operand forces the corresponding bit in the R operand to a ZERO, eliminating it from participation in the priority encoding function. The Priority Encoder accepts a 16-bit input and produces a 5-bit binary-weighted code indicating the bit position of the highest priority active bit. If none of the inputs are active, the output is ZERO. In the word mode, if input bit 15 is active, the output is 1, etc. Figure 17 lists the output as a function of the highest-priority active-bit position in both the word and byte mode.

CRC INSTRUCTION (Figures 18, 19)

The CRC (Cyclic Redundancy Check) instructions contain one indicator: the address of the RAM register to use as check sum register. The CRC instruction provides a method for generation of the check bits in a CRC calculation. Two CRC instructions are provided – CRC Forward and CRC Reverse. The reason for providing two instructions is that the CRC standards do not specify which data bit must be transmitted first, the LSB or the MSB, but they do specify which check bit must be transmitted first. Figure 17 illustrates the method used to generate these check bits for the CRC Forward function and Figure 18 illustrates method used for the CRC Reverse function. The ACC serves as a polynomial mask to define the generating polynomial while the RAM register holds the partial result and eventually the calculated

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Check Sum. The Link-Bit is used as the serial input. The serial input combines with the MSB of the check-sum register, according to the polynomial defined by the polynomial mask register. When the last input bit has been processed, the check-sum register contains the CRC check bits.

NO/OP INSTRUCTION

The NO-OP instruction has a fixed 16-bit code. This instruction does not change any internal registers in the Am29116. It preserves the status register, RAM register and the ACC register.

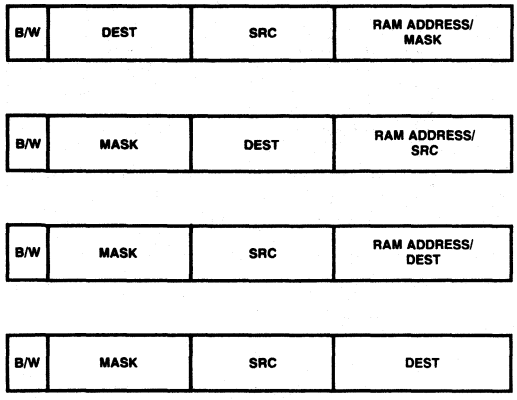

Figure 15. Prioritize Instruction

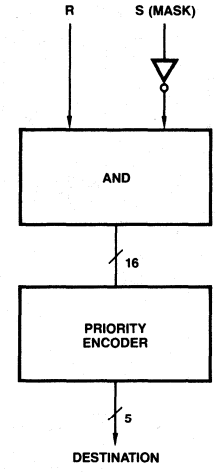

Figure 16. Prioritize Function

WORD MODE		WORD MODE*	
Highest-Priority Active Bit	Encoder Output	Highest-Priority Active Bit	Encoder Output
None	0	None	0
15	1	7	1
14	2	6	2
.	.	.	.
.	.	.	.
.	.	.	.
1	15	1	7
0	16	0	8

*Bits 8-15 do not participate.

Figure 17. Priority Encoding

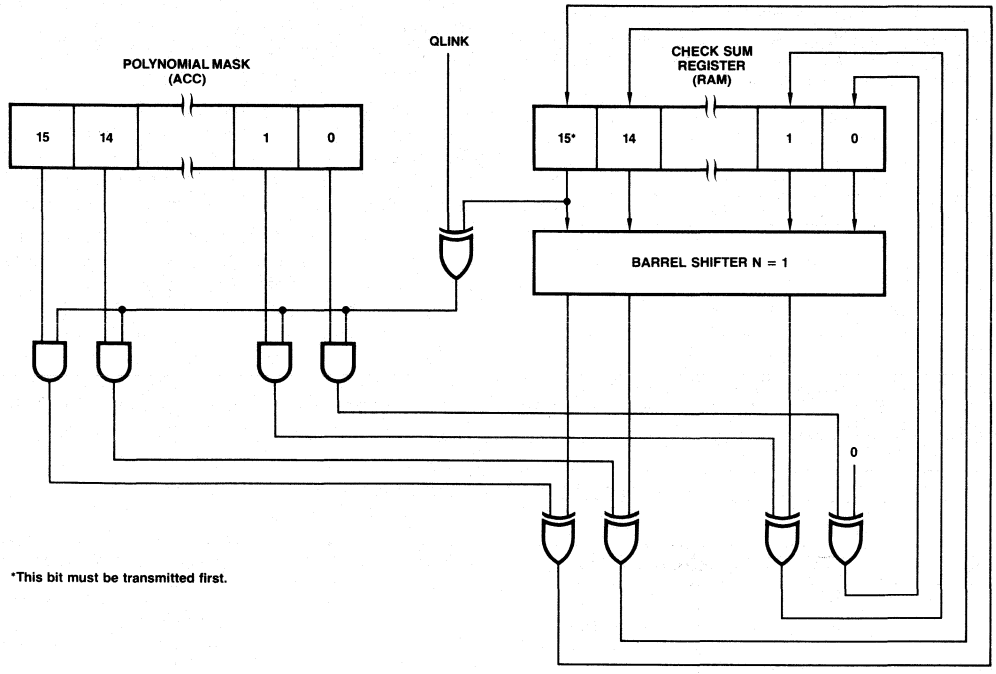

Figure 18. CRC Forward Function

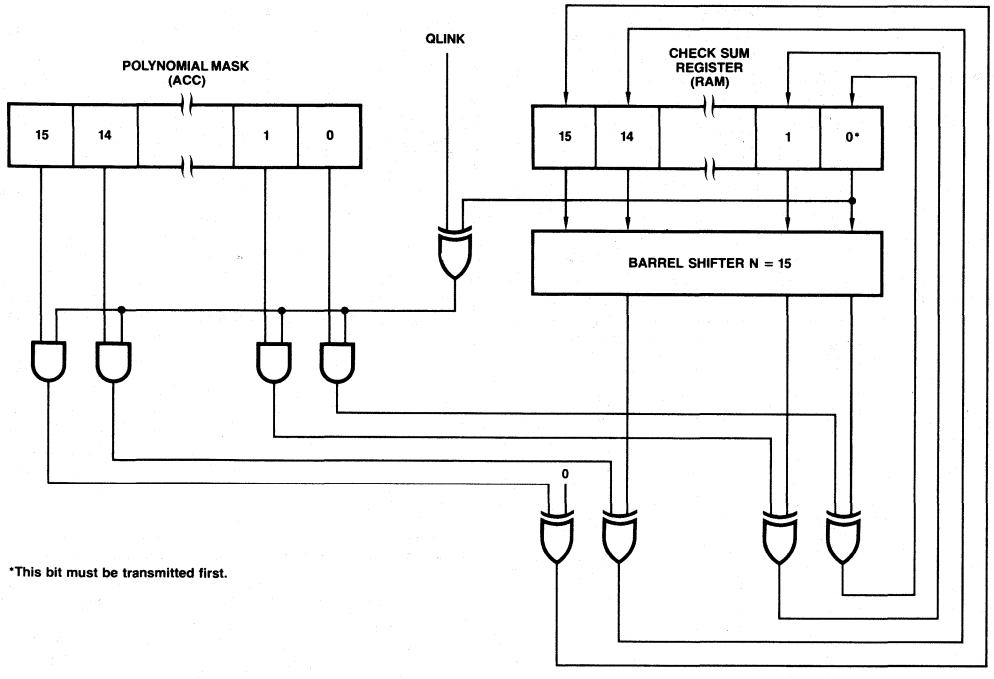

Figure 19. CRC Reverse Function

STATUS INSTRUCTIONS

Status Instructions – The Set Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the Status Register (Figure 20), are to be set (forced to a ONE).

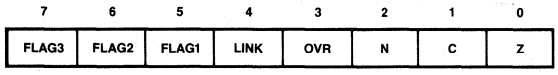

Figure 20. Status Byte

The *Reset Status Instruction* contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register are to be reset (forced to ZERO).

The *Store Status Instruction* contains two indicators, a byte/word and a second indicator that specifies the destination of the Status Register. The Store Status Instruction allows the status of the processor to be saved and restored later, which is an especially useful function for interrupt handling.

The *Load Status Instruction* contains two indicators. The indicators specify the byte or word mode and the source for the Status Register. In the byte mode only, the lower 4-bits (QC, QN, QZ, QOVR) are loaded from the source. In the word mode, all 8-bits of the Status Register are loaded from the source.

The *Test Status Instructions* contain a single indicator which specifies which one of the 12 possible test conditions are to be placed on the Conditional-Test output. Besides the eight bits in the status register (QZ, QC, QN, QOVR, QLINK, QFLAG1, QFLAG2, and QFLAG3), four logical functions (QNOQOVR), (QNOQOVR) + QZ, QZ + QC and LOW may also be selected. These functions are useful in testing results of 2's complement and unsigned number arithmetic operations. The Status Register may also be tested via the bidirectional T bus.

TABLE I. OPERAND COMBINATIONS

Instruction Type	Operand Combinations (Note 1)		
Single Operand	Source (R/S)		Destination
	RAM (Note 2) ACC D D (0E) D (SE) I 0		RAM ACC Y Bus Status ACC & Status
Two-Operand	Source (R)	Source (S)	Destination
	RAM RAM D D ACC D	ACC I RAM ACC I I	RAM ACC Y Bus
Single Bit Shift	Source (U)		Destination
	RAM ACC ACC D D D		RAM ACC Y Bus RAM ACC Y Bus
Rotate n Bits	Source (U)		Destination
	RAM ACC D		RAM ACC Y Bus
Bit Oriented	Source (R/S)		Destination
	RAM ACC D		RAM ACC Y Bus

Instruction Type	Operand Combinations (Note 1)		
Rotate & Merge	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
	D D D D ACC RAM	I RAM I ACC I I	ACC ACC RAM RAM RAM ACC
Rotate & Compare	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
	D D D RAM	I I ACC I	ACC RAM RAM ACC
Prioritize (Note 3)	Source (R)	Mask (S)	Destination
	RAM ACC D	RAM ACC I 0	RAM ACC Y Bus
Cyclic Redundancy Check	Data In		Destination
	QLINK		RAM

Notes:
1. When there is no dividing line between the R & S OPERAND or SOURCE and DESTINATION, the two must be used as a given pair. But where there exists such a separation, any combination of them is possible.
2. In the SINGLE OPERAND INSTRUCTION, RAM cannot be used when both ACC and STATUS are designated as a DESTINATION.
3. In the PRIORITIZE INSTRUCTIONS, OPERAND and MASK must be different sources.

TABLE 1. OPERAND COMBINATIONS (Cont.)

Instruction Type	Operand Combinations (Note 1)		
No Operation			
SET RESET STATUS	Bits Affected		
	OVR, N, C, Z LINK FLAG 1 FLAG 2 FLAG 3		
Store Status	Source		Destination
	Status		RAM ACC Y Bus
Status Load	Source (R)	Source (S)	Destination
	D ACC D	ACC I I	Status Status & ACC
	Test Condition (CT)		
Test Status	(N0OVR) + Z N0OVR Z OVR LOW C Z + C N LINK FLAG1 FLAG2 FLAG3		

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Am29116
INSTRUCTION MNEMONICS

INSTRUCTION TYPE

SOR	Single Operand RAM
SONR	Single Operand Non-RAM
TOR1	Two Operand RAM (Quad 0)
TOR2	Two Operand RAM (Quad 2)
TONR	Two Operand Non-RAM
SHFTR	Single Bit Shift RAM
SHFTNR	Single Bit Shift Non-RAM
ROTR1	Rotate n Bits RAM (Quad 0)
ROTR2	Rotate n Bits RAM (Quad 1)
ROTNR	Rotate n Bits Non-RAM
BOR1	Bit Oriented RAM (Quad 3)
BOR2	Bit Oriented RAM (Quad 2)
BONR	Bit Oriented Non-RAM
ROTM	Rotate and Merge
ROTC	Rotate and Compare
PRTR1	Prioritize RAM; Type 1
PRTR2	Prioritize RAM; Type 2
PRTR3	Prioritize RAM; Type 3
PRTNR	Prioritize Non-RAM
CRCF	Cyclic Redundancy Check Forward
CRCR	Cyclic Redundancy Check Reverse
NOOP	No Operation
SETST	Set Status
RSTST	Reset Status
SVSTR	Save Status RAM
SVSTNR	Save Status Non-RAM
TEST	Test Status

SOURCE AND DESTINATION

Single Operand

SORA	Single Operand RAM to ACC
SORY	Single Operand RAM to Y Bus
SORS	Single Operand RAM to Status
SOAR	Single Operand ACC to RAM
SODR	Single Operand D to RAM
SOIR	Single Operand I to RAM
SOZR	Single Operand 0 to RAM
SOZER	Single Operand D (0E) to RAM
SOSER	Single Operand D (SE) to RAM
SORR	Single Operand RAM to RAM
SOA	Single Operand ACC
SOD	Single Operand D
SOI	Single Operand I
SOZ	Single Operand 0
SOZE	Single Operand D (0E)
SOSE	Single Operand D (SE)
NRY	Non-RAM Y Bus
NRA	Non-RAM ACC
NRS	Non-RAM STATUS
NRAS	Non-RAM ACC, STATUS

Two Operand

TORAA	Two Operand RAM, ACC to ACC
TORIA	Two Operand RAM, I to ACC
TODRA	Two Operand D, RAM to ACC
TORAY	Two Operand RAM, ACC to Y Bus
TORIY	Two Operand RAM, I to Y Bus
TODRY	Two Operand D, RAM to Y Bus
TORAR	Two Operand RAM, ACC to RAM
TORIR	Two Operand RAM, I to RAM
TODRR	Two Operand D, RAM to RAM
TODAR	Two Operand D, ACC to RAM
TOAIR	Two Operand ACC, I to RAM
TODIR	Two Operand D, I to RAM
TODA	Two Operand D, ACC
TOAI	Two Operand ACC, I
TODI	Two Operand D, I

Single Bit Shift

SHRR	Shift RAM, Store in RAM
SHDR	Shift D, Store in RAM
SHA	Shift ACC
SHD	Shift D

Rotate n Bits

RTRA	Rotate RAM, Store in ACC
RTRY	Rotate RAM, Place on Y Bus
RTRR	Rotate RAM, Store in RAM
RTAR	Rotate ACC, Store in RAM
RTDR	Rotate D, Store in RAM
RTDY	Rotate D, Place on Y Bus
RTDA	Rotate D, Store in ACC
RTAY	Rotate ACC, Place on Y Bus
RTAA	Rotate ACC, Store in ACC

Rotate and Merge

MDAI	Merge Disjoint Bits of D and ACC Using I as Mask and Store in ACC
MDAR	Merge Disjoint Bits of D and ACC Using RAM as Mask and Store in ACC
MDRI	Merge Disjoint Bits of D and RAM Using I as Mask and Store in RAM
MDRA	Merge Disjoint Bits of D and RAM Using ACC as Mask and Store in RAM
MARI	Merge Disjoint Bits of ACC and RAM Using I as Mask and Store in RAM
MRAI	Merge Disjoint Bits of RAM and ACC Using I as Mask and Store in ACC

Rotate and Compare

CDAI	Compare Unmasked Bits of D and ACC Using I as Mask
CDRI	Compare Unmasked Bits of D and RAM Using I as Mask
CDRA	Compare Unmasked Bits of D and RAM Using ACC as Mask
CRAI	Compare Unmasked Bits of RAM and ACC Using I as Mask

Prioritize

PR1A	ACC as Destination for Prioritize Type 1
PR1Y	Y Bus as Destination for Prioritize Type 1
PR1R	RAM as Destination for Prioritize Type 1
PRT1A	ACC as Source for Prioritize Type 1
PR1D	D as Source for Prioritize Type 1
PR2A	ACC as Destination for Prioritize Type 2
PR2Y	Y Bus as Destination for Prioritize Type 2
PR3R	RAM as Source for Prioritize Type 3
PR3A	ACC as Source for Prioritize Type 3
PR3D	D as Source for Prioritize Type 3
PRTA	ACC as Source for Prioritize Type Non-RAM
PRTD	D as Source for Prioritize Type Non-RAM
PRA	ACC as Mask for Prioritize Type 2, 3, and Non-RAM
PRZ	Mask Equal to Zero for Prioritize Type 2, 3, and Non-RAM
PRI	I as Mask for Prioritize Type 2, 3, and Non-RAM

OPCODE

Addition

ADD	Add Without Carry
ADDC	Add with Carry
A2NA	Add 2^n to ACC
A2NR	Add 2^n to RAM
A2NDY	Add 2^n to D, Place on Y Bus

Subtraction

SUBR	Subtract R from S without Carry
SUBRC	Subtract R from S with Carry
SUBS	Subtract S from R without Carry
SUBSC	Subtract S from R with Carry
S2NR	Subtract 2^n from RAM
S2NA	Subtract 2^n from ACC
S2NDY	Subtract 2^n from D, Place on Y Bus

Logical Operations

AND	Boolean AND
NAND	Boolean NAND
EXOR	Boolean EXOR
NOR	Boolean NOR
OR	Boolean OR
EXNOR	Boolean EXNOR

SHIFTS

SHUPZ	Shift Up Towards MSB with 0 Insert
SHUP1	Shift Up Towards MSB with 1 Insert
SHUPL	Shift Up Towards MSB with Link Insert
SHDNZ	Shift Down Towards LSB with 0 Insert
SHDN1	Shift Down Towards LSB with 1 Insert
SHDNL	Shift Down Towards LSB with Link Insert
SHDNC	Shift Down Towards LSB with Carry Insert
SHDNOV	Shift Down Towards LSB with Sign EXOR Overflow Insert

Loads

LD2NR	Load 2^n into RAM
LDC2NR	Load 2^n into RAM
LD2NA	Load 2^n into ACC
LDC2NA	Load 2^n into ACC
LD2NY	Place 2^n on Y Bus
LDC2NY	Place 2^n on Y Bus

Bit Oriented

SETNR	Set RAM, Bit n
SETNA	Set ACC, Bit n
SETND	Set D, Bit n
SONCZ	Set OVR, N, C, Z, in Status Register
SL	Set Link Bit in Status Register
SF1	Set FLAG1 Bit in Status Register
SF2	Set FLAG2 Bit in Status Register
SF3	Set FLAG3 Bit in Status Register
RSTNR	Reset RAM, Bit n
RSTNA	Reset ACC, Bit n
RSTND	Reset D, Bit n
RONCZ	Reset OVR, N, C, Z, in Status Register
RL	Reset Link Bit in Status Register
RF1	Reset FLAG1 Bit in Status Register
RF2	Reset FLAG2 Bit in Status Register
RF3	Reset FLAG3 Bit in Status Register
TSTNR	Test RAM, Bit n
TSTNA	Test ACC, Bit n
TSTND	Test D, Bit n

Arithmetic Operations

MOVE	Move and Update Status
COMP	Complement (1's Complement)
INC	Increment
NEG	Two's Complement

Conditional Test

TNOZ	Test (N ⊕ OVR) + Z
TNO	Test N ⊕ OVR
TZ	Test Zero Bit
TOVR	Test Overflow Bit
TLOW	Test for LOW
TC	Test Carry Bit
TZC	Test Z + C
TN	Test Negative Bit
TL	Test Link Bit
TF1	Test FLAG1 Bit
TF2	Test FLAG2 Bit
TF3	Test FLAG3 Bit

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Am29116 APPLICATIONS

The intended primary applications for the Am29116 are high-performance peripheral controllers. Figure 14 shows a typical system configuration for a Host Computer, Memory and Peripheral Controller. The interface between the three units is via three buses; the data bus (D1), the address bus (A1) and the control bus (C1). The interface between the Peripheral Controller and the Peripheral Devices is via a data bus (D2) which may be either serial or parallel, and a control bus (C2). Information on the control buses consists of status, command and timing signals.

A typical implementation of the Peripheral Controller is shown in Figure 15. The bidirectional interface to the D1 data bus is via two Am2950 8-Bit Parallel I/O Ports; two Am2940 8-bit DMA Address Generators drive the A1 bus and another Am2950 interfaces to the bidirectional C1 bus. The interface to the serial D2 bus is via a parallel-to-serial and a serial-to-parallel converter, and the bidirectional interface to the C2 bus is via two Am2950s. The interface between these bus-interface units and the Am29116 is a 16-bit bidirectional bus which connects to the Y_{0-15} outputs of the Am29116.

Also connected to this bus is a 256-word RAM for temporary data storage and a 12-bit interface (1-1/2 Am2920s) to the D_{0-11} inputs of the Am2910 Microprogram Sequencer. The bus-control and clock-enable signals for these devices are generated by the Pipeline Register at the output of the Microprogram Memory.

The Am29116, Am2910 and the Microprogram Memory perform the data manipulation and routing; command and status testing and generation; and timing-signal generation functions. The implementation illustrated in Figure 15 minimizes the amount of hardware necessary to implement a controller. This is accomplished by A) sharing the Instruction-Inputs to the Am29116 with the D_{0-11} inputs to the Am2910, B) generating all necessary test conditions within the Am29116 which allow connecting the CT output of the Am29116 directly to the $\overline{CC}$ inputs of the Am2910, C) by generating the CT output via the Instruction Inputs, D) performing all the necessary status manipulations within the Am29116, E) using the same RAM address for reading and writing and F) running the controller at a fixed clock rate.

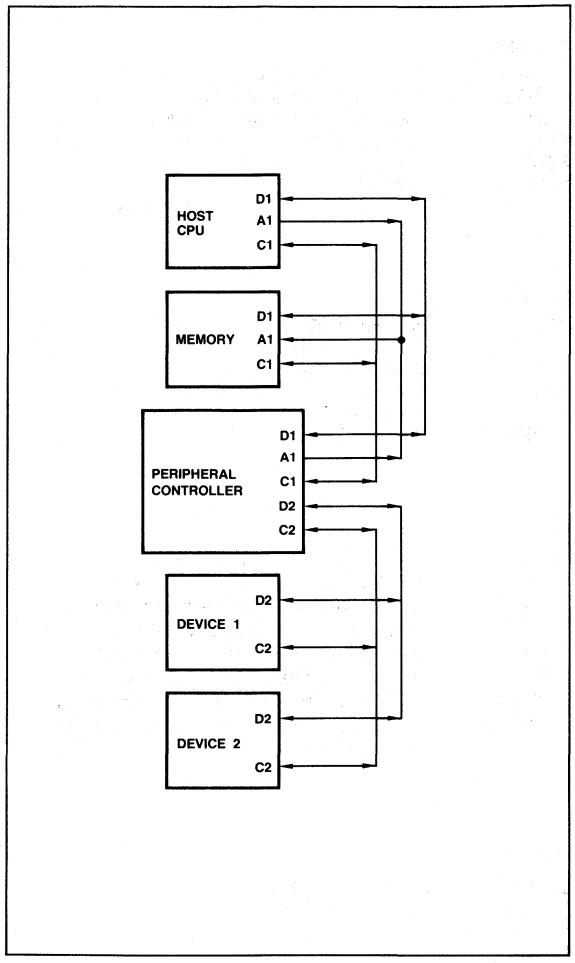


Figure 21. Typical System Configuration

Although the implementation shown in Figure 15 minimizes the amount of required hardware, it does limit the throughput of the controller. The architecture shown in Figure 16 uses the same bus interface circuits but maximizes the throughput of the controller at the expense of additional hardware. In this implementation, the Instruction Inputs of the Am29116 and the D_{0-11} inputs of the Am2910 are driven from separate microcode bits; this allows simultaneous instruction execution in the Am29116 and direct jumping in the Am2910. The multiplexer at the $\overline{CC}$ input of the Am2910 allows testing of conditions without loading the signals into the Am29116. Four additional bits of microcode drive the T_{1-4} inputs of the Am29116; this allows simultaneous conditional testing and execution of an instruction in the Am29116. The Am2904 can be loaded with the four ALU arithmetic status bits (Z, C, N, OVR). The flexibility of the Am2904, such as selective loading of status bits, reduces the number of cycles necessary to perform status manipulation. By adding five additional microcode bits and a multiplexer at the I_{0-4} inputs of the Am29116, separate RAM source and destination addresses can be used in the same microcycle; for example, the contents of RAM address 3 can be added to the contents of the Accumulator and the results can be stored in RAM address 27. The Am2925 System-Clock Generator and Driver, in addition to providing the basic oscillator and clock driver functions, provides the ability to dynamically alter the length of the microcycle; this facilitates interfacing the Am29116 to slower bus interface and peripheral circuits.

Figures 15 and 16 are intended to show the two extremes of minimizing hardware versus maximizing throughput.

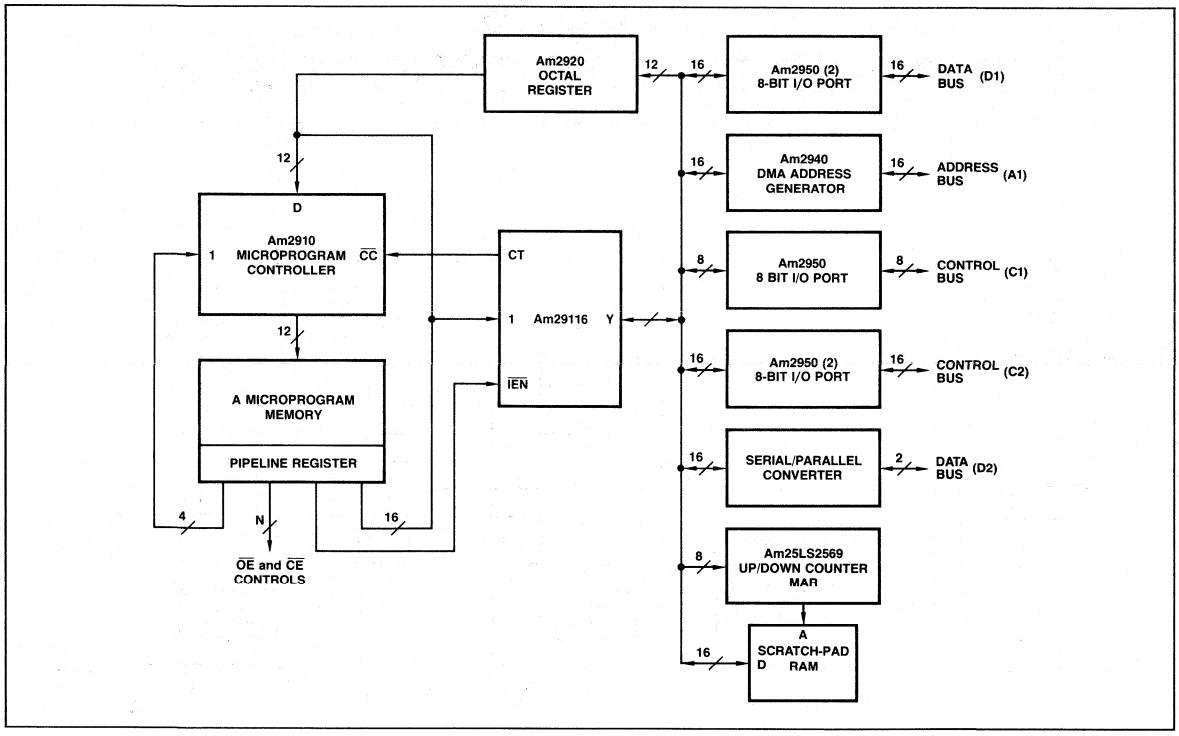


Figure 22. Peripheral Controller, Minimum Parts Configuration

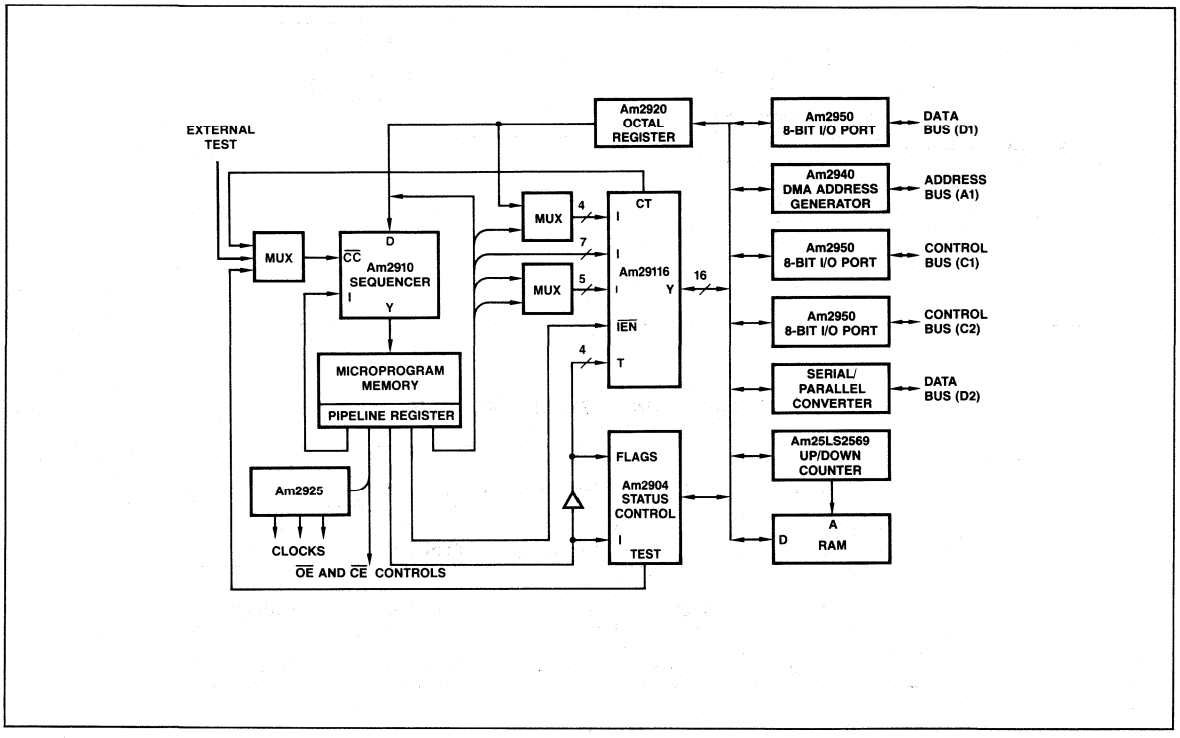
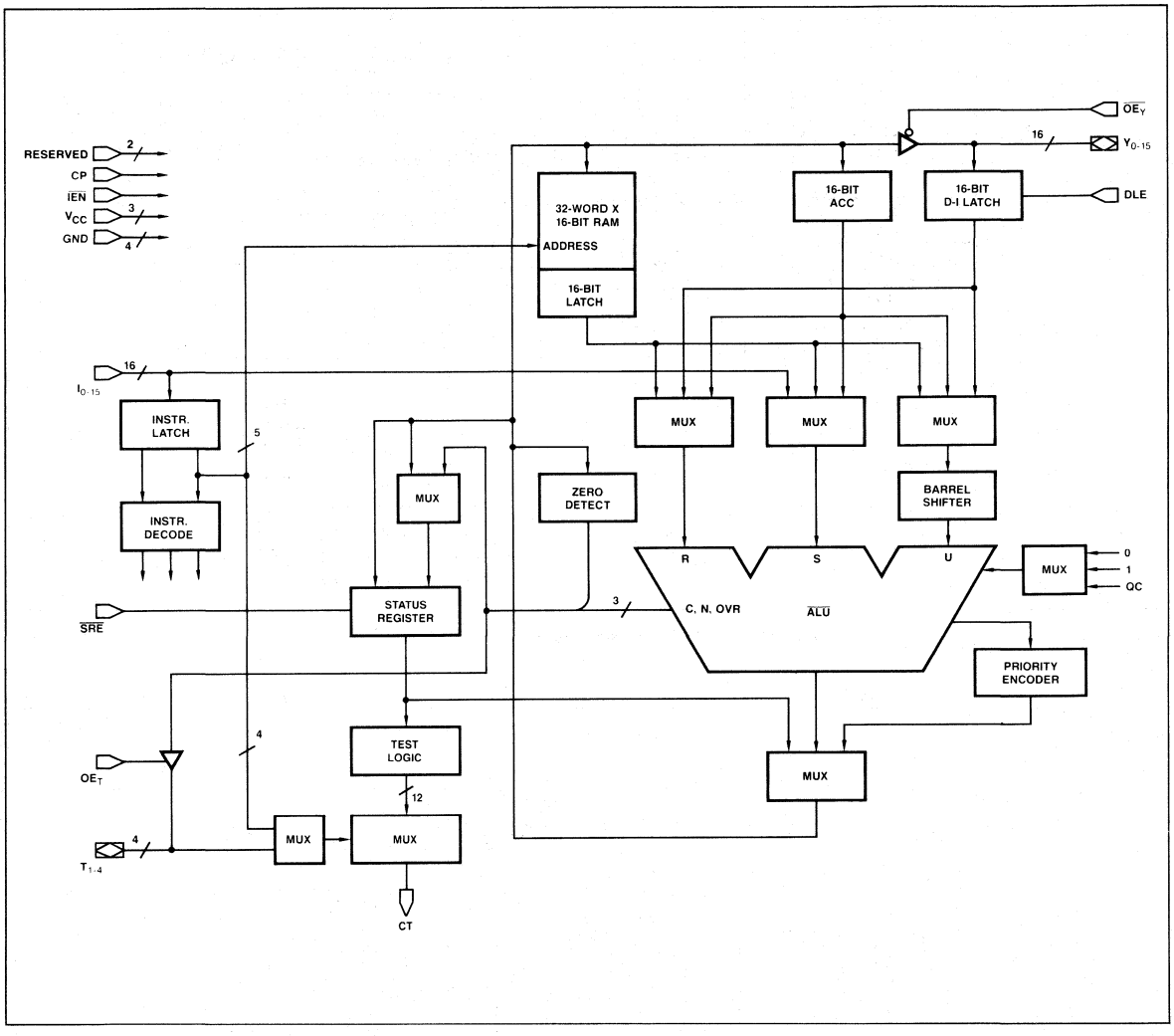


Figure 23. Peripheral Controller, Maximum Performance Configuration

Am29116
COMPARED TO OTHER PROCESSORS



COMPARISON OF EXECUTION TIMES

Processor Type	Bit Test	Bit Set	16-Bit Add	Rotate by N	Rotate by N and Merge
Am8048	2* 5000ns**	1 2500ns	6 15,000ns	12 382,500ns	28 422,500ns
Am9080	5 4250ns	2 1750ns	1 2500ns	17 200,000ns	37 225,000ns
Am29116***	1 100ns	1 100ns	1 100ns	1 100ns	1 100ns

*Number of instruction words
**Execution time
***Target

PERFORMANCE ANALYSIS

Processor Type	Instruction Type	
	Bit Test	Bit Set
Am8048	2 / 5,000ns	1 / 2,500ns
Am9080	5 / 4,250ns	2 / 1,750ns
AmZ8000	1 / 1,000ns	1 / 1,000ns
Am2901B (4) Am2904 Am2902A Am25LS2538 (2)	1 / 100ns	1 / 100ns
2901B (4) Am2904 Am2902A Am25LS2538 (2) Am25S10 (8)	1 / 100ns	1 / 100ns
Am29116*	1 / 100ns	1 / 100ns

# of Instruction Words / Execution Time

*Target

The Am29116 is designed to excel as the data path processor of an intelligent peripheral controller. These performance comparisons demonstrate its speed for logic and bit manipulation instruction types.

PERFORMANCE ANALYSIS

Processor Type	Instruction Type	
	Rotate by N	Rotate and Merge
Am8048	28 / 212,500ns	44 / 252,500ns
Am9080	32 / 113,000ns	42 / 138,000ns
AmZ8000	8 / 11,250ns	12 / 15,250ns
Am2901B (4) Am2904 Am2902A Am25LS2538 (2)	9 / 1,025ns	12 / 1,325ns
Am2901B (4) Am2904 Am2902A Am25LS2538 (2) Am25S10 (8)	1 / 160ns	4 / 460ns
Am29116*	1 / 100ns	1 / 100ns

# of Instruction Words / Execution Time

*Target

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PERFORMANCE ANALYSIS

Processor Type	Instruction Type	
	16-Bit Add	16-Bit Multiply
Am8048	6 / 15,000ns	54 / 810,000ns
Am9080	1 / 2,500ns	40 / 509,000ns
AmZ8000	1 / 1,000ns	1 / 17,500ns
Am2901B (4) Am2904 Am2902A Am25LS2538 (2)	1 / 115ns	2 / 2,000ns
Am2901B (4) Am2904 Am2902A Am25LS2538 (2) Am25S10 (8)	1 / 115ns	2 / 2,000ns
Am29116*	1 / 100ns	12 / 9,600ns

*Target

# of Instruction Words / Execution Time

Am29500
Digital Signal Processor Family Index

The Am29500 Family

A New High Performance Architecture For Digital Signal/Array Processing

The new system designs of the '80s will continue to press the performance limits of technology. Parallel processing and pipelined architectures will become the standard approach. The new architectures are best implemented with a chip set that has been designed from the ground up with high speed signal processing in mind.

The Am29500 Family is designed specifically for these new architectures. Every key product feature supports the system end objective of maximum performance and flexibility. These include:

- Microprogrammable, parallel functions
- Pipelined organization used throughout
- IMOX™ process and ECL internal structures
- TTL I/O for easy interfacing

The first members of the family are targeted for the efficient execution of DSP and array processing algorithms. The most common include Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) digital filters and Fast Fourier Transform (FFT) processors.

The first major building blocks are designed to support maximum performance signal processing applications.

Included are:

- **Am29501 Microprogrammable Signal Processor**

  A specialized parallel processor which executes multiple simultaneous data operations. Its Register/ALU structure provides the key functional element for a high performance signal processing system.

- **Am29540 FFT Address Sequencer**

  This algorithm-specific VLSI chip generates data and coefficient addresses for the Fast Fourier Transform. It supports a wide variety of FFT algorithms in either radix-2 or radix-4.

- **Am29516/29517 High Speed 16 x 16-Bit Parallel Multipliers**

  Both are 16 x 16-bit Parallel Multipliers. The Am29516 is pin and functionally compatible with the MPY-16HJ, but with an added multiplexer to output the LSP at the MSP port. The Am29517 is the same function, but with clock enables for microprogrammed applications.

- **Am29520/29521 Multilevel Pipeline Registers**

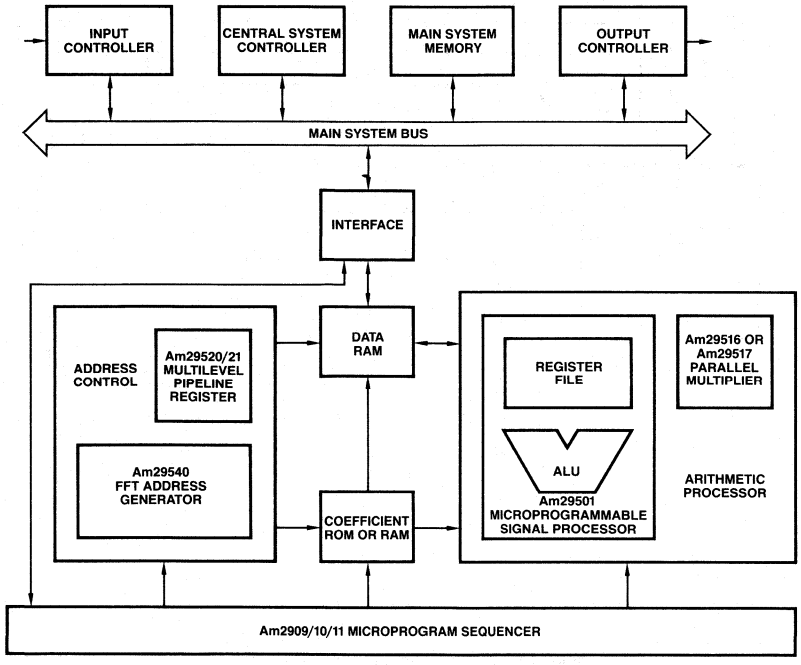
  Both devices contain four 8-bit registers for dual two-stage (FFT butterfly) or single four-stage (general purpose) data or address pipelining. Combined load-and-shift (Am29520) or separate load-and-shift (Am29521) control options are available.

- **Am295XX more components to be announced.**

A high performance signal processor may be constructed as shown in the diagram. The processor is built entirely with new Am29500 digital signal processing and Am2900 devices. Such a processor is attached as a slave to the main system bus to perform the multitude of arithmetic operations which prevail in DSP algorithms.

Using this architecture it is possible to implement a radix-2FFT butterfly in four instruction cycles. This allows a 1024-point complex FFT to be performed in approximately 3ms.

HIGH PERFORMANCE SIGNAL PROCESSOR



9

Am29501

Microprogrammable Signal Processor

DISTINCTIVE CHARACTERISTICS

- Expandable 8-bit slice
- Fast, flexible storage for data pipelining
- 8-bit ALU
  - 4 Arithmetic Operations
  - 4 Logic Operations
- Six 8-bit Registers
  - Structure permits multiple register-to-register moves
- Multiple Bus Architecture
  - Allows multiple simultaneous data manipulation
- Completely microprogrammable
  - No instruction encoding
  - All operation combinations available
- 100ns microcycle
- 64-pin DIP, single 5V supply
- 100% product assurance testing to MIL-STD-883 requirements

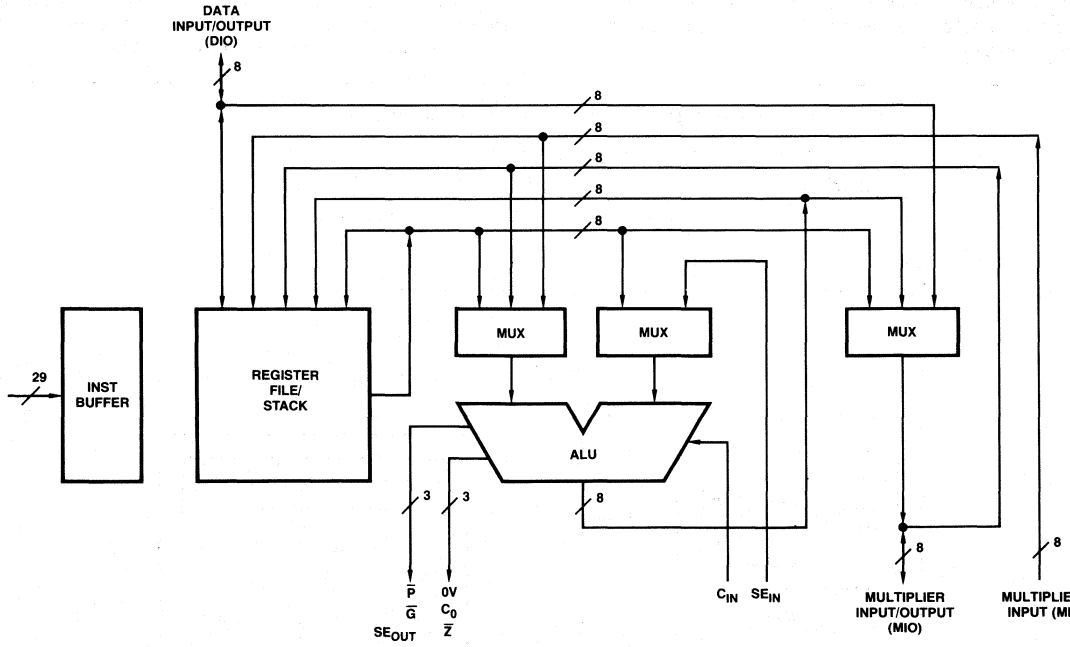
GENERAL DESCRIPTION

The Am29501 is an expandable 8-bit slice register/ALU device designed to operate in a signal processing environment. It enables the designer to construct a CPU which operates with complex numbers and efficiently supports a multiplier. Its storage and bus structures provide a high degree of parallelism and are especially efficient for vector operations.

Six 8-bit registers are provided with the capability of moving data between registers without busying internal busses. The ALU has four arithmetic (R Plus S, R Minus S, S Minus R, Pass R) and four logic instructions (R AND S, R OR S, R EX-OR S, $\overline{R}$). Four of the six registers may act as accumulators. Three output busses are provided, two of which communicate with the multiplier, and the third communicating with the data memory.

A feature of the part is its lack of instruction encoding which permits optimum use of its flexible architecture.

LOGIC DIAGRAM



Am29516 • Am29517

16 x 16-Bit Parallel Multipliers

DISTINCTIVE CHARACTERISTICS

- High speed 16 x 16 parallel multiplier
- Two's complement, unsigned or mixed operands
- Full product multiplexed at output
- Am29516 pin and functionally compatible with TRW MPY-16HJ
- Am29517 optimized for microprogramming, single clock with register enables
- 64-pin package
- 100% product assurance testing to MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am29516 and Am29517 are high speed parallel 16 x 16-bit multipliers utilizing internal ECL logic to generate a 32-bit product. 17-bit input registers are provided for the X and Y operands and their associated mode controls X_m and Y_m. These mode controls are used to specify the operands as 2's complement or unsigned numbers.

At the output of the multiplier array a format adjust control (FA) allows the user to select either a full 32-bit product or a left shifted 31-bit product suitable for 2's complement only.

Two 16-bit output registers are provided to hold the most and least significant halves of the product (MSP and LSP) as defined by FA. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high. A round control (RND) allows the rounding of the MSP. This control is registered, and is entered whenever either input register is clocked.

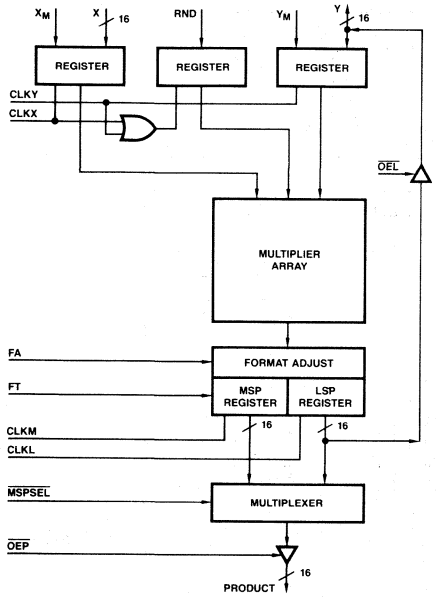
The two halves of the product may be routed to a 16-bit 3-state output port (P) via a multiplexer. In addition the LSP is connected to the Y-input port through a separate 3-state buffer.

In the Am29516 the X, Y, MSP and LSP registers have independent clocks (CLKX, CLKY, CLKM, CLKL). The output multiplexer control ($\overline{\text{MSPSEL}}$) uses a pin which is a supply ground in the TRW MPY 16HJ. When this control is LOW the function is that of the MPY16HJ, thus allowing full compatibility.

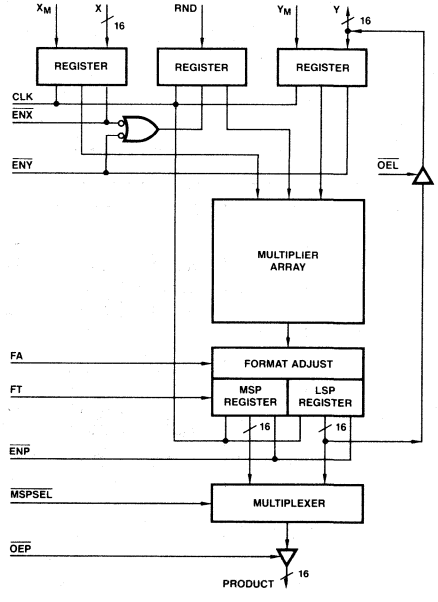
The Am29517 differs in that it has a single clock input (CLK) and three register enables ($\overline{\text{ENX}}$, $\overline{\text{ENY}}$, $\overline{\text{ENP}}$) for the two input registers and the entire product. This facilitates the use of the part in microprogrammed systems. In both parts data is entered into the registers on the positive edge of the clock.

LOGIC DIAGRAMS

Am29516



Am29517



9

Am29520 • Am29521

Multilevel Pipeline Registers

DISTINCTIVE CHARACTERISTICS

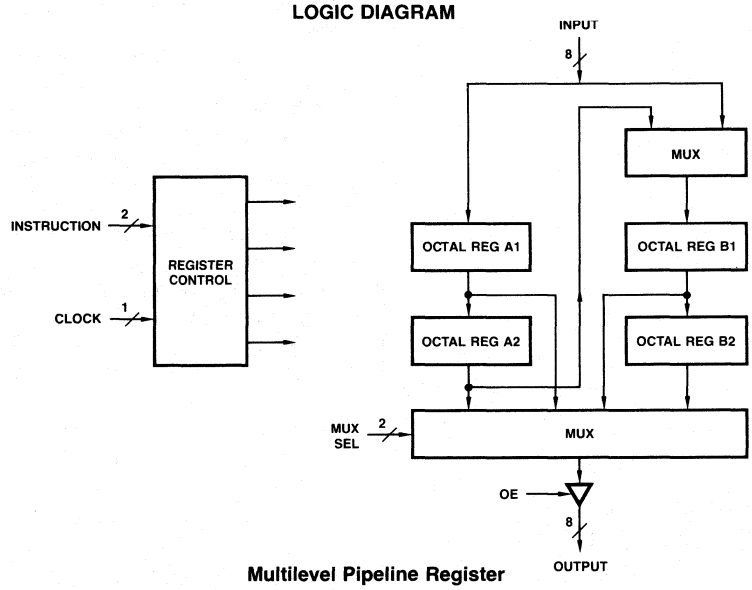
- Four 8-bit high speed registers
- Dual two-level or single four-level operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- 24-pin 0.3" package
- 100% product assurance screening to MIL-STD-883

FUNCTIONAL DESCRIPTIONS

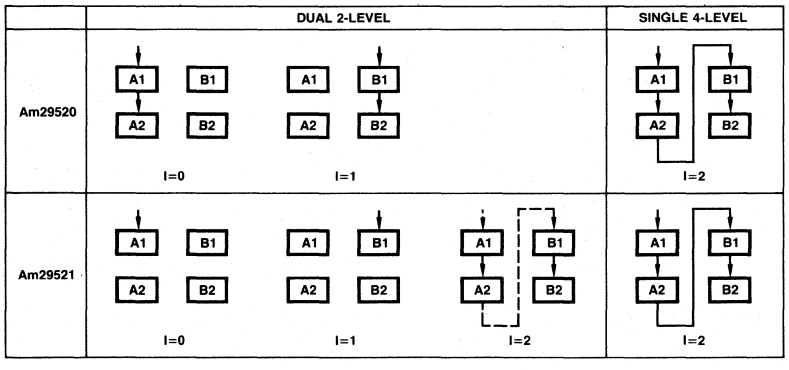
The Am29520 and Am29521 each contain four 8-bit registers. These may be operated in a dual 2-level scheme or in a single 4-level scheme. A single 8-bit input is provided and all four registers are available at the 8-bit 3-state output.

The Am29520 and Am29521 differ only in the way data is loaded into and between the registers in dual 2-level operation. This difference is illustrated in Figure 1. In the Am29520 when data is shifted into the first level (I=0 or I=1) the existing data in the first level is moved to the second level. In the Am29521 these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level instruction (I=2). This transfer also causes the first level to change. In either part I=3 is a NO-OP.

LOGIC DIAGRAM



Multilevel Pipeline Register



I=3 NO-OP

Figure 1.

Am29540

Programmable FFT Address Sequencer

DISTINCTIVE CHARACTERISTICS

- Generates data and coefficient addresses
- Programmable transform length 2 to 65,536 points
- Radix-2 or Radix-4
- Decimation in frequency (DIF) or decimation in time (DIT) FFT algorithms supported
- In-place or non-in place transformation
- 40-pin DIP package
- 5 volt single supply
- 100% product assurance screening to MIL-STD-883

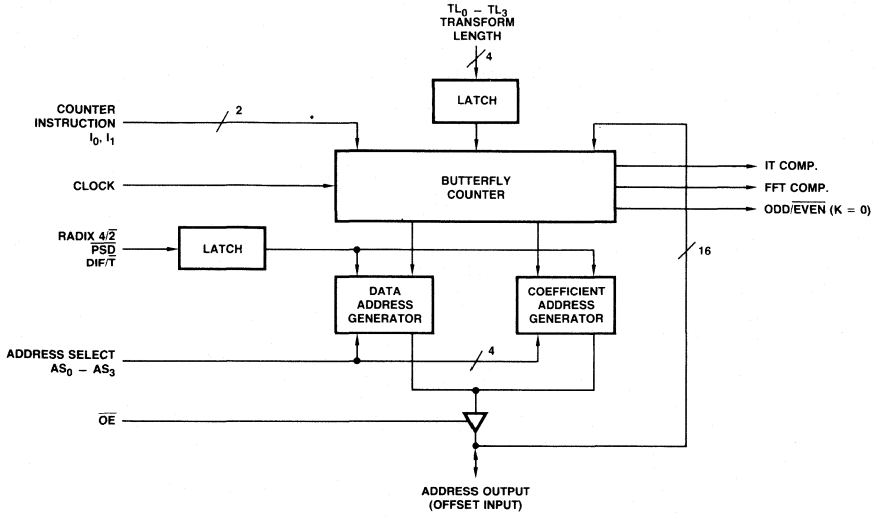
FUNCTIONAL DESCRIPTION

The Am29540 Fast Fourier Transform Address Sequencer generates all the data (RAM) and coefficient (ROM) addresses necessary to perform the repetitive butterfly operations of the FFT. Decimation in time and decimation in frequency algorithms are supported (control DIT/$\overline{F}$) in radix-2 or radix-4 (RADIX4/$\overline{2}$). A radix-2 real valued input (RVI) transform is also supported. For radix-2 operation the transform length is programmable in powers of 2 from 2 to 65,536 points. In radix-4 the range is 4 to 65,536 in powers of 4.

Address sequences can be selected to be compatible with data which may or may not have been pre-scrambled ("bit-reversed"). If the data has been pre-scrambled the control $\overline{PSD}$ must be LOW to select the correct sequence. If the data is not pre-scrambled ($\overline{PSD}$ HIGH) and an in-place transform is performed, the output data will necessarily be in bit-reversed order. If this is not desirable, alternate addresses are available for a non-in place, non-bit-reversing algorithm.

The butterfly counter operates on the positive clock edge and responds to four instructions. COUNT causes the counter to increment to the next butterfly. RESET causes the counter to initialize for the specified transform length. RESET/LOAD causes the counter to initialize and a data address offset to be loaded into the part via the bi-directional 3-state ADDRESS port. This offset is effectively OR-ed onto the higher significance bits of the address which are unused for the selected transform length. A HOLD instruction is also provided. Three status lines are provided. ODD/EVEN (K = 0) controls the alternation of read and write memories for non-in place transforms and determines the butterfly structure in the RVI transform. Iteration complete (ITCOMP) flags the bottom of a "column" of butterflies and is used in conjunction with block floating point schemes. FFT COMP identifies the last butterfly of the transform.

LOGIC DIAGRAM



FFT Address Sequencer

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RAMs, PROMs, Address Control Units Index

Am29700 • Am29701

Non-Inverting Schottky 64-Bit Random Access Memories

Refer to

Am27S06 • Am27S07

Bipolar Memory Data Sheets

The Am29700 is replaced by the Am27S06 (open collector).

The Am29701 is replaced by the Am27S07 (3-state).

Am29702 • Am29703

Schottky 64-Bit Random Access Memories

Refer to

Am27S02 • Am27S03

Bipolar Memory Data Sheets

The Am29702 is replaced by the Am27S02 (open collector).

The Am29703 is replaced by the Am27S03 (3-state).

Am29705

16-Word by 4-Bit 2-Port RAM

Distinctive Characteristics

- 16-word by 4-bit, 2-port RAM
- Two output ports, each with separate output control
- Separate four-bit latches on each output port
- Data output is non-inverting with respect to data input
- Chip Select and Write Enable inputs for ease cascading
- Advanced Low-Power Schottky processing
- 100% reliability testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

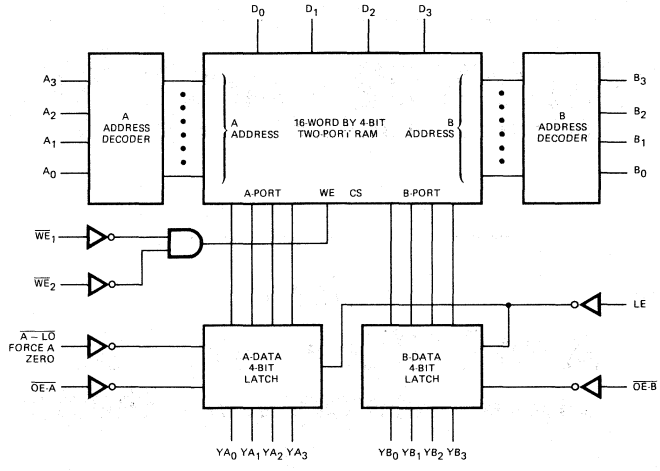
The Am29705 is a 16-word by 4-bit, two-port RAM built using advanced Low-Power Schottky processing. This RAM features two separate output ports such that any two 4-bit words can be read from these outputs simultaneously. Each output port has a four-bit latch but a common Latch Enable (LE) input is used to control all eight latches. The device has two Write Enable ($\overline{WE}$) inputs and is designed such that the Write Enable 1 ($\overline{WE}_1$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge triggered.

The device has a fully decoded four-bit A-address field to address any of the 16 memory words for the A-output port. Likewise, a four-bit B-address input is used to simultaneously select any of the 16 words for presentation at the B-output port. New incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load new data into the device.

The Am29705 features three-state outputs so that several devices can be cascaded to increase the total number of memory words in the system. The A-output port is in the high-impedance state when the $\overline{OE}$-A input is HIGH. Likewise, the B-output port is in the high-impedance state when the $\overline{OE}$-B input is HIGH. Four devices can be paralleled using only one Am25LS139 decoder for output control.

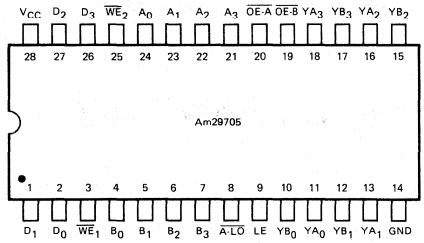
The Write Enable inputs control the writing of new data into the RAM. When both Write Enable inputs are LOW, new data is written into the word selected by the B-address field. When either Write Enable input is HIGH, no data is written into the RAM.

LOGIC DIAGRAM



MPR-25

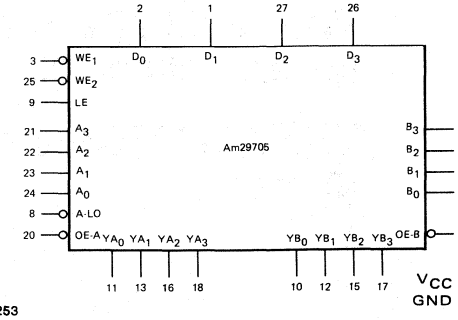
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-252

LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

MPR-253

WITCHING CHARACTERISTICS(Cont.)

nput Levels = 0V and 3.0V, Transitions Measured at 1.5V)

linimum Set-up and Hold Times (in ns)

arameters	From	To	Conditions	$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max.	$T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max.
Data Set-up Time	D Stable	Either $\overline{WE}$ HIGH		20	25
Data Hold Time	Either $\overline{WE}$ HIGH	D Changing		3	5
Address Set-up Time	B Stable	Both $\overline{WE}$ LOW		5	5
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		0	0
Latch Close Before Write Begins	LE LOW	$\overline{WE}_1$ LOW	$\overline{WE}_2$ LOW	0	0
	LE LOW	$\overline{WE}_2$ LOW	$\overline{WE}_1$ LOW	0	0
Address Set-up Before Latch Closes	A or B Stable	LE LOW		45	50
Time Between Write Enables	$\overline{WE}_1$ HIGH	$\overline{WE}_2$ LOW		7	7

linimum Pulse Widths

arameters	Input	Pulse	Conditions	$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max.	$T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max.
Write Pulse Width	$\overline{WE}_1$	HIGH-LOW-HIGH	$\overline{WE}_2$ LOW	25	25
	$\overline{WE}_2$	HIGH-LOW-HIGH	$\overline{WE}_1$ LOW	20	20
A Latch Reset Pulse	$\overline{A\text{-}LO}$	HIGH-LOW-HIGH		20	20
Latch Data Capture	LE	LOW-HIGH-LOW		20	25

FUNCTION TABLES

WRITE CONTROL

$\overline{WE}_1$	$\overline{WE}_2$	Function	RAM Outputs at Latch Inputs A-Port	B-Port
L	L	Write D Into B	A data (A ≠ B)	Not Specified
X	H	No write	A data	B data
H	X	No write	A data	B data

H = HIGH
L = LOW
X = Don't care

YA READ

Inputs $\overline{OE-A}$	Inputs $\overline{A-LO}$	Inputs LE	YA Output	Function
H	X	X	Z	High impedance
L	L	X	L	Force YA LOW
L	H	H	A – Port RAM data	Latches transparent
L	H	L	NC	Latches retain data

H = HIGH
L = LOW
X = Don't care
Z = High impedance
NC = No change

YB READ

Inputs $\overline{OE-B}$	Inputs LE	YB Output	Function
H	X	Z	High impedance
L	H	B – Port RAM data	Latches transparent
L	L	NC	Latches retain data

H = HIGH
L = LOW
X = Don't care
Z = High impedance
NC = No change

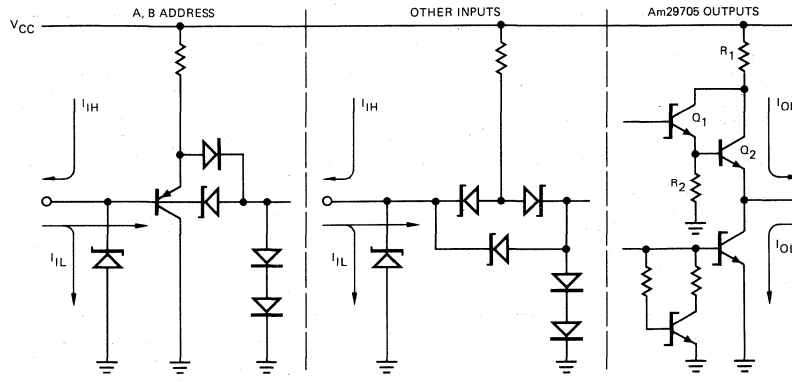
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_1	1	1	–	–
D_0	2	1	–	–
$\overline{WE}_1$	3	1	–	–
B_0	4	0.55	–	–
B_1	5	0.55	–	–
B_2	6	0.55	–	–
B_3	7	0.55	–	–
$\overline{A-LO}$	8	1	–	–
LE	9	1	–	–
YB_0	10	–	100/200	33
YA_0	11	–	100/200	33
YB_1	12	–	100/200	33
YA_1	13	–	100/200	33
GND	14	–	–	–
YB_2	15	–	100/200	33
YA_2	16	–	100/200	33
YB_3	17	–	100/200	33
YA_3	18	–	100/200	33
$\overline{OE-B}$	19	1	–	–
$\overline{OE-A}$	20	1	–	–
A_3	21	0.55	–	–
A_2	22	0.55	–	–
A_1	23	0.55	–	–
A_0	24	0.55	–	–
$\overline{WE}_2$	25	1	–	–
D_3	26	1	–	–
D_2	27	1	–	–
V_{CC}	28	–	–	–

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and –0.36mA measured at 0.4V LOW.

10

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-254

DEFINITION OF TERMS

D_0, D_1, D_2, D_3 Data Inputs. New data is written into the RAM through these inputs.

A_0, A_1, A_2, A_3 The A-address Inputs. The four-bit field presented at the A inputs selects one of the 16 memory words for presentation to the A-Data Latch.

B_0, B_1, B_2, B_3 The B-address inputs. The four-bit field presented at the B inputs selects one of the 16 memory words for presentation to the B-Data Latch. The B address field also selects the word into which new data is written.

YA_0, YA_1, YA_2, YA_3 The four A-Data Latch Outputs.

YB_0, YB_1, YB_2, YB_3 The four B-Data Latch Outputs.

$\overline{WE}_1, \overline{WE}_2$ Write Enables. When both Write Enables are LOW, new data is written into the word selected by the B-address field. If either Write Enable input is HIGH, no new data can be written into the memory.

$\overline{OE}$-A A-port Output Enable. When $\overline{OE}$-A is LOW, data in the A-Data Latch is present at the YA_i outputs. If $\overline{OE}$-A is HIGH, the YA_i outputs are in the high-impedance (off) state.

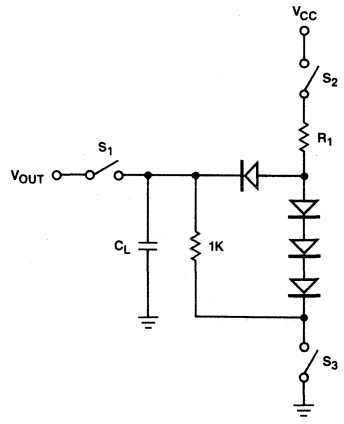
$\overline{OE}$-B B-port Output Enable. When $\overline{OE}$-B is LOW, data in the B-Data Latch is present at the YB_i outputs. When $\overline{OE}$-B is HIGH, the YB_i outputs are in the high-impedance (off) state.

LE Latch Enable. The LE input controls the latches for both the RAM A-output port and RAM B-output port. When the LE input is HIGH, the latches are open (transparent) and data from the RAM, as selected by the A and B address fields, is present at the outputs. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of the current A and B address field inputs.

$\overline{A\text{-}LO}$ Force A Zero. This input is used to force the outputs of the A-port latches LOW independent of the Latch Enable input or A-address field select inputs. Thus, the A-output bus can be forced LOW using this control signal. When the $\overline{A\text{-}LO}$ input is HIGH, the A latches operate in their normal fashion. Once the A latches are forced LOW, they remain LOW independent of the $\overline{A\text{-}LO}$ input if the latches are closed.

TEST OUTPUT LOAD CONFIGURATIONS FOR Am29705

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

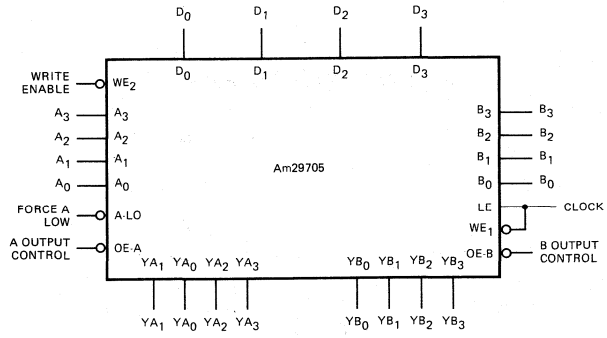
Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all A.C. tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5pF for output disable tests.

TEST OUTPUT LOADS FOR Am29705

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	YA_{0-3}	A	312	1K
–	YB_{0-3}	A	312	1K

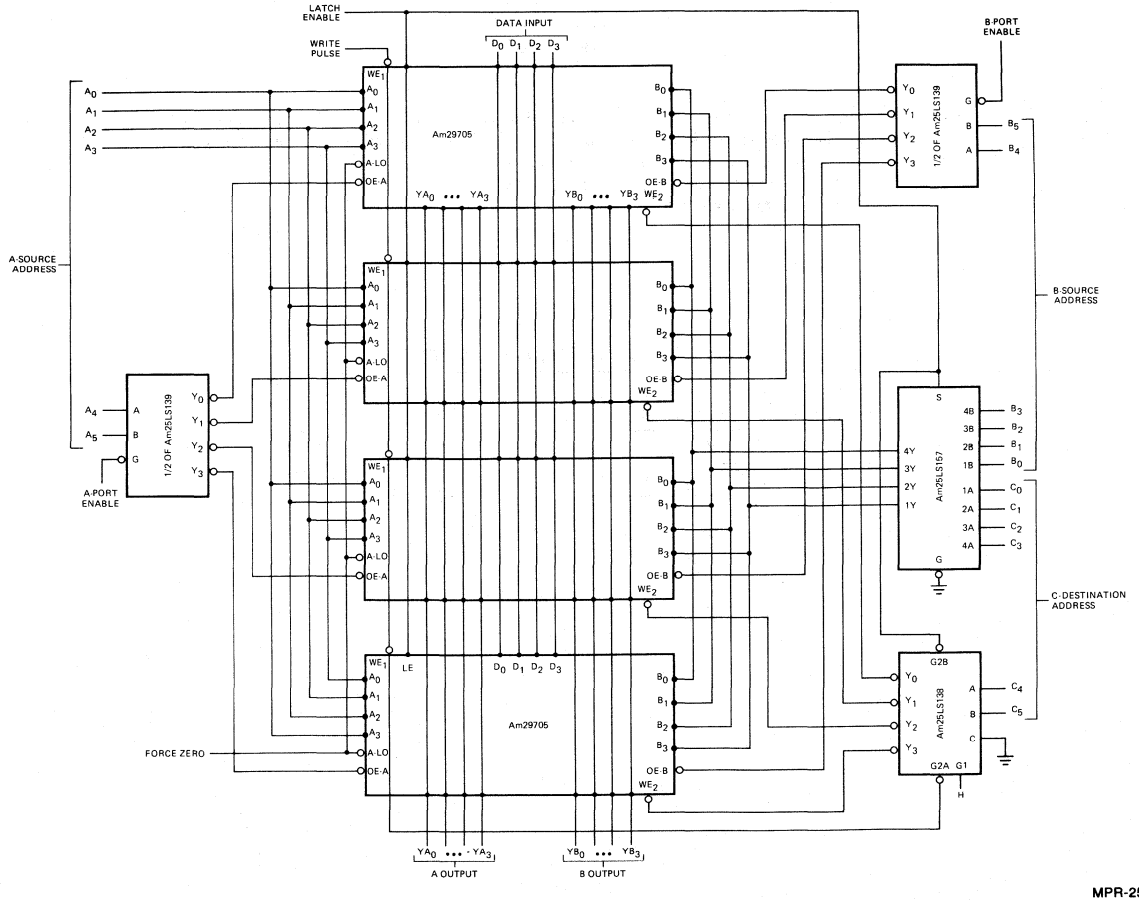
For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS



MPR-257

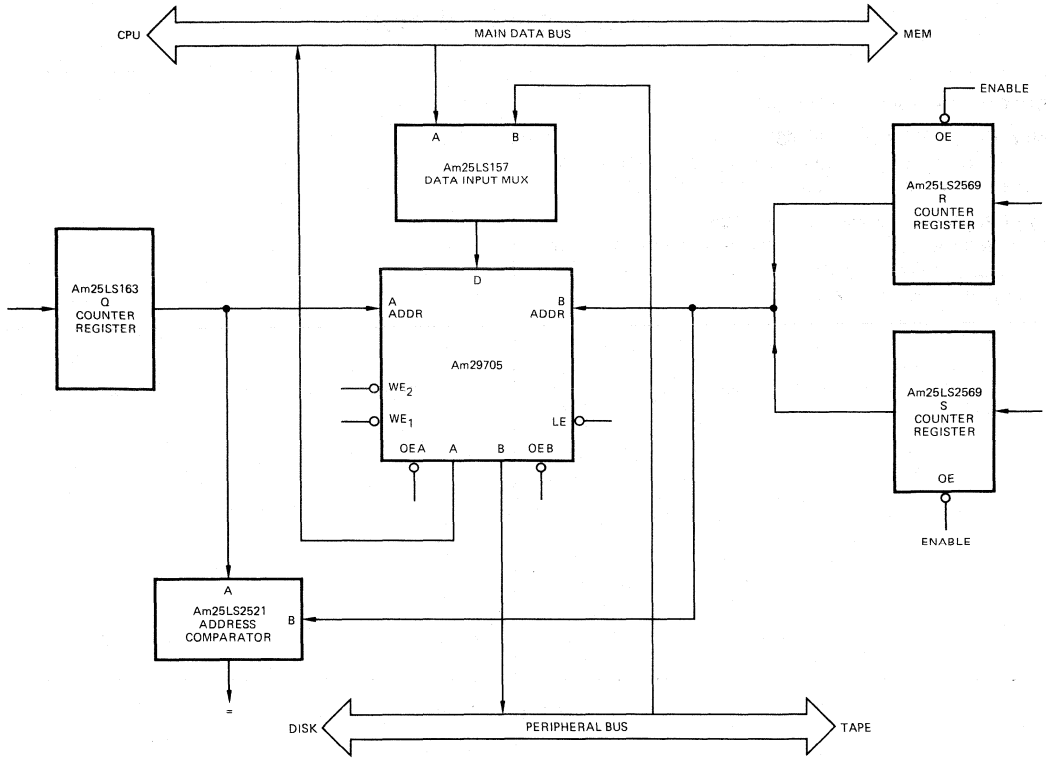
A 16-word by 4-bit two-port RAM with LE and WE_1 connected to make the device appear edge triggered. WE_1 and WE_2 are logically identical but are electrically slightly different. For synchronous operation without possibility of race, WE_1 should be connected to LE.



MPR-258

A 64-word by 4-bit three address memory. Data is read from the A address to the YA outputs and from the B address to the YB outputs while the latch enable is HIGH. When the latch enable goes LOW, the YA and YB data is held in the internal latches, and the RAM B address is switched to the C-destination address lines. A write pulse will then deposit the input data into the location selected by the C address.

APPLICATIONS (Cont'd)



The Am29705 as a two-way interface buffer. Data may be passed between the main data bus and the peripheral data bus under I/O control. The two-port RAM allows data to be written into buffer storage from a peripheral device, using the B address port and the S counter register, while it is being read into main memory, using the A address port and the Q counter register. This simultaneous read/write capability facilitates DMA transfers because the CPU can ignore write requests from the peripheral device. Data output from CPU to the peripheral device is handled by sequential write and read operations. Data is written into buffer storage from the CPU, using the B address port and the R counter register. It is read onto the peripheral device using the B address port and either the R register, for single word transfers, or the S register, for block transfers.

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29705PC	P-28	C	C-1
AM29705DC	D-28	C	C-1
AM29705DC-B	D-28	C	B-2 (Note 4)
AM29705DM	D-28	M	C-3
AM29705DM-B	D-28	M	B-3
AM29705FM	F-28-1	M	C-3
AM29705FM-B	F-28-1	M	B-3
AM29705XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29705XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am29705A

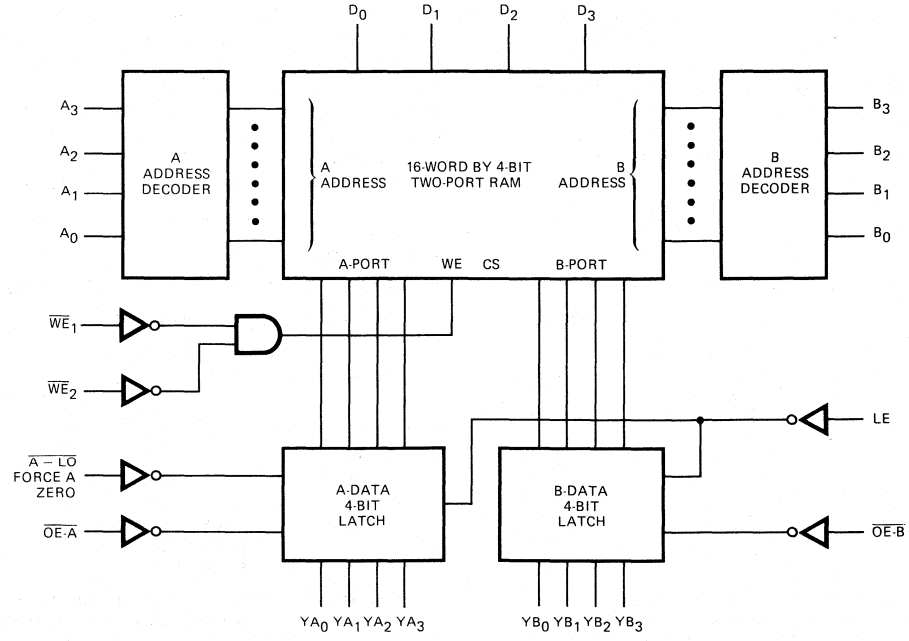
16-Word by 4-Bit 2-Port RAM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Faster Version of the Am29705**
  The Am29705A has a design objective of a 30-40% speed improvement on the critical paths versus the Am29705.
- **Plug-in Replacement for the Am29705**
  The Am29705A is a pin-for-pin replacement for the Am29705. Systems using the Am29705 will be able to use the Am29705A instead with no design changes.

LOGIC DIAGRAM



MPR-742

SWITCHING CHARACTERISTICS

Typical Room Temperature (in ns) (R_L = 390Ω, C_L = 50pF)
(Output Levels = 0V and 3.0V, Transitions Measured at 1.5V)

Parameters	From	To	Conditions	T_A = 25°C V_{CC} = 4.75 to 5.25V
Access Time	A Address Stable or B Address Stable	YA Stable or YB Stable	LE = HIGH	13
Turn-On Time	$\overline{OE}$-A or $\overline{OE}$-B LOW	YA or YB Stable		6
Turn-Off Time	$\overline{OE}$-A or $\overline{OE}$-B HIGH	YA or YB Off		13
Reset Time	$\overline{A\text{-}LO}$ LOW	YA LOW		8
Enable Time	LE HIGH	YA and YB Stable		8
Transparency	$\overline{WE}$ or $\overline{WE}_2$	YA or YB		12
	D	YA or YB		14

Minimum Set-up and Hold Times (in ns)

Parameters	From	To	Conditions	T_A = 25°C V_{CC} = 5.0V ±5% Max
Data Set-Up Time	D Stable	Either $\overline{WE}$ HIGH		2
Data Hold Time	Either $\overline{WE}$ HIGH	D Changing		4
Address Set-Up Time	B Stable	Both $\overline{WE}$ LOW		−1
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		8
Latch Close Before Write Begins	LE LOW	$\overline{WE}_1$ LOW	$\overline{WE}_2$ LOW	0
	LE LOW	$\overline{WE}_2$ LOW	$\overline{WE}_1$ LOW	0
Address Set-Up Before Latch Closes	A or B Stable	LE LOW		7

Minimum Pulse Widths

Parameters	Input	Pulse	Conditions	T_A = 0 to +70°C V_{CC} = 5.0V ±5% Max
Write Pulse Width	$\overline{WE}_1$	HIGH-LOW-HIGH	$\overline{WE}_2$ LOW	25
	$\overline{WE}_2$	HIGH-LOW-HIGH	$\overline{WE}_1$ LOW	20
A Latch Reset Pulse	$\overline{A\text{-}LO}$	HIGH-LOW-HIGH		20
Latch Data Capture	LE	LOW-HIGH-LOW		20

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Am29707
16-Word by 4-Bit 2-Port RAM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- 16-word by 4-bit, 2-port RAM
- 20% improved cycle time over Am29705A when used with Am29203 in a three address architecture
- Two output ports, each with separate output control
- Separate four-bit latches on each output port with separate enables
- Data output is non-inverting with respect to data input
- Chip Select and Write Enable inputs for ease in cascading
- Advanced Low-Power Schottky processing
- 100% reliability testing in compliance with MIL-STD-833

FUNCTIONAL DESCRIPTION

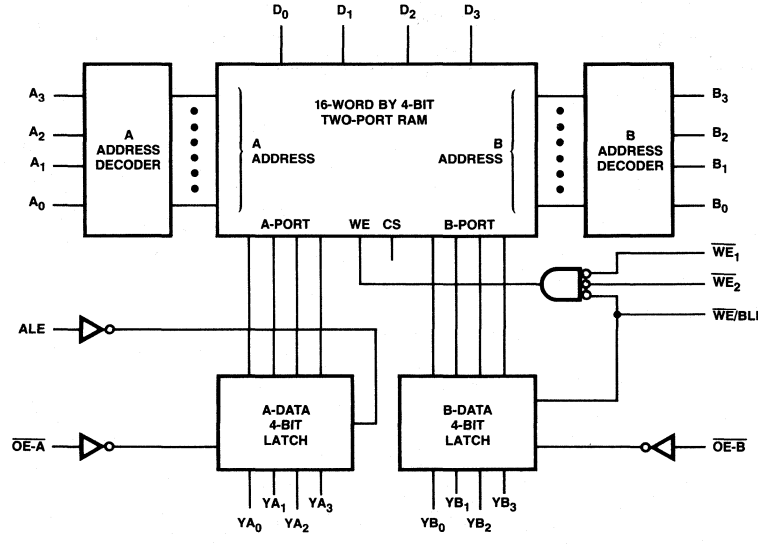
The Am29707 is a 16-word by 4-bit, two-port RAM built using advanced Low-Power Schottky processing. This RAM features two separate output ports such that any two 4-bit words can be read from these outputs simultaneously. Each output port has a four-bit latch with separate Latch Enable (LE) inputs. The device has three Write Enable ($\overline{WE}$) inputs. The combination $\overline{WE}$/BLE makes the output of the B Data Latch appear to be edge triggered. The $\overline{WE}$/BLE may also be wired together with ALE to make the entire RAM appear edge triggered.

The device has a fully decoded four-bit A-address field to address any of the 16 memory words for the A-output port. Likewise, a four-bit B-address input is used to simultaneously select any of the 16 words for presentation at the B-output port. New incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load new data into the device.

The Am29707 features three-state outputs so that several devices can be cascaded to increase the total number of memory words in the system. The A-output port is in the high-impedance state when the $\overline{OE}$-A input is HIGH. Likewise, the B-output port is in the high-impedance state when the $\overline{OE}$-B input is HIGH. Four devices can be paralleled using only one Am25LS139 decoder for output control.

The Write Enable inputs control the writing of new data into the RAM. When all three Write Enables inputs are LOW, new data is written into the word selected by the B-address field. When any of the Write Enable inputs are HIGH, no data is written into the RAM. The $\overline{WE}$/BLE may be connected directly to the $\overline{IEN}$ of the Am29203 for speed improved cycle times over the Am29705A.

LOGIC DIAGRAM



SWITCHING CHARACTERISTICS

Typical Room Temperature (in ns) (R_L = 390Ω, C_L = 50pF)
(Output Levels = 0V and 3.0V, Transitions Measured at 1.5V)

Parameters	From	To	Conditions	T_A = 25°C, V_{CC} = 4.75 to 5.25V
Access Time	A Address Stable or B Address Stable	YA Stable or YB Stable	LE = HIGH	13
Turn-On Time	$\overline{OE}$-A or $\overline{OE}$-B LOW	YA or YB Stable		6
Turn-Off Time	$\overline{OE}$-A or $\overline{OE}$-B HIGH	YA or YB Off		13
Reset Time	$\overline{A\text{-}LO}$ LOW	YA LOW		8
Enable Time	LE HIGH	YA and YB Stable		8
Transparency	$\overline{WE}$ or $\overline{WE}_2$	YA or YB		12
	D	YA or YB		14

Minimum Set-up and Hold Times (in ns)

Parameters	From	To	Conditions	T_A = 25°C, V_{CC} = 5.0V ±5% Max
Data Set-Up Time	D Stable	Either $\overline{WE}$ HIGH		2
Data Hold Time	Either $\overline{WE}$ HIGH	D Changing		4
Address Set-Up Time	B Stable	Both $\overline{WE}$ LOW		−1
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		8
Latch Close Before Write Begins	LE LOW	$\overline{WE}_1$ LOW	$\overline{WE}_2$ LOW	0
	LE LOW	$\overline{WE}_2$ LOW	$\overline{WE}_1$ LOW	0
Address Set-Up Before Latch Closes	A or B Stable	LE LOW		7

Minimum Pulse Widths

Parameters	Input	Pulse	Conditions	T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Max
Write Pulse Width	$\overline{WE}_1$	HIGH-LOW-HIGH	$\overline{WE}_2$ LOW	25
	$\overline{WE}_2$	HIGH-LOW-HIGH	$\overline{WE}_1$ LOW	20
A Latch Reset Pulse	$\overline{A\text{-}LO}$	HIGH-LOW-HIGH		20
Latch Data Capture	LE	LOW-HIGH-LOW		20

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Am29720 • Am29721

Low-Power Schottky 256-Bit Random Access Memories

Refer to
Am27LS00 • Am27LS01
Bipolar Memory Data Sheets

The Am29720 is replaced by the Am27LS01 (open collector).

The Am29721 is replaced by the Am27LS00 (3-state).

Am29750A • Am29751A

256-Bit Generic Series Bipolar PROM

Refer to
Am27S18 • Am27S19
Bipolar Memory Data Sheets

The Am29750A is replaced by the Am27S18 (open collector).

The Am29751A is replaced by the Am27S19 (3-state).

Am29760A • Am29761A

1024-Bit Generic Series Bipolar PROM

Refer to

Am27S20 • Am27S21

Bipolar Memory Data Sheets

The Am29760A is replaced by the Am27S20 (open collector).

The Am29761A is replaced by the Am27S21 (3-state).

Am29770 • Am29771

2048-Bit Generic Series Bipolar PROM

Refer to

Am27S12 • Am27S13

Bipolar Memory Data Sheets

The Am29770 is replaced by the Am27S12 (open collector).

The Am29771 is replaced by the Am27S13 (3-state).

Am29774 • Am29775

4096-Bit Generic Series Bipolar PROM with Register

Refer to

Am27S26 • Am27S27

Bipolar Memory Data Sheets

The Am29774 is replaced by the Am27S26 (open collector).

The Am29775 is replaced by the Am27S27 (3-state).

Am29803A
16-Way Branch Control Unit

DISTINCTIVE CHARACTERISTICS

- 16 separate instructions – 2 , 4 , 8 , or 16-way branch in one microprogram execution cycle
- Four individual test inputs
- Four individual outputs for driving the four OR inputs on the Am2909 Microprogram Sequencer
- Provides maximum branch capability in a microprogram control unit using the Am2909
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

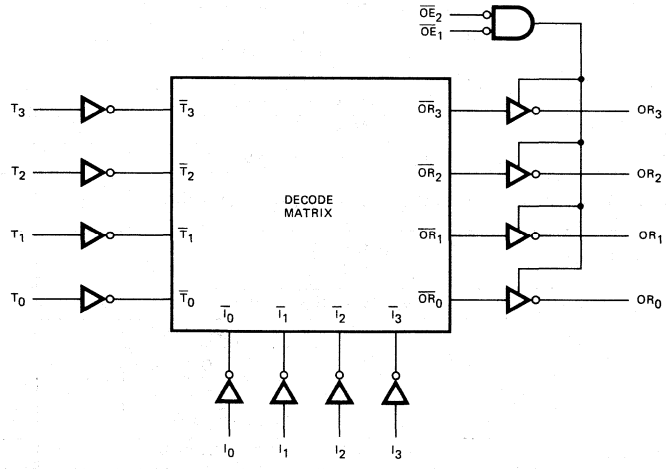
FUNCTIONAL DESCRIPTION

The Am29803A is a Low-Power Schottky processed device that provides 16-way branch control when used in conjunction with the Am2909 Microprogram Sequencer.

The device features 16 instructions that provide all combinations of simultaneous testing of four different inputs. The device has four outputs that are used to drive the four OR inputs of the Am2909 Microprogram Sequencer.

The "zero" instruction inhibits the testing of any of the four test (T) inputs. The remaining 15 instructions are used to test combinations of 1, 2, 3, or 4 of the T inputs simultaneously. If one T input is being tested, the Am29803A will select one of two possible addresses. If two T inputs are being tested, the device will select one of four possible addresses. If three T inputs are being tested, the device will select one of eight possible addresses. If all four T inputs are being tested, the device will select one of sixteen addresses as the field used to drive the OR inputs of the Am2909.

LOGIC DIAGRAM



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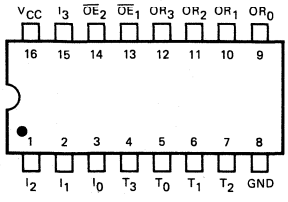
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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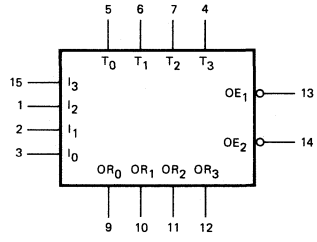
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29803ADC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29803ADM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)
PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		95	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 4.5V			40	μA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 2.4V			40	μA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 0.4V			−40	μA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

WITCHING CHARACTERISTICS

T_A = +25°C, V_{CC} = 5.0V)

arameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} / t_{PHL}	I_i to OR_i	C_L = 15pF, R_L = 2.0kΩ		25	35	ns
t_{PLH} / t_{PHL}	T_i to OR_i			25	35	ns
t_{ZH} / t_{ZL}	$\overline{OE}_i$ to OR_i			15	18	ns
t_{HZ} / t_{LZ}	$\overline{OE}_i$ to OR_i	C_L = 5.0pF, R_L = 2.0kΩ		15	18	ns

;WITCHING CHARACTERISTICS)VER OPERATING RANGE

			COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%		MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10%		
arameters	Description	Test Conditions	Min.	Max.	Min.	Max.	Units
t_{PLH} / t_{PHL}	I_i to OR_i	C_L = 15pF, R_L = 2.0kΩ		45		60	ns
t_{PLH} / t_{PHL}	T_i to OR_i			45		60	ns
t_{ZH} / t_{ZL}	$\overline{OE}_i$ to OR_i			30		30	ns
t_{HZ} / t_{LZ}	$\overline{OE}_i$ to OR_i			20		20	ns

DEFINITION OF FUNCTIONAL TERMS

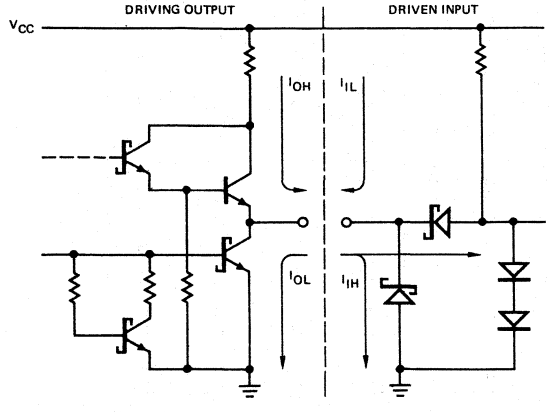
I_0, I_1, I_2, I_3 The four instruction inputs to the device

T_0, T_1, T_2, T_3 The four test inputs for the device

OR_0, OR_1, OR_2, OR_3 The four outputs of the device that are connected to the four OR inputs of the Am2909

$\overline{OE}_1, \overline{OE}_2$ Output Enable. When either $\overline{OE}$ input is HIGH, the OR_i outputs are in the high impedance state. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the OR outputs are enabled and the selected data will be present.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	I_2	0.5	–	–	–
2	I_1	0.5	–	–	–
3	I_0	0.5	–	–	–
4	T_3	0.5	–	–	–
5	T_0	0.5	–	–	–
6	T_1	0.5	–	–	–
7	T_2	0.5	–	–	–
8	GND	–	–	–	–
9	OR_0	–	100	44	44
10	OR_1	–	100	44	44
11	OR_2	–	100	44	44
12	OR_3	–	100	44	44
13	$\overline{OE}_1$	0.5	–	–	–
14	$\overline{OE}_2$	0.5	–	–	–
15	I_3	0.5	–	–	–
16	V_{CC}	–	–	–	–

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FUNCTION TABLE

Function	I_3	I_2	I_1	I_0	T_3	T_2	T_1	T_0	OR_3	OR_2	OR_1	OR_0
No Test	L	L	L	L	X	X	X	X	L	L	L	L
Test T_0	L	L	L	H	X	X	X	L	L	L	L	L
					X	X	X	H	L	L	L	H
Test T_1	L	L	H	L	X	X	L	X	L	L	L	L
					X	X	H	X	L	L	L	H
Test T_0 & T_1	L	L	H	H	X	X	L	L	L	L	L	L
					X	X	L	H	L	L	L	H
					X	X	H	L	L	L	H	L
					X	X	H	H	L	L	H	H
Test T_2	L	H	L	L	X	L	X	X	L	L	L	L
					X	H	X	X	L	L	L	H
Test T_0 & T_2	L	H	L	H	X	L	X	L	L	L	L	L
					X	L	X	H	L	L	L	H
					X	H	X	L	L	L	H	L
					X	H	X	H	L	L	H	H
Test T_1 & T_2	L	H	H	L	X	L	L	X	L	L	L	L
					X	L	H	X	L	L	L	H
					X	H	L	X	L	L	H	L
					X	H	H	X	L	L	H	H
Test T_0, T_1 & T_2	L	H	H	H	X	L	L	L	L	L	L	L
					X	L	L	H	L	L	L	H
					X	L	H	L	L	L	H	L
					X	L	H	H	L	L	H	H
					X	H	L	L	L	H	L	L
					X	H	L	H	L	H	L	H
					X	H	H	L	L	H	H	L
					X	H	H	H	L	H	H	H
Test T_3	H	L	L	L	L	X	X	X	L	L	L	L
					H	X	X	X	L	L	L	H
Test T_0 & T_3	H	L	L	H	L	X	X	L	L	L	L	L
					L	X	X	H	L	L	L	H
					H	X	X	L	L	L	H	L
					H	X	X	H	L	L	H	H
Test T_1 & T_3	H	L	H	L	L	X	L	X	L	L	L	L
					L	X	H	X	L	L	L	H
					H	X	L	X	L	L	H	L
					H	X	H	X	L	L	H	H
Test T_0, T_1 & T_3	H	L	H	H	L	X	L	L	L	L	L	L
					L	X	L	H	L	L	L	H
					L	X	H	L	L	L	H	L
					L	X	H	H	L	L	H	H
					H	X	L	L	L	H	L	L
					H	X	L	H	L	H	L	H
					H	X	H	L	L	H	H	L
					H	X	H	H	L	H	H	H
Test T_2 & T_3	H	H	L	L	L	L	X	X	L	L	L	L
					L	H	X	X	L	L	L	H
					H	L	X	X	L	L	H	L
					H	H	X	X	L	L	H	H
Test T_0, T_2 & T_3	H	H	L	H	L	L	X	L	L	L	L	L
					L	L	X	H	L	L	L	H
					L	H	X	L	L	L	H	L
					L	H	X	H	L	L	H	H
					H	L	X	L	L	H	L	L
					H	L	X	H	L	H	L	H
					H	H	X	L	L	H	H	L
					H	H	X	H	L	H	H	H
Test T_1, T_2 & T_3	H	H	H	L	L	L	H	X	L	L	L	L
					L	L	H	X	L	L	L	H
					L	H	L	X	L	L	H	L
					L	H	H	X	L	L	H	H
					H	L	L	X	L	H	L	L
					H	L	H	X	L	H	L	H
					H	H	L	X	L	H	H	L
					H	H	H	X	L	H	H	H
Test T_0, T_1, T_2 & T_3	H	H	H	H	L	L	L	L	L	L	L	L
					L	L	L	H	L	L	L	H
					L	L	H	L	L	L	H	L
					L	L	H	H	L	L	H	H
					L	H	L	L	L	H	L	L
					L	H	L	H	L	H	L	H
					L	H	H	L	L	H	H	L
					L	H	H	H	L	H	H	H
					H	L	L	L	H	L	L	L
					H	L	L	H	H	L	L	H
					H	L	H	L	H	L	H	L
					H	L	H	H	H	L	H	H
					H	H	L	L	H	H	L	L
					H	H	L	H	H	H	L	H
					H	H	H	L	H	H	H	L
					H	H	H	H	H	H	H	H

L = LOW, H = HIGH, X = Don't care

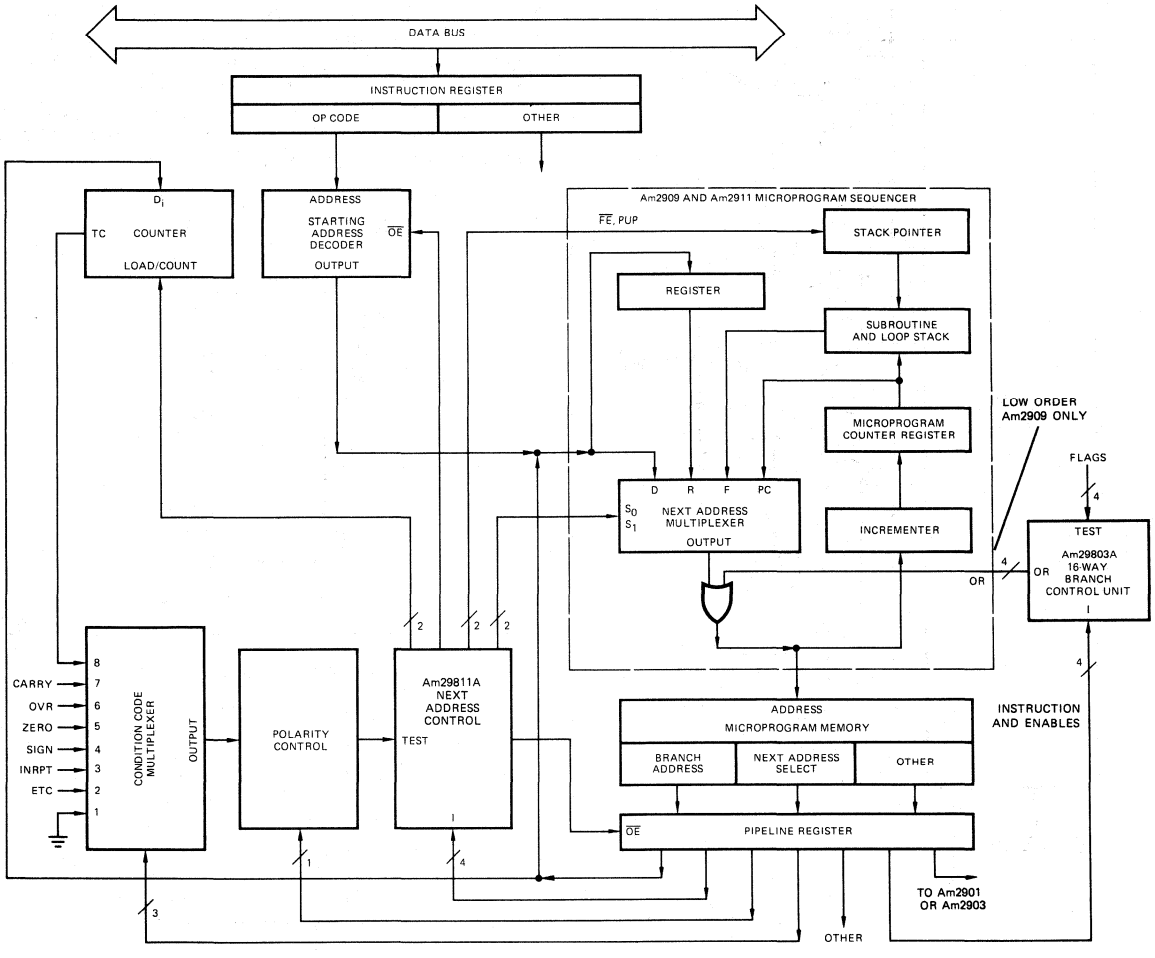
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29803APC	P-16	C	C-1
AM29803ADC	D-16	C	C-1
AM29803ADC-B	D-16	C	B-1
AM29803ADM	D-16	M	C-3
AM29803ADM-B	D-16	M	B-3
AM29803AFM	F-16	M	C-3
AM29803AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



A typical computer control unit using the Am2909, Am2911, Am29803A and Am29811A. Note that the least significant microprogram sequencer is an Am2909 and the more significant sequencers are Am2911's.

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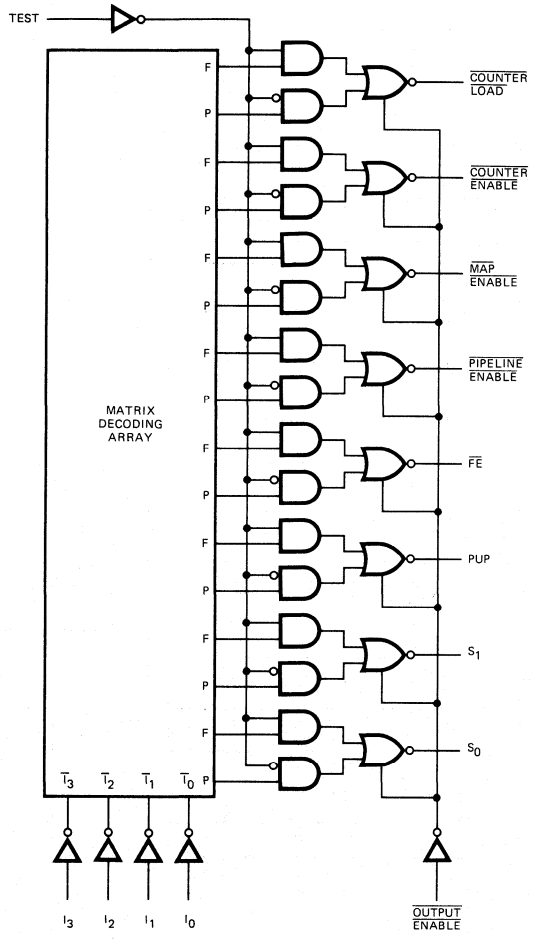
Am29811A
Next Address Control Unit

DISTINCTIVE CHARACTERISTICS

- Next address control unit for the Am2911 Microprogram Sequencer
- 16 next address instructions
- Test input for conditional instructions
- Separate outputs to control the Am2911, an independent event counter, and a mapping PROM/branch address interface
- Advanced Low-Power Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883

LOGIC DIAGRAM



P = Pass
F = Fail

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FUNCTIONAL CHARACTERISTICS

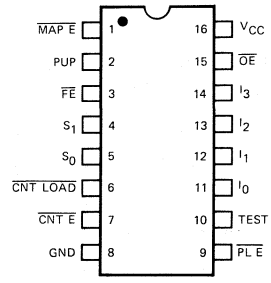
The Am29811A is a Low-Power Schottky device designed specifically for next address control of the Am2911 Microprogram Sequencer. The device contains all outputs required to control a high-performance computer control unit or a structured state machine design using microprogramming techniques.

Sixteen instructions are available by using a four-bit instruction field $I_{0\text{-}3}$. In addition, a test input is available such that conditional instructions can be performed based on a condition code test input.

The full instruction set consists of such functions as conditional jumps, conditional jump-to-subroutine, conditional return-from-subroutine, conditional repeat loops, conditional branch to starting address, and so forth.

One Am29811A can be used to control any number of Am2911 Microprogram Sequencers. The Am2911 Sequencer is a four-bit slice itself. Thus, one Am29811A Next Address Control Unit and three Am2911 Microprogram Sequencers can be used to build the most powerful, state-of-the-art, microprogram sequencer capable of controlling 4k words of microprogram memory.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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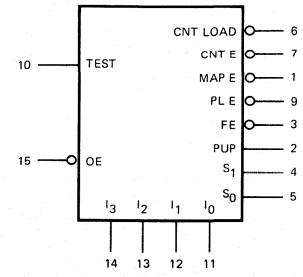
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)	
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29811ADC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29811ADM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

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SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} / t_{PHL}	I_i to Any Output	C_L = 15 pF, R_L = 2.0 kΩ		25	35	ns
t_{PLH} / t_{PHL}	Test to Any Output			25	35	ns
t_{ZH} / t_{ZL}	$\overline{OE}$ to Any Output			15	20	ns
t_{HZ} / t_{LZ}	$\overline{OE}$ to Any Output	C_L = 5.0 pF, R_L = 2.0 kΩ		15	20	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	COM'L T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5% Min.	COM'L Max.	MIL T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10% Min.	MIL Max.	Units
t_{PLH} / t_{PHL}	I_i to Any Output	C_L = 15 pF, R_L = 2.0 kΩ		40		50	ns
t_{PLH} / t_{PHL}	Test to Any Output			40		50	ns
t_{ZH} / t_{ZL}	$\overline{OE}$ to Any Output			25		30	ns
t_{HZ} / t_{LZ}	$\overline{OE}$ to Any Output			25		30	ns

DEFINITION OF FUNCTIONAL TERMS

I_0, I_1, I_2, I_3 The four instruction inputs to the Am29811A.

TEST The condition code input to the device. When the test input is LOW, the device assumes the test has failed. When the test input is HIGH, the device assumes the condition code required has been met; the test has passed.

$\overline{\text{Counter Load}}$ This output is used to drive the parallel load input of an Am25LS169 up/down counter.

$\overline{\text{Counter Enable}}$ This output is used to drive the counter enable input of an Am25LS169 up/down counter.

$\overline{\text{Map Enable}}$ This output is used to control the three-state outputs of the mapping PROM or PLA used to provide the initial starting address for each machine instruction.

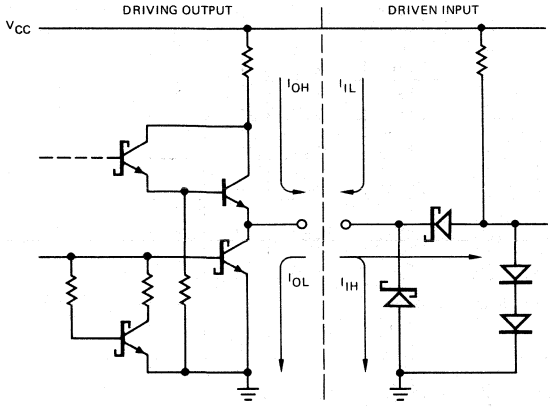
$\overline{\text{Pipeline Enable}}$ This output is used to control the three-state output of the pipeline register (Am2918) containing the branch address for the computer control unit.

$\overline{\text{FE}}$ File Enable This output is used to drive the file enable input of the Am2911. When the file enable output is LOW, a stack operation will take place.

PUP Push/Pop. The PUP output is used to drive the push/pop input of the Am2911 Microprogram Sequencer. When the PUP output is HIGH, a push will take place when the file is enabled. When the PUP output is LOW, a pop will take place when the file is enabled.

S_0, S_1 These two outputs are used to drive the S_0 and S_1 inputs to the Am2911 Microprogram Sequencer. These outputs control whether the direct input, the register, the microprogram counter, or the stack is selected as the source of the next address for the microprogram memory.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	$\overline{\text{MAP E}}$	–	100	44	44
2	PUP	–	100	44	44
3	$\overline{\text{FE}}$	–	100	44	44
4	S_1	–	100	44	44
5	S_0	–	100	44	44
6	$\overline{\text{CNT LOAD}}$	–	100	44	44
7	$\overline{\text{CNT E}}$	–	100	44	44
8	GND	–	–	–	–
9	$\overline{\text{PL E}}$	–	100	44	44
10	TEST	0.5	–	–	–
11	I_0	0.5	–	–	–
12	I_1	0.5	–	–	–
13	I_2	0.5	–	–	–
14	I_3	0.5	–	–	–
15	$\overline{\text{OE}}$	–	100	44	44
16	V_{CC}	–	–	–	–

INSTRUCTION TABLE

MNEMONIC	I_3 I_2 I_1 I_0	INSTRUCTION
JZ	L L L L	Jump to Address Zero
CJS	L L L H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register.
JMAP	L L H L	Jump to Address at Mapping PROM Output.
CJP	L L H H	Conditional Jump to Address in Pipeline Register
PUSH	L H L L	Push Stack and Conditionally Load Counter
JSRP	L H L H	Jump-to-Subroutine with Starting Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
CJV	L H H L	Conditional Jump to Vector Address.
JRP	L H H H	Jump to Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
RFCT	H L L L	Repeat Loop if Counter is not Equal to Zero.
RPCT	H L L H	Repeat Pipeline Address if Counter is not Equal to Zero.
CRTN	H L H L	Conditional Return-from-Subroutine.
CJPP	H L H H	Conditional Jump to Pipeline Address and Pop Stack.
LDCT	H H L L	Load Counter and Continue.
LOOP	H H L H	Test End of Loop.
CONT	H H H L	Continue to Next Address.
JP	H H H H	Jump to Pipeline Register Address.

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Am29811A FUNCTION TABLE

MNEMONIC	INPUTS				OUTPUTS				
	INSTRUCTION I_3 I_2 I_1 I_0	FUNCTION	TEST INPUT	NEXT ADDR SOURCE	FILE	COUNTER	MAP-E	PL-E
JZ	L L L L	JUMP ZERO	X	D	HOLD	LL*	H	L
CJS	L L L H	COND JSB PL	L	PC	HOLD	HOLD	H	L
			H	D	PUSH	HOLD	H	L
JMAP	L L H L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L L H H	COND JUMP PL	L	PC	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
PUSH	L H L L	PUSH/COND LD CNTR	L	PC	PUSH	HOLD	H	L
			H	PC	PUSH	LOAD	H	L
JSRP	L H L H	COND JSB R/PL	L	R	PUSH	HOLD	H	L
			H	D	PUSH	HOLD	H	L
CJV	L H H L	COND JUMP VECTOR	L	PC	HOLD	HOLD	H	H
			H	D	HOLD	HOLD	H	H
JRP	L H H H	COND JUMP R/PL	L	R	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
RFCT	H L L L	REPEAT LOOP, CNTR ≠ 0	L	F	HOLD	DEC	H	L
			H	PC	POP	HOLD	H	L
RPCT	H L L H	REPEAT PL, CNTR ≠ 0	L	D	HOLD	DEC	H	L
			H	PC	HOLD	HOLD	H	L
CRTN	H L H L	COND RTN	L	PC	HOLD	HOLD	H	L
			H	F	POP	HOLD	H	L
CJPP	H L H H	COND JUMP PL & POP	L	PC	HOLD	HOLD	H	L
			H	D	POP	HOLD	H	L
LDCT	H H L L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H H L H	TEST END LOOP	L	F	HOLD	HOLD	H	L
			H	PC	POP	HOLD	H	L
CONT	H H H L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H H H H	JUMP PL	X	D	HOLD	HOLD	H	L

L = LOW
H = HIGH
X = Don't Care

DEC = Decrement
*LL = Special Case

Am29811A TRUTH TABLE

MNEMONIC	FUNCTION	INPUTS					OUTPUTS							
							NEXT ADDR SOURCE		FILE		COUNTER		$\overline{MAP E}$	$\overline{PL E}$
		I_3	I_2	I_1	I_0	TEST	S_1	S_0	$\overline{FE}$	PUP	$\overline{LOAD}$	$\overline{EN}$		
	PIN NO.	14	13	12	11	10	4	5	3	2	6	7	1	9
JZ	JUMP ZERO	L	L	L	L	L	H	H	H	H	L	L	H	L
		L	L	L	L	H	H	H	H	H	L	L	H	L
CJS	COND JSB PL	L	L	L	H	L	L	L	H	H	H	H	H	L
		L	L	L	H	H	H	H	L	H	H	H	H	L
JMAP	JUMP MAP	L	L	H	L	L	H	H	H	H	H	H	L	H
		L	L	H	L	H	H	H	H	H	H	H	L	H
CJP	COND JUMP PL	L	L	H	H	L	L	L	H	H	H	H	H	L
		L	L	H	H	H	H	H	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR	L	H	L	L	L	L	L	L	H	H	H	H	L
		L	H	L	L	H	L	L	L	H	L	H	H	L
JSRP	COND JSB R/PL	L	H	L	H	L	L	H	L	H	H	H	H	L
		L	H	L	H	H	H	H	L	H	H	H	H	L
CJV	COND JUMP VECTOR	L	H	H	L	L	L	L	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	H	H	H
JRP	COND JUMP R/PL	L	H	H	H	L	L	H	H	H	H	H	H	L
		L	H	H	H	H	H	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR ≠ 0	H	L	L	L	L	H	L	H	L	H	L	H	L
		H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR ≠ 0	H	L	L	H	L	H	H	H	H	H	L	H	L
		H	L	L	H	H	L	L	H	H	H	H	H	L
CRTN	COND RTN	H	L	H	L	L	L	L	H	L	H	H	H	L
		H	L	H	L	H	H	L	L	L	H	H	H	L
CJPP	COND JUMP PL & POP	H	L	H	H	L	L	L	H	L	H	H	H	L
		H	L	H	H	H	H	H	L	L	H	H	H	L
LDCT	LD CNTR & CONTINUE	H	H	L	L	L	L	L	H	H	L	H	H	L
		H	H	L	L	H	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP	H	H	L	H	L	H	L	H	L	H	H	H	L
		H	H	L	H	H	L	L	L	L	H	H	H	L
CONT	CONTINUE	H	H	H	L	L	L	L	H	H	H	H	H	L
		H	H	H	L	H	L	L	H	H	H	H	H	L
JP	JUMP PL	H	H	H	H	L	H	H	H	H	H	H	H	L
		H	H	H	H	H	H	H	H	H	H	H	H	L

L = LOW
H = HIGH

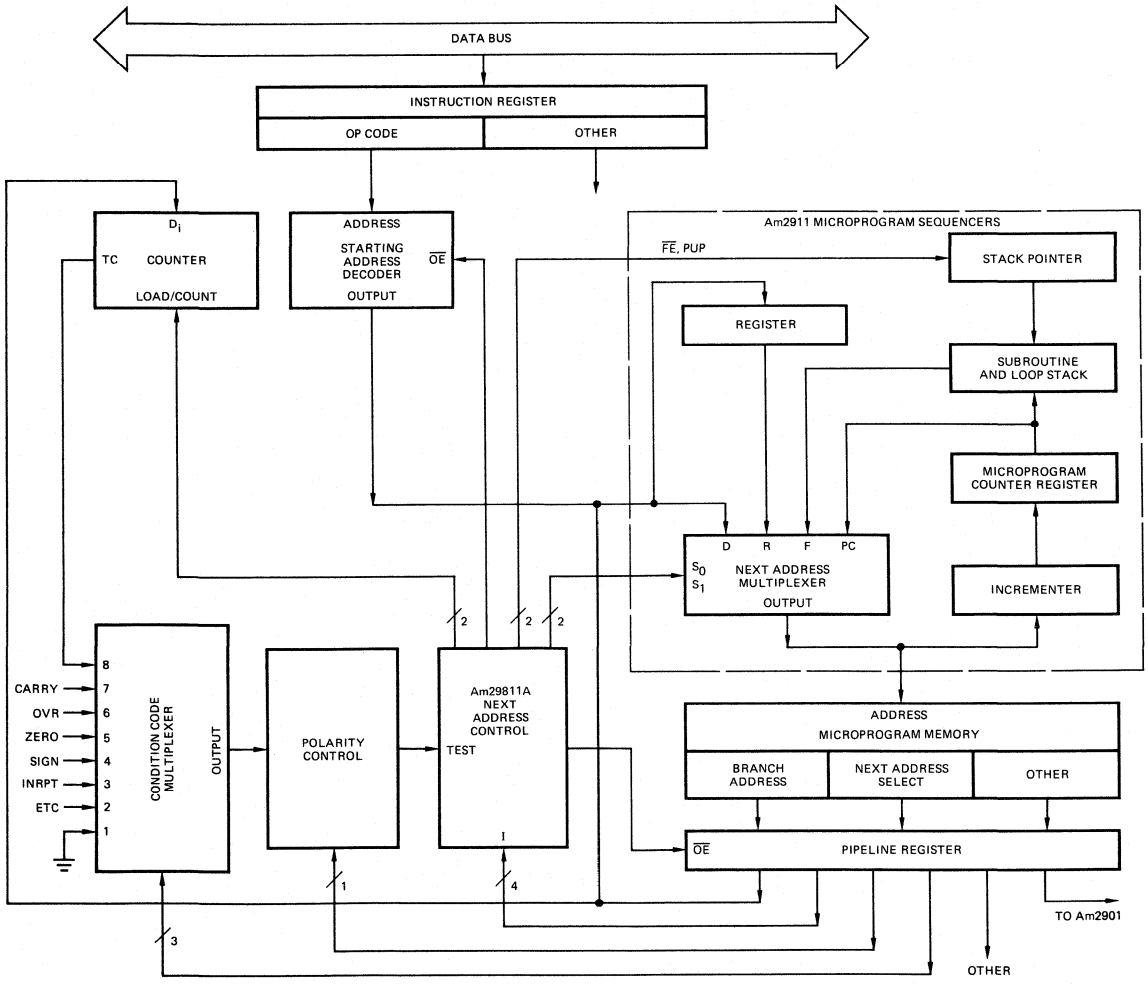
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29811APC	P-16	C	C-1
AM29811ADC	D-16	C	C-1
AM29811ADC-B	D-16	C	B-1
AM29811ADM	D-16	M	C-3
AM29811ADM-B	D-16	M	B-3
AM29811AFM	F-16	M	C-3
AM29811AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



A Typical Computer Control Unit Using the Am2911 and Am29811A.

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10

Am2900 FAMILY DESIGN AIDS INDEX

Am2900 Family Applications Literature

Bit Slice Design: Controllers and ALUs, White D.E.,
Garland STPM Press, N.Y. © 1981
May be ordered directly from
Advanced Micro Devices,
Customer Education Center,
490-A Lakeside Drive
Sunnyvale, Ca. 94086
Price: $24.50 + Tax + Shipping
ISBN 0-8240-7103-4

This book provides the inexperienced bit-slice design engineer with an easily understood description of how a computer control unit and ALU is built with the fundamental Am2900 devices (Am2901B, Am2909/11, Am2903, Am2910 and Am2914). This book forms the basis of the introductory bit-slice design course (ED2900A) at the AMD Customer Education Center.

Bit Slice Microprocessor Design, Mick and Brick,
McGraw-Hill Publishing Co.
1221 Avenue of the Americas
New York, N.Y. 10020
Price: $18.50 + Tax + Shipping
ISBN 0-07-041781-4
or from
Advanced Micro Devices
Customer Education Center
490-A Lakeside Drive M/S 71
Sunnyvale, CA. 94086

This comprehensive book discusses in detail the design of a microprogrammed computer using the Am2900 Family for the more experienced bit-slice designer. The book also includes sections on DMA design with the Am2940/Am2942 and Program Control Unit design with the Am2930/Am2932. The books chapters are:

I – Computer Architecture
II – Microprogrammed Design
III – The Data Path
IV – The Data Path, Part Two
V – Program Control Unit
VI – Interrupt
VII – Direct Memory Access
VIII – The Hex 29
IX – The Super Sixteen

ED2900A Study Guide,
may be ordered from
AMD Customer Education Center,
490-A Lakeside Drive M/S 71
Sunnyvale, Ca. 94086
Price: $18.00

This study guide is used in conjunction with the ED2900A course and complements Bit-Slice Design: Controllers and ALUs. The study guide contains example design problems, exercises and example AMSYS®29 programs.

A High Performance Disc Controller

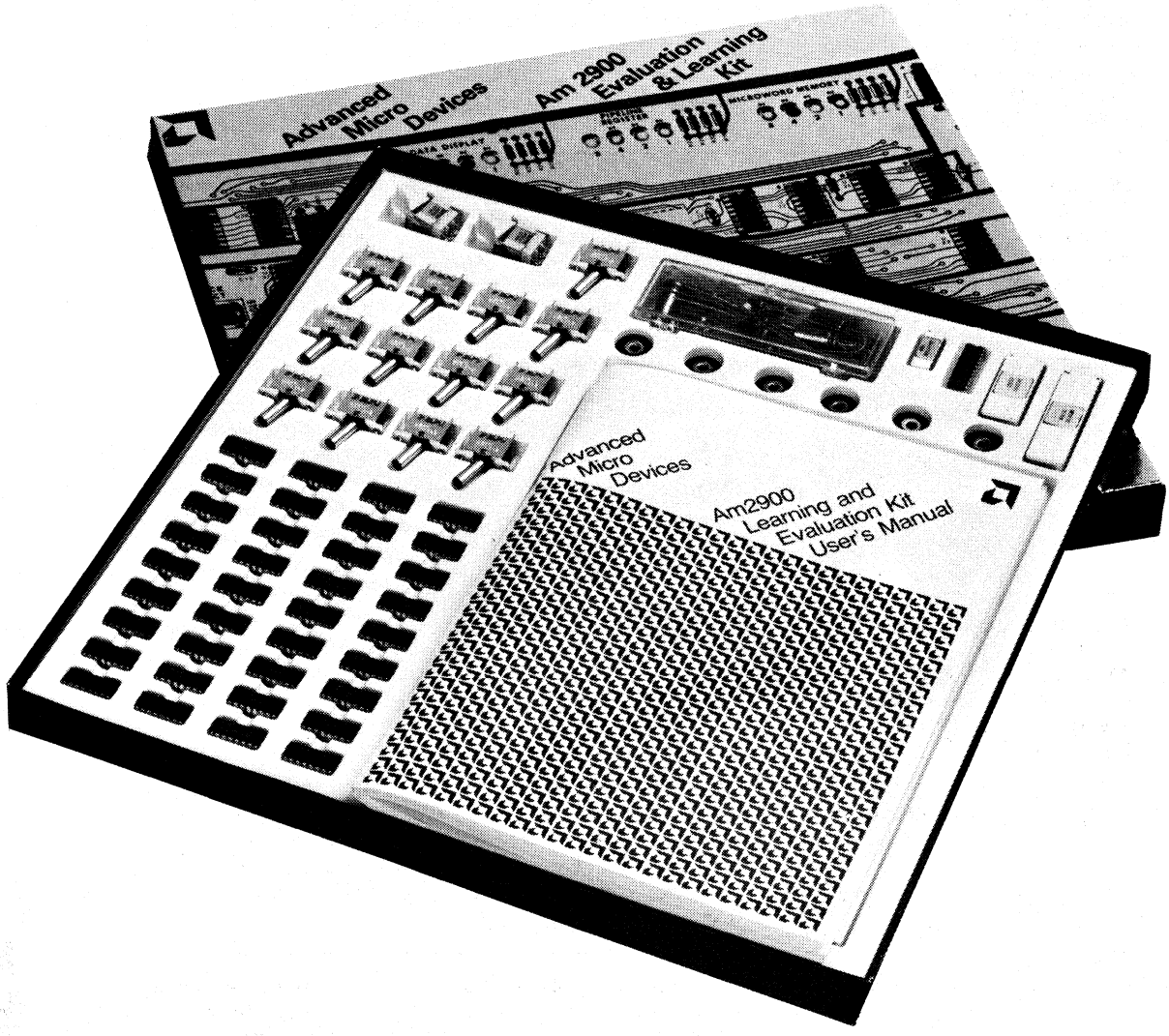
This application note covers the detailed design of a controller. Specifically it is an interface between a Pertec disc and a DEC PDP-11® minicomputer. Most controllers will be architecturally similar. Includes schematics and microcode.
Order AM-PUB065 Free

An Emulation of the Am9080A

This application note describes an Am2900 based system which executes instructions of the Am9080A MOS microprocessor. It operates about 4 times faster than the Am9080A and leaves space for user defined instructions in addition to the standard instruction set.
Order AM-PUB064 Free

Microprogram Design with the Am2900 Family

A discussion of the "instruction-cracking" problem in micro-programmed machines. Discusses ways to translate op codes into microprogram addresses and control lines.
Order AM-PUB069 Free


Advanced
Micro
Devices
Am 2900
Evaluation
& Learning
Kit
Advanced
Micro
Devices
Am2900
Learning and
Evaluation Kit
User's Manual

THE Am2900 EVALUATION AND LEARNING KIT

Pictured at the left is the Am2900 Evaluation Kit. The system consists of a microprogrammed control unit which controls all the inputs to an Am2901 microprocessor slice. Thirty-two bit microinstructions are entered into a RAM in the control unit using the switch register. Each microinstruction contains bits to control the Am2901A's A and B addresses, instruction, carry in, and data input. Additional bits in the microinstruction control an Am2909 sequencer which generates the addresses for the microprogram memory. Once entered, microinstructions may be executed using a single step clock or using a pulse generator. The LED display provides access to nearly every signal path in the system.

Sixteen "sequence control" instructions are available, including execute, branch conditional, jump-to-subroutine, return, and loop. Because the set of sequence instructions is implemented in a PROM, the user can devise his own set of operations by programming a new PROM.

The kit is supplied with 40 IC's, all resistors, capacitors, LED's and switches, the PC board, and a manual containing assembly instructions, theory and a set of exercises. The user need only solder the components in place and attach a 5 V power supply (2.0 ampere rating).

Working with the kit, the user will gain familiarity with a high performance pipelined microprogrammed architecture, and with the operation of the Am2909 and Am2901A. By driving the kit from a pulse generator, the user can observe the operation of the components in real time, executing real instructions.

The part number for this kit is Am2900K1.

School of Advanced Engineering

BIPOLAR APPLICATION DESIGN COURSES

AMD's School of Advanced Engineering offers graduate-level instruction in designing with the newest technologies. Bipolar design courses take you from the basics of bit-slice architecture through basic design with the 2900 Family on to the microprogram development system and its application to your design and finally to emulation and CPU architecture where students create microcode to drive an actual system, using the writable control store of the AmSYS29 development system.

For More Information:

Contact your AMD Sales Representative or write to:

Advanced Micro Devices
School of Advanced Engineering
Customer Education Center
490-A Lakeside Drive
P.O. Box 453
Sunnyvale, California 94086 U.S.A.

AmSYS®29
Microprogram Development System

AmSYS29, from Advanced Micro Computers, is the proven system for developing microprogrammed machines. It greatly simplifies the speed of developing and integrating software and hardware for Am2900 based microprogrammed machines. AmSYS29 supports 2901/03 based CPU designs, 29116 based controller designs and 295XX based signal processing designs.

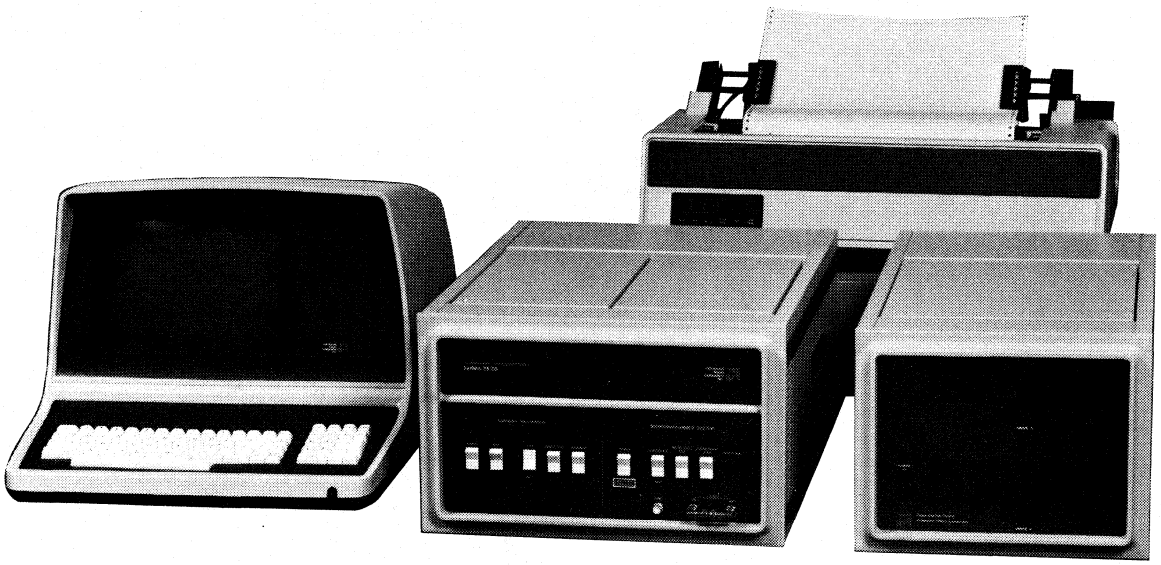
A microcode assembly language of your specifications is implemented through AMDASM™. You can then write the microprogram in your symbolic language and assemble the source file with AMDASM.

The Control Store Emulator contains a high-speed Writable Control Store to replace microprogram PROM during development. Your microsequencer address accesses a block of microcode in WCS RAM that can be mapped anywhere in your target system memory.

Emulator Control Logic controls the target system clock providing single-step and full speed control with multiple breakpoints. Monitor points provide measurements of the target system logic state during hardware debug.

Microprogram support software moves microcode object files out to Writable Control Store and saves working programs on to disk. DDT29 procedure interfaces the system console to the Control Store Emulator providing clock control, breakpoint setting, microprogram address control, logic state tracing and microcode editing.

AmSYS29 provides complete software and hardware support for the development of any microprogrammed system.



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Logic and Interface Index

Note 1: See AmZ8000 Family Data Book

Am3448A

IEEE-488 Quad Bidirectional Transceiver

DISTINCTIVE CHARACTERISTICS

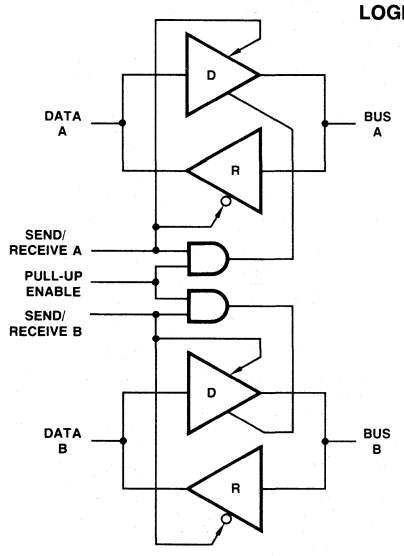
- Four independent driver/receiver pairs
- Three-state outputs
- High impedance inputs
- Receiver hysteresis – 600mV (Typ.)
- Fast Propagation Times – 15-20ns (Typ.)
- TTL compatible receiver outputs
- Single +5 volt supply
- Open collector driver output option with internal passive pull up
- Power up/power down protection (No invalid information transmitted to bus)
- No bus loading when power is removed from device
- Required termination characteristics provided
- Advanced Schottky processing
- 100% product assurance screening to MIL-STD-883 requirements

GENERAL DESCRIPTION

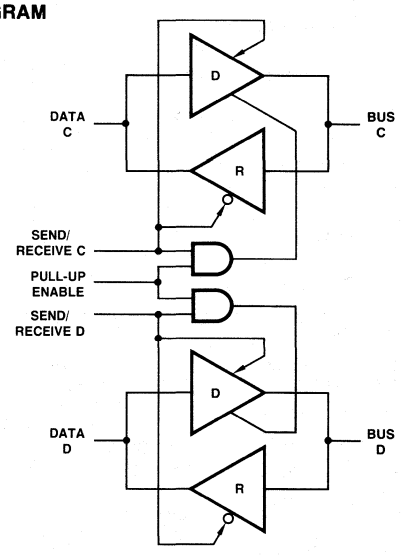
The Am3448A is a quad bidirectional transceiver meeting the requirement of IEEE-488 standard digital interface for programmable instrumentation for the driver, receiver, and composite device load. One pull-up enable input is provided for each pair of transceivers which controls the operating mode of the driver outputs as either an open collector or active pull-up configuration.

The receivers feature input hysteresis for improved noise immunity in system applications. The device bus (receiver input) changes from standard bus loading to a high impedance load when power is removed. In addition no spurious noise is generated on the bus during power-up or power-down.

LOGIC DIAGRAM



LIC-446

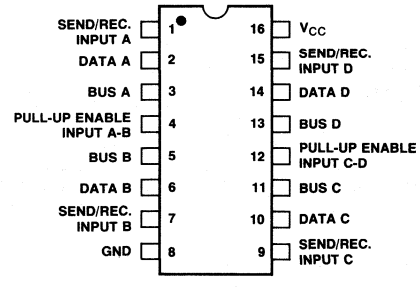


LIC-447

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	MC3448AL
Molded DIP	0°C to +70°C	MC3448AP
Dice	0°C to +70°C	AM3448AX

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-448

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ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Driver Output Current	150mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am3448A T_A = 0°C to 70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
Bus Characteristics							
$V_{(BUS)}$	Bus Voltage	Bus Pin Open, $V_{I(S/R)}$ = 0.8V		2.75		3.7	Volts
$V_{IC(BUS)}$		$I_{(BUS)}$ = −12mA				−1.5	
$I_{(BUS)}$	Bus Current	5.0V ≤ $V_{(BUS)}$ ≤ 5.5V		0.7		2.5	mA
		$V_{(BUS)}$ = 0.5V		−1.3		−3.2	
		V_{CC} = 0V, 0V ≤ $V_{(BUS)}$ ≤ 2.75V				0.04	
Driver Characteristics							
$V_{IC(D)}$	Driver Input Clamp Voltage	$V_{I(S/R)}$ = 2.0V, $I_{IC(D)}$ = −18mA				−1.5	Volts
$V_{OH(D)}$	Driver Output Voltage − High Logic State	$V_{I(S/R)}$ = 2.0V, $V_{IH(D)}$ = 2.0V, $V_{IH(E)}$ = 2.0V, I_{OH} = −5.2mA		2.5			Volts
$V_{OL(D)}$	Driver Output Voltage − Low Logic State	$V_{I(S/R)}$ = 2.0V, $I_{OL(D)}$ = 48mA				0.5	Volts
$I_{OS(D)}$	Output Short Circuit Current	$V_{I(S/R)}$ = 2.0V, $V_{IH(D)}$ = 2.0V $V_{IH(E)}$ = 2.0V		−30		−120	mA
$V_{IH(D)}$	Driver Input Voltage − High Logic State	$V_{I(S/R)}$ = 2.0V		2.0			Volts
$V_{IL(D)}$	Driver Input Voltage − Low Logic State	$V_{I(S/R)}$ = 2.0V				0.8	Volts
$I_{I(D)}$	Driver Input Current − Data Pins	$V_{I(S/R)}$ = $V_{I(E)}$ = 2.0V	0.5 ≤ $V_{I(D)}$ ≤ 2.7V	−200		40	μA
$I_{IB(D)}$			$V_{I(D)}$ = 5.5V			200	
Receiver Characteristics							
$V_{HYS(R)}$	Receiver Input Hysteresis	$V_{I(S/R)}$ = 0.8V		400	600		mV
$V_{ILH(R)}$	Receiver Input Threshold	$V_{I(S/R)}$ = 0.8V, Low to High			1.6	1.8	Volts
$V_{IHL(R)}$		$V_{I(S/R)}$ = 0.8V, High to Low		0.8	1.0		
$V_{OH(R)}$	Receiver Output Voltage − High Logic State	$V_{I(S/R)}$ = 0.8V, $I_{OH(R)}$ = −800μA, $V_{(BUS)}$ = 2.0V		2.7			Volts
$V_{OL(R)}$	Receiver Output Voltage − Low Logic State	$V_{I(S/R)}$ = 0.8V, $I_{OL(R)}$ = 16mA, $V_{(BUS)}$ = 0.8V				0.5	Volts
$I_{OS(R)}$	Receiver Output Short Circuit Current	$V_{I(S/R)}$ = 0.8V, $V_{(BUS)}$ = 2.0V		−15		−75	mA
Enable, Send/Receive Characteristics							
$I_{I(S/R)}$	Input Current − Send/Receive	0.5 ≤ $V_{I(S/R)}$ ≤ 2.7V		−100		20	μA
$I_{IB(S/R)}$		$V_{I(S/R)}$ = 5.5V				100	
$I_{I(E)}$	Input Current − Enable	0.5 ≤ $V_{I(E)}$ ≤ 2.7V		−200		20	μA
$I_{IB(E)}$		$V_{I(E)}$ = 5.5V				100	
Power Supply Current							
I_{CCL}	Power Supply Current	Listening Mode − All Receivers On			63	85	mA
I_{CCH}		Talking Mode − All Drivers On			106	125	

Note 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C unless otherwise noted)

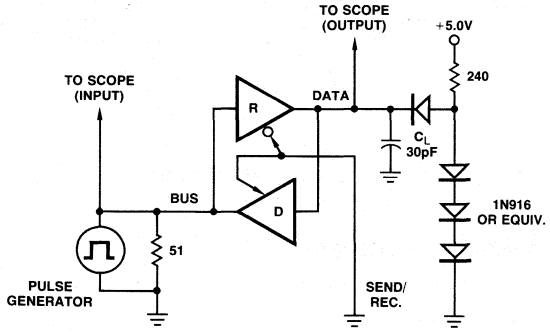
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{PLH(D)}$	Propagation Delay of Driver (Fig. 2)	Output Low to High	–		15	ns
$t_{PHL(D)}$		Output High to Low			17	
$t_{PLH(R)}$	Propagation Delay of Receiver (Fig. 1)	Output Low to High	–		25	ns
$t_{PHL(R)}$		Output High to Low	–		23	
$t_{PHZ(R)}$	Propagation Delay Time – Send/Receiver to Data (Fig. 4)	Logic High to Third State	–		30	ns
$t_{PZH(R)}$		Third State to Logic High	–		30	
$t_{PLZ(R)}$		Logic Low to Third State	–		30	
$t_{PZL(R)}$		Third State to Logic Low			30	
$t_{PHZ(D)}$	Propagation Delay Time – Send/Receiver to Bus (Fig. 3)	Logic High to Third State	–		30	ns
$t_{PZH(D)}$		Third State to Logic High	–		30	
$t_{PLZ(D)}$		Logic Low to Third State	–		30	
$t_{PZL(D)}$		Third State to Logic Low			30	
$t_{POFF(E)}$	Turn-On Time – Enable to Bus (Fig. 5)	Pull-Up Enable to Open Collector	–		30	ns
$t_{PON(E)}$		Open Collector to Pull-Up Enable	–		20	

TRUTH TABLE

Send/Rec.	Enable	Into Flow	Comments
0	X	Bus → Data	
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Collector

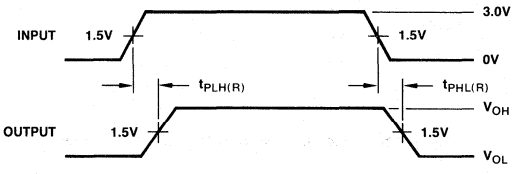
X = Don't Care

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS



*Includes Jig and Probe Capacitance.

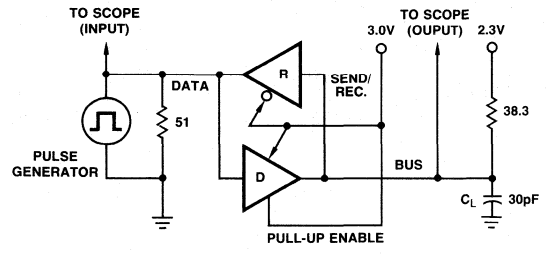
LIC-449



f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

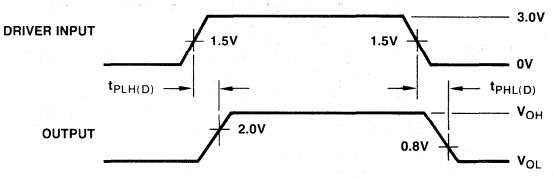
LIC-450

Figure 1. Bus Input to Data Output (Receiver).



*Includes Jig and Probe Capacitance.

LIC-451



f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

LIC-452

Figure 2. Data Input to Bus Output (Driver).

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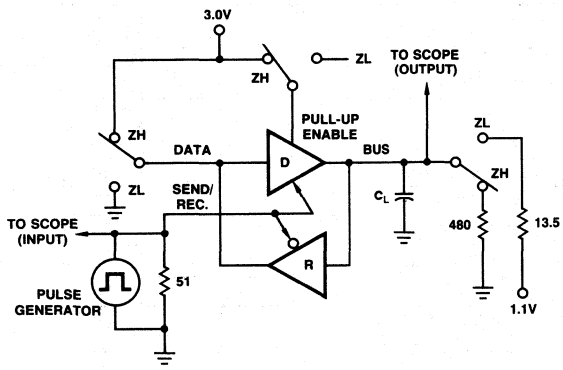
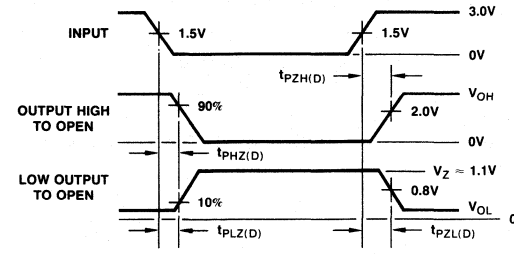
PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)



C_L = 15pF (Includes Jig and Probe Capacitance)

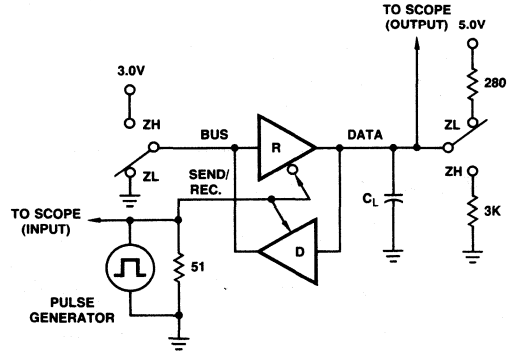
LIC-453



f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

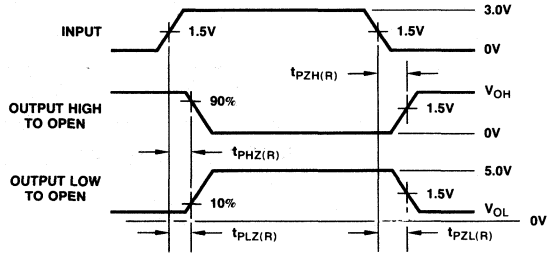
LIC-454

Figure 3. Send/Receive Input to Bus Output (Driver).



C_L = 15pF (Includes Jig and Probe Capacitance)

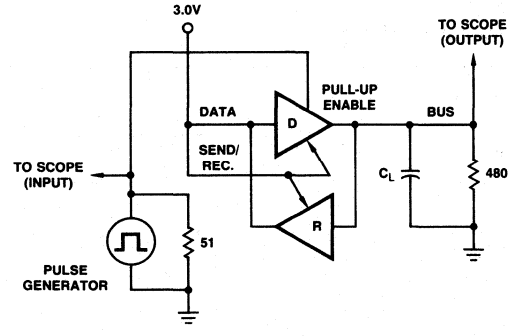
LIC-455



f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

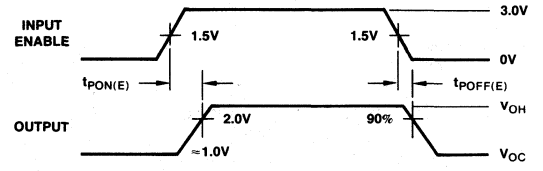
LIC-456

Figure 4. Send/Receive Input to Data Output (Receiver).



C_L = 15pF (Includes Jig and Probe Capacitance)

LIC-457



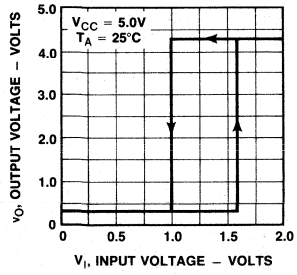
f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

LIC-458

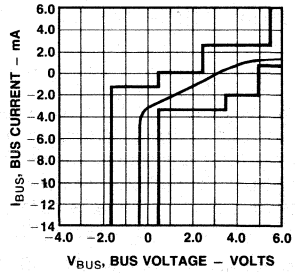
Figure 5. Enable Input to Bus Output (Driver).

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)

TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

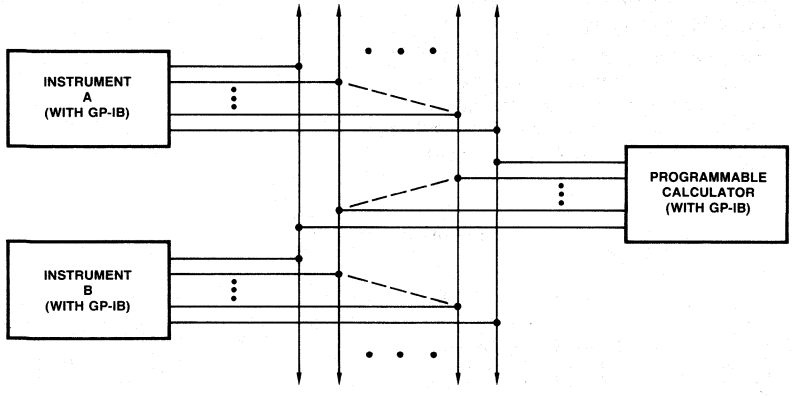


TYPICAL BUS LOAD LINE



LIC-459

TYPICAL APPLICATION

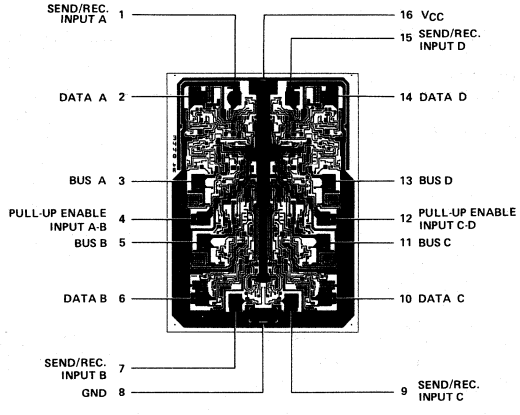


16 LINES TOTAL
(FOUR Am3448A'S FOR EACH BUS INTERFACE)

LIC-460

TYPICAL MEASUREMENT SYSTEM APPLICATION

Metallization and Pad Layout



DIE SIZE .063" X .087"

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Am54S/74S160 • Am54S/74S161 • Am54S/74S163

BCD Decade/Four-Bit Binary Counters

Distinctive Characteristics

- Fully synchronous counting
- Fully synchronous parallel loading
- Edge-triggered clock action
- Advanced Schottky technology
- 100% MIL-STD-883 reliability assurance testin

FUNCTIONAL DESCRIPTION

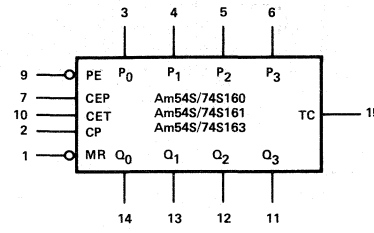
The Am54S/74S160 is a fully synchronous 4-bit decimal counter. The Am54S/74S161 and Am54S/74S163 are fully synchronous 4-bit binary counters. With the parallel enable ($\overline{PE}$) LOW, data on the P_0-P_3 inputs is parallel loaded on the positive clock transition. When $\overline{PE}$ is HIGH and both count enables CEP and CET are also HIGH, counting will occur on the LOW-to-HIGH clock transition.

The terminal count state (1001 for the Am54S/74S160 and 1111 for both the Am54S/74S161 and Am54S/74S163) is decoded and ANDed with CET in the terminal count (TC) output. If CET is HIGH and the counter is in its terminal count state, then TC is HIGH.

Both the Am54S/74S160 and Am54S/74S161 have an asynchronous master reset ($\overline{MR}$). A LOW on the $\overline{MR}$ input forces the Q outputs LOW independent of all other inputs.

The Am54S/74S163 has a synchronous master reset ($\overline{MR}$). A LOW on the $\overline{MR}$ input forces the Q outputs LOW after the next clock pulse independent of all other inputs. The only requirements on the $\overline{PE}$, CEP, CET and P_0-P_3 inputs is that they meet the set-up time requirements before the clock LOW-to-HIGH transition.

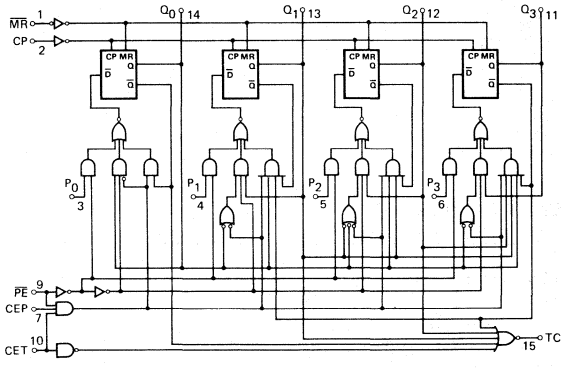
LOGIC SYMBOL



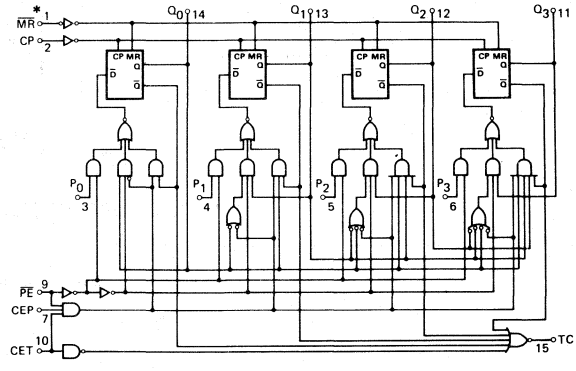
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am54S/74S160



Am54S/74S161/S163



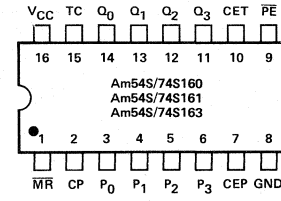
*$\overline{MR}$ is asynchronous on the Am54S/74S161 and synchronous on the Am54S/74S163

ORDERING INFORMATION

Package Type	Temperature Range	Am54S/74S160 Order Number	Am54S/74S161 Order Number	Am54S/74S163 Order Number
Molded DIP	0 to +75°C	SN74S160N	SN74S161N	SN74S163N
Hermetic DIP	0 to +75°C	SN74S160J	SN74S161J	SN74S163J
Dice	0 to +75°C	SN74S160X	SN74S161X	SN74S163X
Hermetic DIP	−55 to +125°C	SN54S160J	SN54S161J	SN54S163J
Hermetic Flat Pak	−55 to +125°C	SN54S160W	SN54S161W	SN54S163W
Dice	−55 to +125°C	SN54S160X	SN54S161X	SN54S163X

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

AXIMUM RATINGS (Above which the useful life may be impaired)

orage Temperature	−65°C to +150°C
mperature (Ambient) Under Bias	−55°C to +125°C
pply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
C Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
C Input Voltage	−0.5V to +5.5V
C Output Current, Into Outputs	30mA
C Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

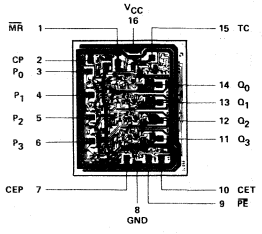
Am74S160X, Am74S161X, Am74S163	T_A = 0 to +75°C	V_{CC} = 5.0V ± 5% (COM'L)	MIN = 4.75V	MAX = 5.25V
Am54S160X, Am54S161X, Am54S163	T_A = −55 to +125°C	V_{CC} = 5.0V ± 10% (MIL)	MIN = 4.5V	MAX = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −1mA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}			0.35	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	P; MR; CEP			−2.0	mA
			CET			−3.0	
			$\overline{PE}$			−4.0	
			CP			−5.0	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	P; $\overline{MR}$; CEP			50	μA
			CET			75	
			$\overline{PE}$			100	
			CP			125	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX		−40	−65	−100	mA
I_{CC}	Power Supply Current Am54S/74S160/161 only	V_{CC} = MAX (Note 5)			82	127	mA
	Am54S/74S163 only	V_{CC} = MAX (Note 6)			96	150	mA

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; $\overline{MR}$ = 0V; all other inputs HIGH.
6. Outputs open; $\overline{MR}$, CP, CET = HIGH; all other inputs LOW.

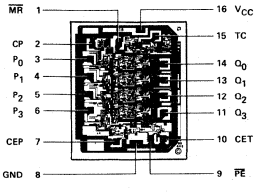
Metallization and Pad Layouts

Am54S/74S160



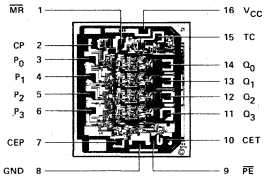
DIE SIZE 0.078" X 0.096"

Am54S/74S161



DIE SIZE 0.092" X 0.076"

Am54S/74S163



DIE SIZE 0.092" X 0.076"

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DEFINITION OF FUNCTIONAL TERMS

$\overline{PE}$ Parallel Enable. When $\overline{PE}$ is LOW, the parallel inputs, P_0 through P_3, are enabled. When $\overline{PE}$ is HIGH, the count function is possible.

CEP Count Enable Parallel. CEP is one of the count enable inputs that must be HIGH for the counter to count.

CET Count Enable Trickle. CET is one of the count enable inputs that must be HIGH for the counter to count. In addition, CET is included in the TC output gate and must be HIGH for TC to be HIGH.

CP Clock Pulse. Causes the required output change on the LOW-to-HIGH transition (Edge-triggered).

$\overline{MR}$ Master Reset (Am54S/74S160/S161). When the asynchronous master reset is LOW, the Q_0 through Q_3 outputs will be LOW regardless of the other inputs.

$\overline{MR}$ Master Reset (Am54S/74S163). When the synchronous master reset is LOW the Q_0 through Q_3 outputs will be LOW following the next clock pulse regardless of the other inputs.

P_0, P_1, P_2, P_3 The parallel data inputs for the four internal flip-flops.

Q_0, Q_1, Q_2, Q_3 The four parallel outputs from the counter.

TC Terminal Count. The terminal count output will be HIGH for CET HIGH and binary nine on the Am54S/74S160 or CET HIGH and binary 15 on the Am54S/74S161.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{MR}$	1	1	–	–
CP	2	2.5	–	–
P_0	3	1	–	–
P_1	4	1	–	–
P_2	5	1	–	–
P_3	6	1	–	–
CEP	7	1	–	–
GND	8	–	–	–
$\overline{PE}$	9	2	–	–
CET	10	1.5	–	–
Q_3	11	–	20	10
Q_2	12	–	20	10
Q_1	13	–	20	10
Q_0	14	–	20	10
TC	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

FUNCTION TABLE

DEVICE TYPE	INPUTS									OUTPUTS			
	CP	$\overline{MR}$	$\overline{PE}$	CEP	CET	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3
Am54S/74S160/S161	X	L	X	X	X	X	X	X	X	L	L	L	L
Am54S/74S163	↑	L	X	X	X	X	X	X	X	L	L	L	L
Am54S/74S160/S161/S163	↑	H	L	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
	↑	H	H	L	L	X	X	X	X	NC	NC	NC	NC
	↑	H	H	L	H	X	X	X	X	NC	NC	NC	NC
	↑	H	H	H	L	X	X	X	X	NC	NC	NC.	NC
	↑	H	H	H	H	X	X	X	X	COUNT			

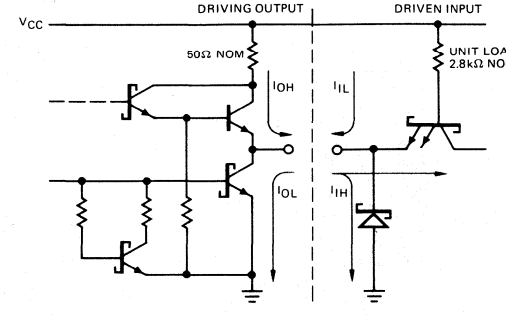
H = HIGH X = Don't Care D_i may be either HIGH or LOW
L = LOW NC = No Change ↑ LOW-to-HIGH Transition

TERMINAL COUNT (TC) TRUTH TABLE

Am54S/74S160					Am54S/74S161/163					TC
CET	Q_0	Q_1	Q_2	Q_3	CET	Q_0	Q_1	Q_2	Q_3	
H	H	L	L	H	H	H	H	H	H	H
L	X	X	X	X	L	X	X	X	X	L
X	L	X	X	X	X	L	X	X	X	L
X	X	H	X	X	X	X	L	X	X	L
X	X	X	H	X	X	X	X	L	X	L
X	X	X	X	L	X	X	X	X	L	L

H = HIGH L = LOW X = Don't Care

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



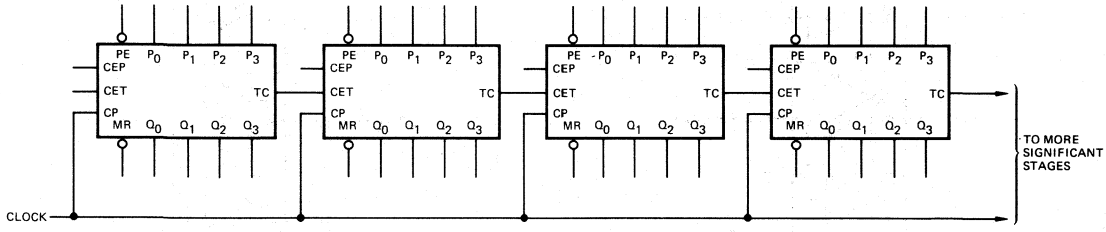
Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS (T_A = +25°)

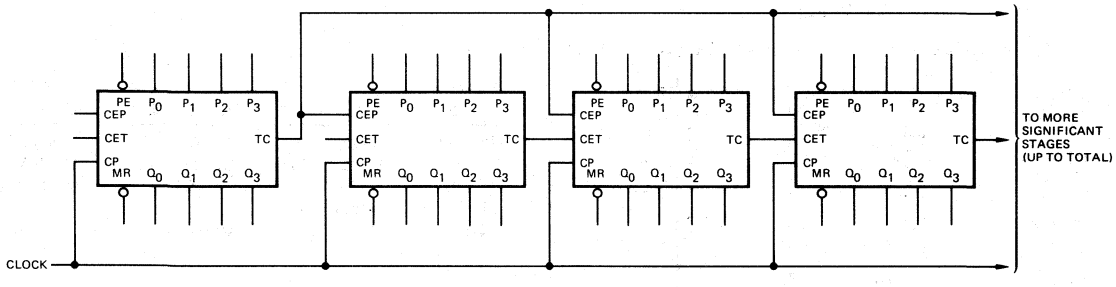
Parameters	Description	Test Conditions	Min	Typ	Max	Units
f_{MAX}	Count Frequency	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω	70	100		MHz
t_{PLH}	Clock to Q			6	9	ns
t_{PHL}				8.5	13	
t_{PLH}	Clock to TC			12	18	ns
t_{PHL}				8	12	
t_{PLH}	CET to TC			6.5	10	ns
t_{PHL}				6.5	10	
t_{PHL}	$\overline{MR}$ to Q (Am54S/74S160/161 only)			14	20	ns
t_s	Recovery Time for MR (inactive) Am54S/74S160 and Am54S/74S161 only		6			ns
t_{pw}	Master Reset Pulse Width		13			ns
t_{pw}	Clock Pulse Width HIGH		6			ns
	Clock Pulse Width LOW		10			
t_s	Data to Clock		8			ns
t_h			0			
t_s	$\overline{PE}$ to Clock		16			ns
t_h			0			
t_s	CEP or CET to Clock		12			ns
t_h			0			
t_s	$\overline{MR}$ to Clock Am54S/74S163 only		14			ns
t_h			0			

APPLICATIONS

SYNCHRONOUS MULTISTAGE COUNTING USING CET INPUT ONLY



FASTER SYNCHRONOUS MULTISTAGE COUNTING USING CET AND CEP INPUTS



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Am54S/74S242 • Am54S/74S243

Quad Bus Transceivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Advanced Schottky processing
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- V_{OL} of 0.55V at 64mA for Am74S; 48mA for Am54S
- Data-to-output propagation delay times:
  Am54S/74S242 Inverting – 7.0ns MAX
  Am54S/74S243 Noninverting – 9.0ns MAX
- Enable-to-output – 15.0ns MAX
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

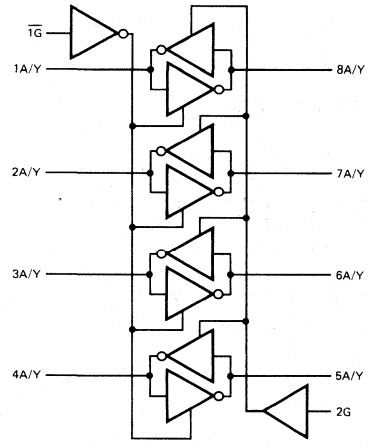
The Am54S/74S242 and Am54S/74S243 are quad bus transceivers designed for asynchronous two-way communications between data buses.

The Am54S/74S242 and Am54S/74S243 have the two 4-line data paths connected input-to-output on both sides to form an asynchronous transceiver/buffer with complementing enable inputs. The Am54S/74S242 is inverting, while the Am54S/74S243 presents noninverting data at the outputs. The outputs of the commercial temperature range versions have 64mA sink and 15mA source capability, which can be used to drive terminated lines down to 133Ω. The outputs of the military temperature range versions have 48mA sink and 12mA source current capability.

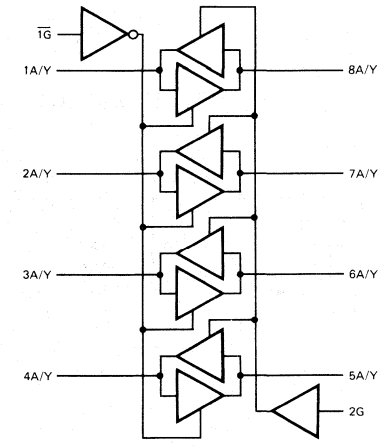
Featuring 0.2V minimum guaranteed hysteresis at each low-current PNP data input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely.

LOGIC DIAGRAMS

Am54S/74S242

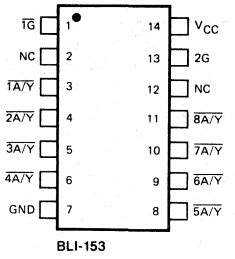


Am54S/74S243



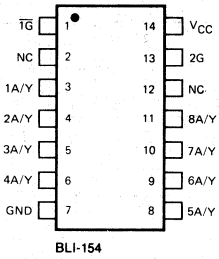
CONNECTION DIAGRAMS
Top Views

Am54S/74S242



BLI-153

Am54S/74S243



BLI-154

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Am54S/74S242 Order Number	Am54S/74S243 Order Number
Hermetic	−55 to +125°C	SN54S242J	SN54S243J
Dice	−55 to +125°C	AM54S242X	AM54S243X
Hermetic	0 to +70°C	SN74S242J	SN74S243J
Molded	0 to +70°C		
Dice	0 to +70°C	AM74S242X	AM74S243X

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am54S242/S243 (MIL) $T_A = -55$ to $+125°C$ V_{CC}(MIN.) = 4.50V V_{CC}(MAX.) = 5.50V
Am74S242/S243 (COM'L) $T_A = 0$ to $+70°C$ V_{CC}(MIN.) = 4.75V V_{CC}(MAX.) = 5.25V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{IH}	High-Level Input Voltage				2.0			Volts
V_{IL}	Low-Level Input Voltage						0.8	Volts
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., I_I = −18mA					−1.2	Volts
V_{OH}	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN.			0.2	0.4		Volts
	High-Level Output Voltage	V_{CC} = MIN., V_{IL} = 0.8V, I_{OH} = −3.0mA			2.4	3.4		Volts
		V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA		2.0			Volts
			COM'L, I_{OH} = −15mA		2.0			Volts
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN.	MIL, I_{OL} = 48mA				0.55	Volts
			COM'L, I_{OL} = 64mA				0.55	Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = 0.8V		V_O = 2.4V			50	µA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied			V_O = 0.5V			−50	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 5.5V					1.0	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} = MAX., V_{IH} = 2.7V					50	µA
I_{IL}	Low-Level Input Current	Any A	V_{CC} = MAX., V_{IL} = 0.5V				−400	µA
		Any G					−2.0	mA
I_{OS}	Short-Circuit Output Current (Note 3)	V_{CC} = MAX.			−50		−225	mA
I_{CC}	Supply Current	Am54S/74S242	All Outputs HIGH	V_{CC} = MAX. Outputs open	MIL		80	123	mA
					COM'L		80	135	mA
			All Outputs LOW		MIL		100	145	mA
					COM'L		100	150	mA
			Outputs at Hi-Z		MIL		100	145	mA
					COM'L		100	150	mA
		Am54S/74S243	All Outputs HIGH		MIL		95	147	mA
					COM'L		95	160	mA
			All Outputs LOW		MIL		120	170	mA
					COM'L		120	180	mA
			Outputs at Hi-Z		MIL		120	170	mA
					COM'L		120	180	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, $T_A = 25°$ C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, $T_A = 25°C$)

Parameter	Description	Test Conditions	Am54S/74S242 Min.	Am54S/74S242 Typ.	Am54S/74S242 Max.	Am54S/74S243 Min.	Am54S/74S243 Typ.	Am54S/74S243 Max.	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 50pF, R_L = 90Ω (Note 3)		4.5	7.0		6.0	9.0	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			4.5	7.0		6.0	9.0	ns
t_{ZL}	Output Enable Time to Low Level			10	15		10	15	ns
t_{ZH}	Output Enable Time to High Level			6.5	10		8.0	12	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0pF, R_L = 90Ω (Note 3)		10	15		10	25	ns
t_{HZ}	Output Disable Time from High Level			6.0	9.0		6.0	9.0	ns

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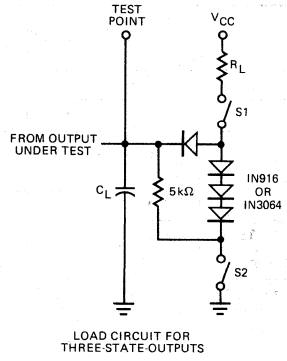
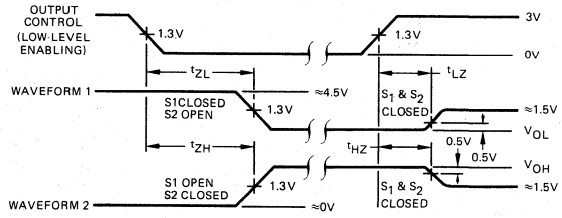
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.

FUNCTION TABLES

Am54S/74S242

CONTROL INPUTS		DATA OUTPUTS	
$\overline{1G}$	2G	A	B
H	H	$\overline{O}$	I
L	H	*	*
H	L	ISOLATED	
L	L	I	$\overline{O}$

I = Input
O = Output
$\overline{O}$ = Inverting Output
H = High
L = Low

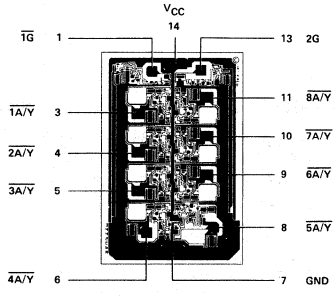
Am54S/74S243

CONTROL INPUTS		DATA OUTPUTS	
$\overline{1G}$	2G	A	B
H	H	O	I
L	H	*	*
H	L	ISOLATED	
L	L	I	O

*Possible destructive oscillation may occur if the transceivers are enabled in both directions at once.

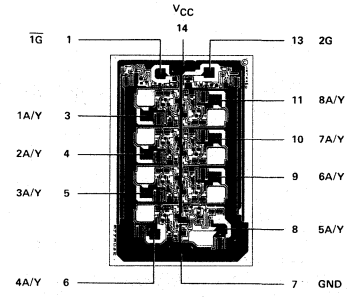
Metallization and Pad Layouts

Am54S/74S242



DIE SIZE 0.060" X 0.103"

Am54S/74S243



DIE SIZE 0.060" X 0.103"

Am71/81LS95 • Am71/81LS96
Am71/81LS97 • Am71/81LS98

Three-State Octal Buffers

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus line directly
- Typical propagation delay
  Am71/81LS95, Am71/81LS97 13ns
  Am71/81LS96, Am71/81LS98 10ns
- Typical power dissipation
  Am71/81LS95, Am71/81LS97 80mW
  Am71/81LS96, Am71/81LS98 65mW
- PNP inputs reduce DC loading on bus lines
- Am71/81LS96 and Am71/81LS98 are inverting; Am71/81LS95 and Am71/81LS97 are non-inverting
- 20-pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

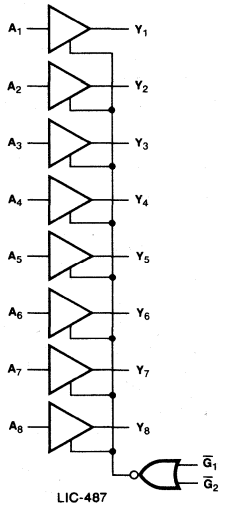
GENERAL DESCRIPTION

The Am71/81LS95, Am71/81LS96, Am71/81LS97 and Am71/81LS98 are octal buffers fabricated using Advanced Low-Power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

The Am71/81LS95 and Am71/81LS97 present true data at the outputs, while the Am71/81LS96 and Am71/81LS98 are inverting. The Am71/81LS95 and Am71/81LS96 have a common enable for all eight buffers with access through a 2-input NOR gate. The Am71/81LS97 and Am71/81LS98 octal buffers have four buffers enabled from one common line, and the other four buffers enabled from another common line. In all cases the outputs are placed in the three-state condition by applying a high logic level to the enable pins. All parts feature low current PNP inputs.

LOGIC DIAGRAMS

Am71/81LS95



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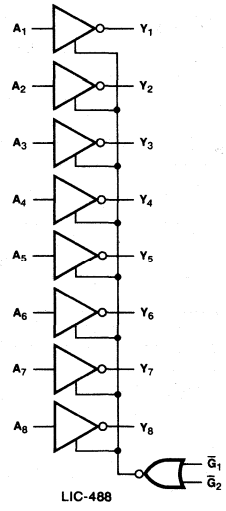
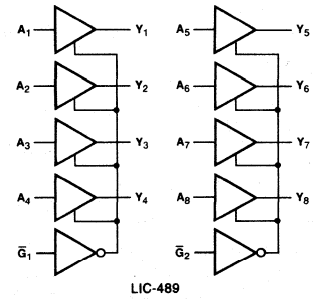
Am71/81LS96



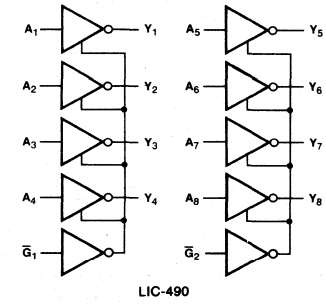
LIC-488

Am71/81LS97



LIC-489

Am71/81LS98



LIC-490

'LS95

INPUTS			OUTPUT
$\overline{G}_1$	$\overline{G}_2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

'LS96

INPUTS			OUTPUT
$\overline{G}_1$	$\overline{G}_2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

'LS97

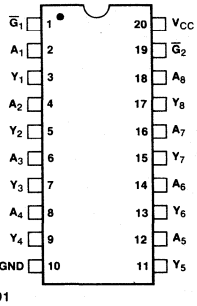
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

'LS98

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

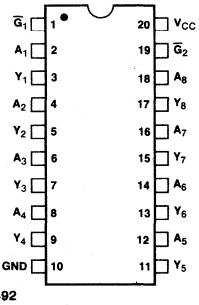
CONNECTION DIAGRAMS – Top Views

Am71/81LS95



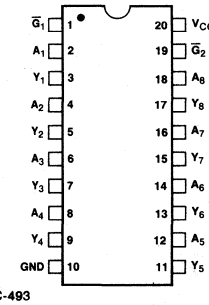
LIC-491

Am71/81LS96



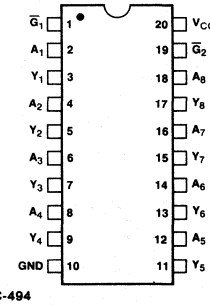
LIC-492

Am71/81LS97



LIC-493

Am71/81LS98



LIC-494

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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Am71/81LS95
Am71/81LS96
Am71/81LS97
Am71/81LS98

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{IH}	High Level Input Voltage				2			Volts
V_{IL}	Low Level Input Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_I = −18mA					−1.5	Volts
I_{OH}	High Level Output Current	MIL					−1.0	mA
		COM'L					−2.6	
V_{OH}	High Level Output Voltage	V_{CC} = Min., V_{IH} = 2.0V, V_{IL} = 0.8V	COM'L	I_{OH} = −5.0mA	2.4			Volts
				I_{OH} = −2.6mA	2.7			
			MIL, I_{OH} = −1.0mA		2.5			
I_{OL}	Low Level Output Current	COM'L					16	mA
		MIL					8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min., V_{IH} = 2.0V, V_{IL} = 0.8V	COM'L, I_{OL} = 16mA				0.5	V
			MIL, I_{OL} = 8.0mA				0.4	
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max., V_{IH} =2.0V, V_{IL} = 0.8V	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max., V_I = 7.0V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current, A Input	V_{CC} = Max.	Both $\overline{G}$ Inputs at 2.0V	V_I = 0.5V			−50	μA
	Low Level Input Current, $\overline{G}$ Input		Both $\overline{G}$ Inputs at 0.4V	V_I = 0.4V			−0.36	mA
				V_I = 0.4V			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max. (Note 2)			−30	−60	−130	mA
I_{CC}	Supply Current	V_{CC} = Max.	Am71/81LS95, Am71/81LS97			16	26	mA
			Am71/81LS96, Am71/81LS98			13	21	

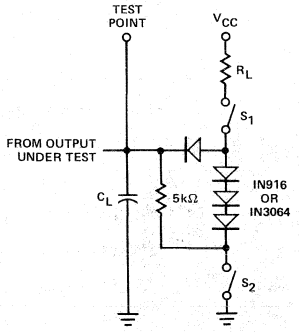
Notes: 1. All typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Not more than output should be shorted at a time, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C

Parameters	Description	Test Conditions	Am71/81LS95 Am71/81LS97 Min.	Typ.	Max.	Am71/81LS96 Am71/81LS98 Min.	Typ.	Max.	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15pF, R_L = 2kΩ		11	16		6	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			15	22		13	17	ns
t_{ZH}	Output Enable Time to High Level			16	25		17	27	ns
t_{ZL}	Output Enable Time to Low Level			13	20		16	25	ns
t_{HZ}	Output Disable Time from HIGH Level	C_L = 5pF, R_L = 2kΩ		13	20		13	20	ns
t_{LZ}	Output Disable Time from Low Level			19	27		18	27	

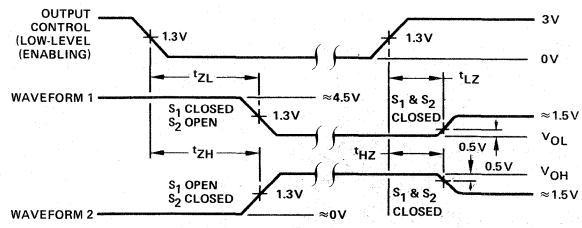
SWITCHING CHARACTERISTICS TEST CONDITIONS

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



LIC-495

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

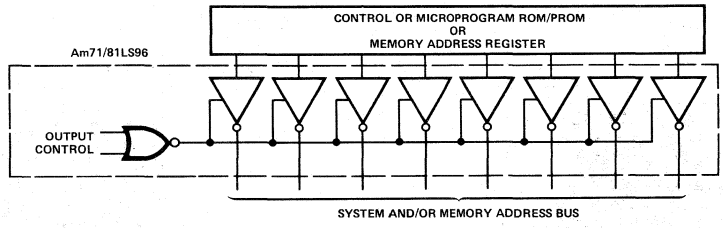


LIC-496

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR ≤ 1MHz, $Z_{OUT} \approx 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6$ns.
5. When measuring t_{PLH} and t_{PHL}, switches S_1 and S_2 are closed.

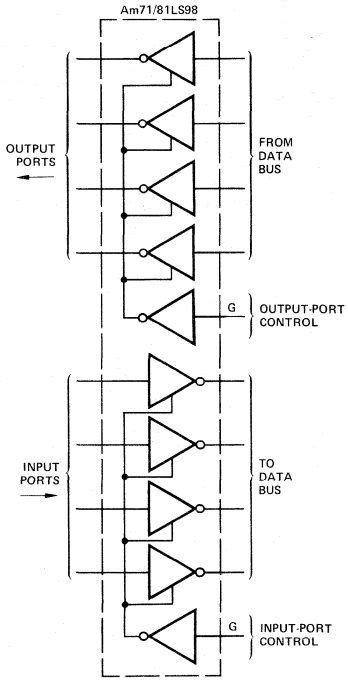
APPLICATIONS

Am71/81LS96 USED AS SYSTEM AND/OR MEMORY BUS DRIVER



LIC-497

INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



LIC-498

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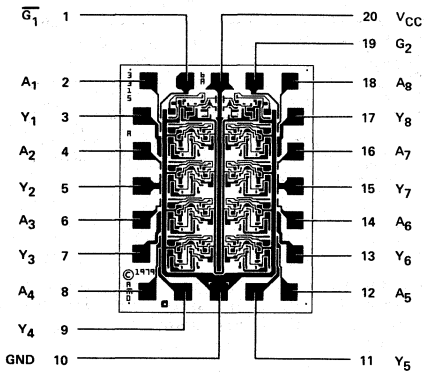
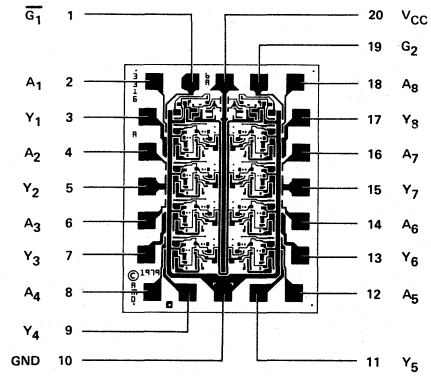
Metallization and Pad Layouts

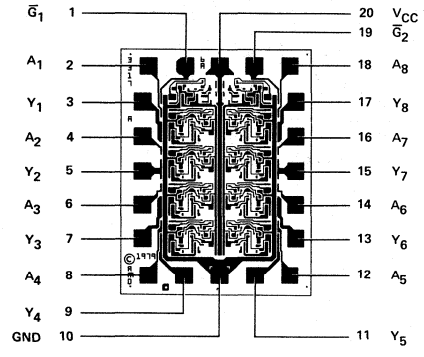
Am71/81LS95



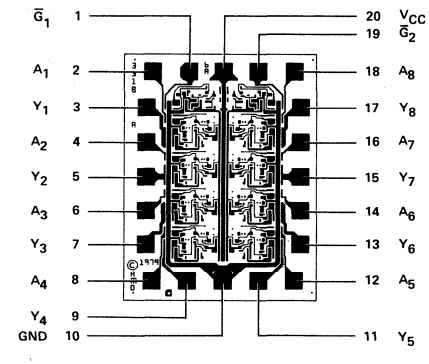
Am71/81LS96



Am71/81LS97



Am71/81LS98



DIE SIZES .064" X .049"

Am73/8303 • Am73/8304B

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} −1.15V V_{OH} interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- Am73/8303 inverting transceivers
- Am73/8304B noninverting transceivers
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20-pin ceramic and molded DIP package
- Low power − 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

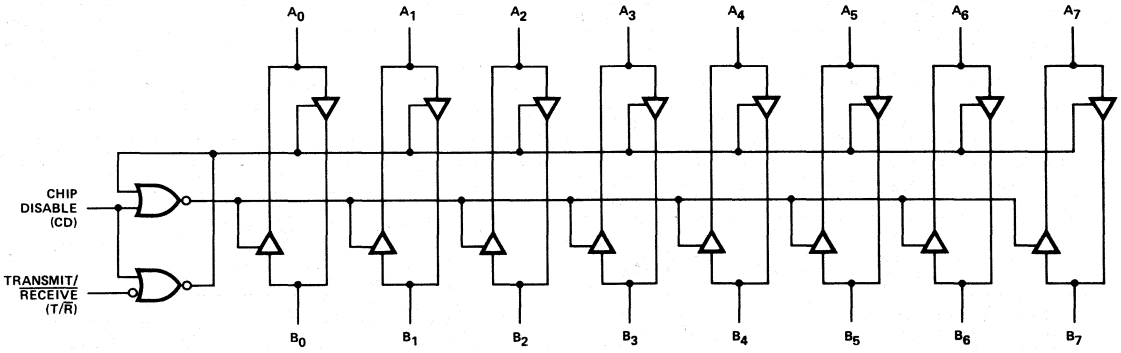
FUNCTIONAL DESCRIPTION

The Am73/8303 and Am73/8304B are 8-bit 3-State Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

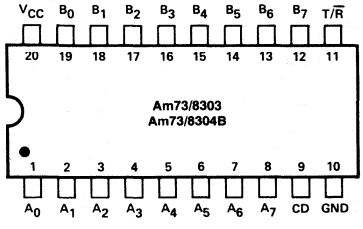
The output high voltage (V_{OH}) is specified at V_{CC} −1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

Am73/8304B LOGIC DIAGRAM



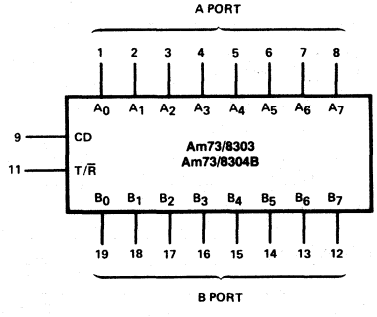
Am73/8303 has inverting transceivers

CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL	T_A = −55 to +125°C	V_{CC} MIN = 4.5V	V_{CC} MAX = 5.5V
COM'L	T_A = 0 to +70°C	V_{CC} MIN = 4.75V	V_{CC} MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
A PORT (A_0-A_7)							
V_{IH}	Logical "1" Input Voltage	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 2.0V	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.7		Volts
			I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical "0" Output Voltage	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OL} = 8mA		0.3	0.4	Volts
			COM'L I_{OL} = 16mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{CD}$ = 2.0V, V_{CC} MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	$\overline{CD}$ = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	$\overline{CD}$ = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			80	
B PORT (B_0-B_7)							
V_{IH}	Logical "1" Input Voltage	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX		2.0			Volts
V_{IL}	Logical "0" Input Voltage	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.8		Volts
			I_{OH} = −5.0mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX, Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{CD}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	$\overline{CD}$ = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	$\overline{CD}$ = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	$\overline{CD}$ = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			200	
CONTROL INPUTS $\overline{CD}$, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage		COM'L			0.8	Volts
			MIL			0.7	
I_{IH}	Logical "1" Input Current	V_I = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX, V_I = V_{CC} MAX				1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			$\overline{CD}$		−0.1	−0.25	
V_C	Input Clamp Voltage	I_{IN} = −12mA			−0.8	−1.5	Volts
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	Am73/8303	$\overline{CD}$ = V_I = 2.0V, V_{CC} = MAX		70	100	mA
			$\overline{CD}$ = 0.4V, V_{INA} = T/$\overline{R}$ = 2.0V, V_{CC} = MAX		100	150	
		Am73/8304B	$\overline{CD}$ = 2.0V, V_I = 0.4V, V_{CC} = MAX		70	100	mA
			$\overline{CD}$ = V_{INA} = 0.4V, T/$\overline{R}$ = 2.0V, V_{CC} = MAX		90	140	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameters	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	7	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	16	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	22	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	14	25	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	23	35	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	22	35	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	26	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	27	35	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

FUNCTION TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{Receive}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameters	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	27	35	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	32	40	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	26	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	30	40	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	28	40	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	31	40	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	28	40	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

DEFINITION OF FUNCTIONAL TERMS

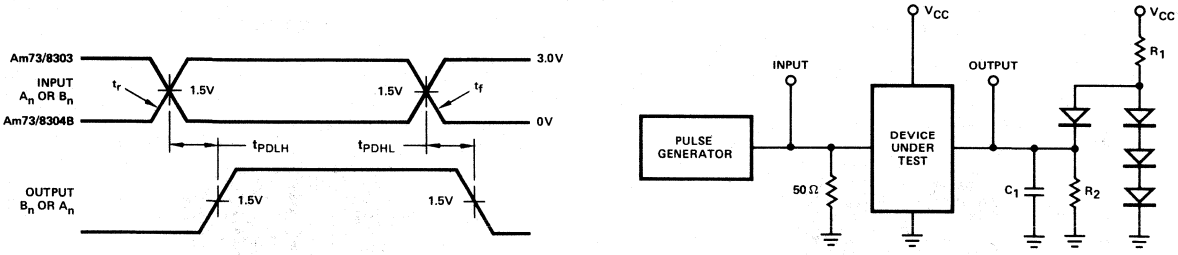
A_0-A_7 A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is LOW and are transmit inputs when T/$\overline{R}$ is HIGH.

B_0-B_7 B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW.

CD Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$).

T/$\overline{R}$ Transmit/$\overline{\text{Receive}}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH A port is the input and B port is the output. With T/$\overline{R}$ LOW A port is the output and B port is the input.

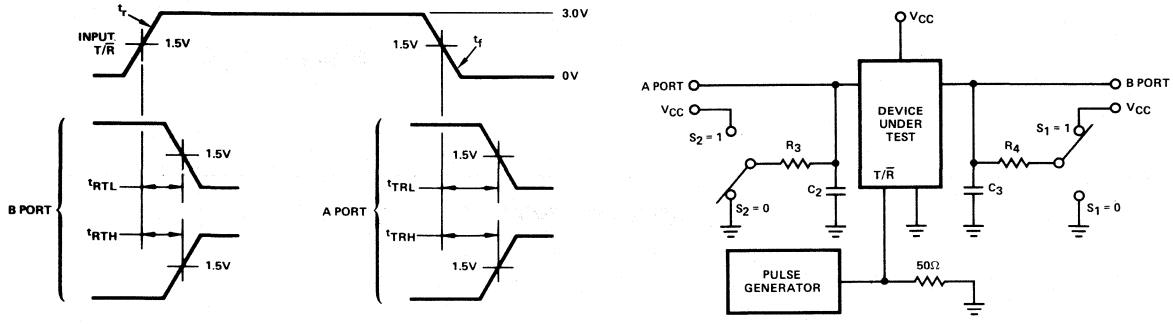
SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



$t_r = t_f < 10ns$
10% to 90%

Note: C_1 includes test fixture capacitance.

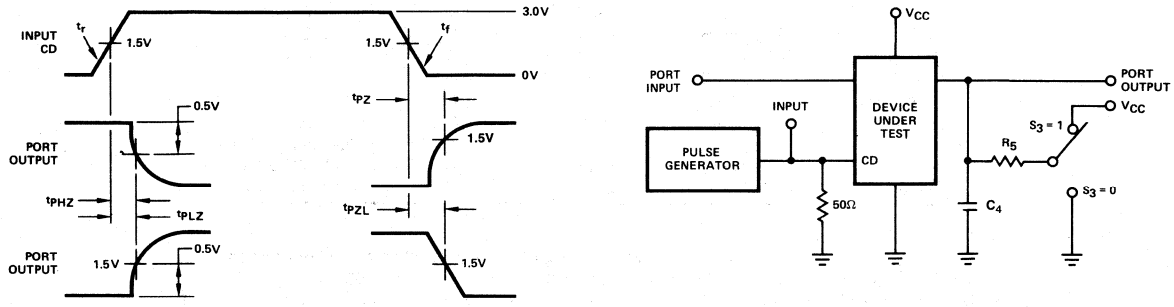
Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.



$t_r = t_f < 10ns$
10% to 90%

Note: C_2 and C_3 include test fixture capacitance.

Figure 2. Propagation Delay from T/$\overline{R}$ to A Port or B Port.



$t_r = t_f < 10ns$
10% to 90%

Note: C_4 includes test fixture capacitance.
Port input is in a fixed logical condition.

Figure 3. Propagation Delay from CD to A Port or B Port.

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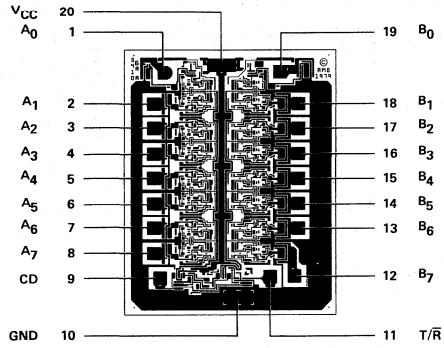
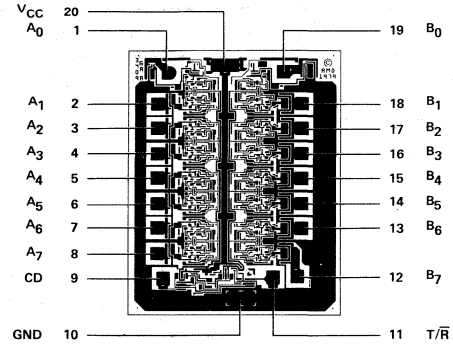
Metallization and Pad Layouts

Am73/8303



DIE SIZE .069" X .089"

Am73/8304B



DIE SIZE .069" X .089"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am73/8303 Order Number	Am73/8304B Order Number	Package Type (Note 1)	Operating (Note 2)	Screening Level (Note 3)
DP7303J	DP7304BJ	D-20	M	C-3
DP7303JB	DP7304BJB	D-20	M	B-3
DP8303J	DP8304BJ	D-20	C	C-1
DP8303JB	DP8304BJB	D-20	C	B-1
DP8303N	DP8304BN	P-20	C	C-1
DP8303NB	DP8304BNB	P-20	C	B-1
AM7303X	AM7304BX	Dice	M	Visual inspection to MIL-STD-883 Method 2010B.
AM8303X	AM8304BX	Dice	C	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am73/8307 • Am73/8308

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} – 1.15V V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- Am73/8307 has inverting tranceivers
- Am73/8308 has noninverting transceivers
- Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

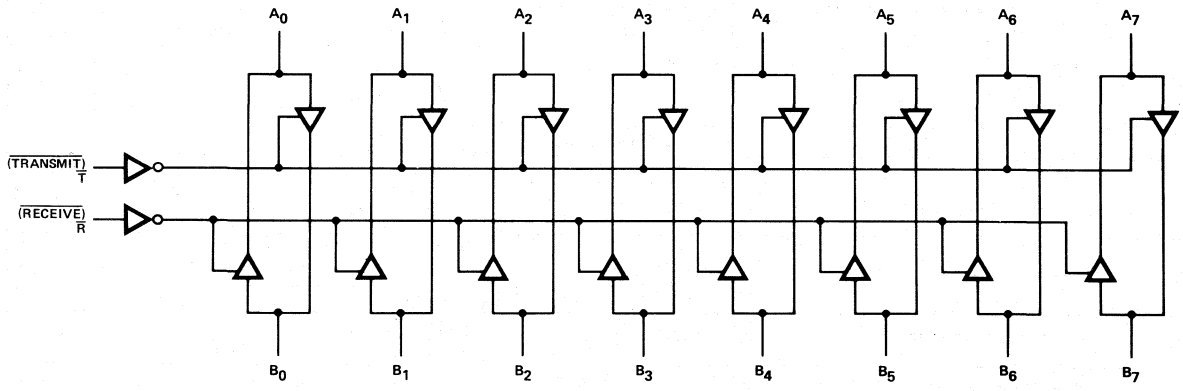
GENERAL DESCRIPTION

The Am73/8307 and Am73/8308 are 8-bit, 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables are provided for microprocessor system with separated read and write control bus lines.

The output high voltage (V_{OH}) is specified at V_{CC} – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM RAM, or microprocessors.

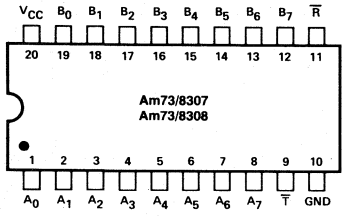
Am73/8308 LOGIC DIAGRAM



Am73/8307 has inverting transceivers

BLI-177

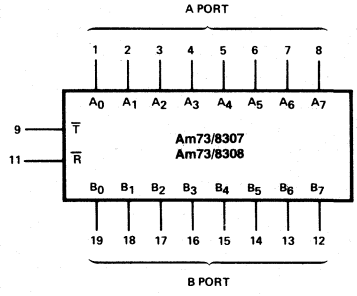
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
Am73/8307 is inverting from A_i to B_i

BLI-178

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

BLI-179

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ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL	T_A = −55 to +125°C	V_{CC} MIN = 4.5V	V_{CC} MAX = 5.5V
COM'L	T_A = 0 to +70°C	V_{CC} MIN = 4.75V	V_{CC} MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description		Test Conditions			Min	Typ (Note 1)	Max	Units
A PORT (A_0-A_7)									
V_{IH}	Logical "1" Input Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V			2.0			Volts
V_{IL}	Logical "0" Input Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V		COM'L			0.8	Volts
					MIL			0.7	
V_{OH}	Logical "1" Output Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.7		Volts
				I_{OH} = −3.0mA		2.7	3.95		
V_{OL}	Logical "0" Output Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OL} = 8mA			0.3	0.4	Volts
				COM'L	I_{OL} = 16mA		0.35	0.50	
I_{OS}	Output Short Circuit Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2			−10	−38	−75	mA
I_{IH}	Logical "1" Input Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V				−200	μA
				V_O = 4.0V				80	
B PORT (B_0-B_7)									
V_{IH}	Logical "1" Input Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V			2.0			Volts
V_{IL}	Logical "0" Input Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V		COM'L			0.8	Volts
					MIL			0.7	
V_{OH}	Logical "1" Output Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.8		Volts
				I_{OH} = −5.0mA		2.7	3.9		
				I_{OH} = −10mA		2.4	3.6		
V_{OL}	Logical "0" Output Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OL} = 20mA			0.3	0.4	Volts
				I_{OL} = 48mA			0.4	0.5	
I_{OS}	Output Short Circuit Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX, Note 2			−25	−50	−150	mA
I_{IH}	Logical "1" Input Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V				−200	μA
				V_O = 4.0V				200	
CONTROL INPUTS $\overline{T}$, $\overline{R}$									
V_{IH}	Logical "1" Input Voltage					2.0			Volts
V_{IL}	Logical "0" Input Voltage				COM'L			0.8	Volts
					MIL			0.7	
I_{IH}	Logical "1" Input Current		V_I = 2.7V				0.5	20	μA
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX, V_I = V_{CC} MAX					1.0	mA
I_{IL}	Logical "0" Input Current		V_I = 0.4V		$\overline{R}$		−0.1	−0.25	mA
					$\overline{T}$		−0.25	−0.5	
V_C	Input Clamp Voltage		I_{IN} = −12mA				−0.8	−1.5	Volts
POWER SUPPLY CURRENT									
I_{CC}	Power Supply Current	Am73/8307	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 2.0V, V_{CC} = MAX				70	100	mA
			$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2.0V, V_{CC} = MAX				100	150	
		Am73/8308	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 0.4V, V_{CC} = MAX				70	100	mA
			$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2.0V, V_{CC} = MAX				90	140	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	25	35	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	24	35	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	8	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	32	40	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	18	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	25	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	16	25	ns

FUNCTION TABLE

Control Inputs		Resulting Conditions	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	Out	In
0	1	In	Out
1	1	3-State	3-State
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	24	35	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	21	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	17	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	24	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	17	25	ns

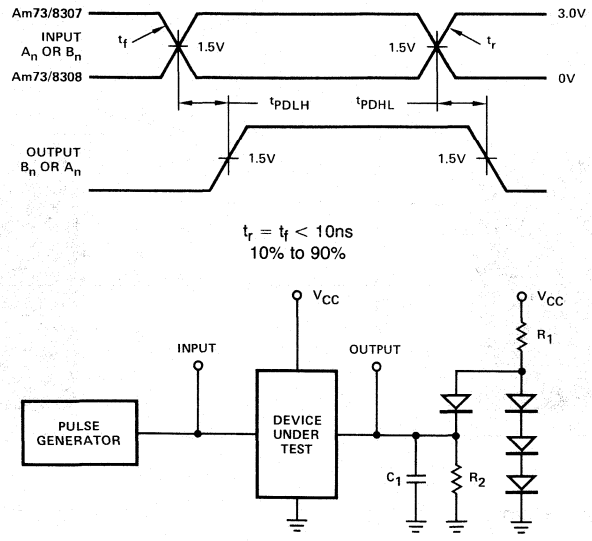
DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 A port inputs/outputs are receiver output drivers when $\overline{Receive}$ is LOW and $\overline{Transmit}$ is HIGH, and are transmit inputs when $\overline{Receive}$ is HIGH and $\overline{Transmit}$ is LOW.

B_0-B_7 B port inputs/outputs are transmit output drivers when $\overline{Transmit}$ is LOW and $\overline{Receive}$ is HIGH, and are receiver inputs when $\overline{Transmit}$ is HIGH and $\overline{Receive}$ is LOW.

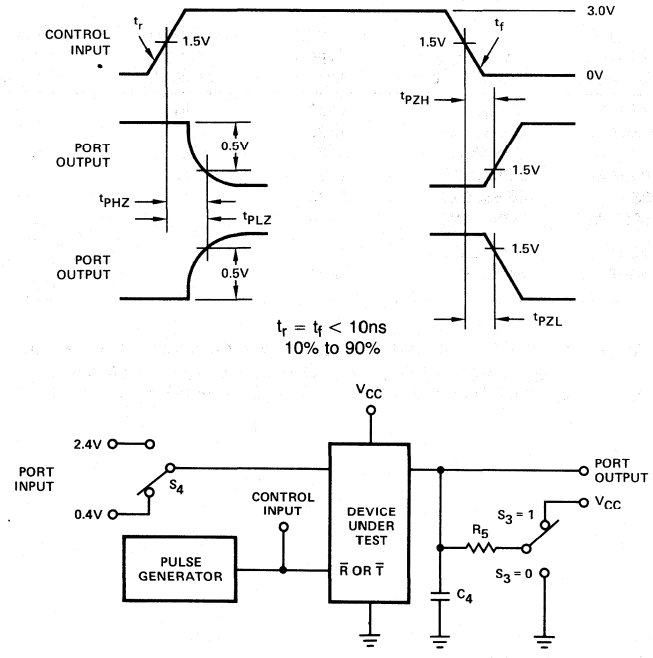
$\overline{Transmit}$, $\overline{Receive}$ These controls determine whether A port and B port drivers are in 3-state. With both $\overline{Transmit}$ and $\overline{Receive}$ HIGH both ports are in 3-state. $\overline{Transmit}$ and $\overline{Receive}$ both LOW activate both drivers and may cause oscillations. This is not an intended logic condition. With $\overline{Transmit}$ HIGH and $\overline{Receive}$ LOW A port is the output and B port is the input. With $\overline{Transmit}$ LOW and $\overline{Receive}$ HIGH B port is the output and A port is the input.

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



Note: C_1 includes test fixture capacitance.

Figure A. Propagation Delay from A Port to B Port or from B Port to A Port



Note: C_4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

Figure B. Propagation Delay to/from Three-State from $\overline{R}$ to A Port and $\overline{T}$ to B Port

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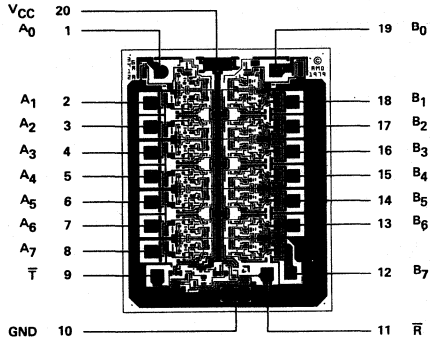
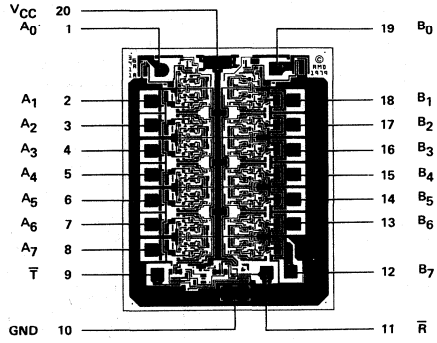
Metallization and Pad Layouts

Am73/8307



DIE SIZE .069" X .089"

Am73/8308



DIE SIZE .069" X .089"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am73/8307 Order Number	Am73/8308 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
DP7307J	DP7308J	D-20	M	C-3
DP7307JB	DP7308JB	D-20	M	B-3
DP8307J	DP8308J	D-20	C	C-1
DP8307JB	DP8308JB	D-20	C	B-1
DP8307N	DP8308N	P-20	C	C-1
DP8307NB	DP8308NB	P-20	C	B-1
AM7307X	AM7308X	Dice	M	Visual Inspection to MIL-STD-883 Method 20103
AM8307X	AM8308X	Dice	C	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpack. Number following letter is number of leads.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

AmZ8103 • AmZ8104

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- VCC – 1.15V VOH interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- AmZ8103 inverting transceivers
- AmZ8104 non-inverting transceivers
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20-pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

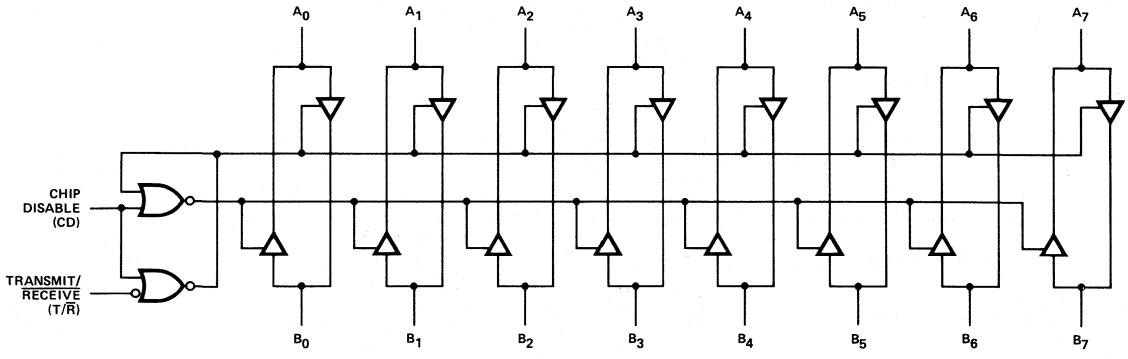
FUNCTIONAL DESCRIPTION

The AmZ8103 and AmZ8104 are 8-bit 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage (VOH) is specified at VCC – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

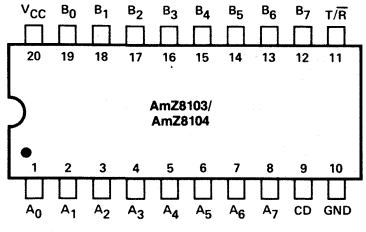
AmZ8104 LOGIC DIAGRAM



AmZ8103 has inverting transceivers.

BLI-216

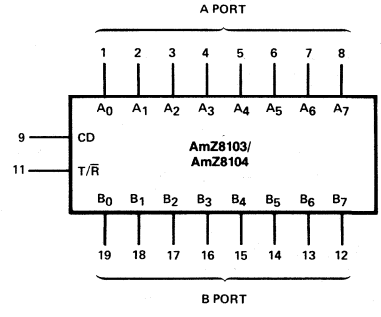
CONNECTION DIAGRAM Top View



BLI-169

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



BLI-170

V_{CC} = Pin 20
GND = Pin 10

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ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL T_A = −55 to +125°C V_{CC} MIN = 4.5V V_{CC} MAX = 5.5V
COM'L T_A = 0 to 70°C V_{CC} MIN = 4.75V V_{CC} MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
A PORT (A_0-A_7)								
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V			2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V		COM'L			0.8	Volts
				MIL			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.7		Volts
			I_{OH} = −3.0mA		2.7	3.95		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OL} = 12mA			0.3	0.4	Volts
			COM'L	I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2			−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	CD = 2.0V	V_O = 0.4V				−200	μA
			V_O = 4.0V				80	
B PORT (B_0-B_7)								
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX			2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX		COM'L			0.8	Volts
				MIL			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.8		Volts
			I_{OH} = −5.0mA		2.7	3.9		
			I_{OH} = −10mA		2.4	3.6		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OL} = 20mA			0.3	0.4	Volts
			I_{OL} = 48mA			0.4	0.5	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX, Note 2			−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	CD = 2.0V	V_O = 0.4V				−200	μA
			V_O = 4.0V				200	
CONTROL INPUTS CD, T/$\overline{R}$								
V_{IH}	Logical "1" Input Voltage				2.0			Volts
V_{IL}	Logical "0" Input Voltage			COM'L			0.8	Volts
				MIL			0.7	
I_{IH}	Logical "1" Input Current	V_I = 2.7V				0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX, V_I = V_{CC} MAX					1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V		T/$\overline{R}$		−0.1	−0.25	mA
				CD		−0.1	−0.25	
V_C	Input Clamp Voltage	I_{IN} = −12mA				−0.8	−1.5	Volts
POWER SUPPLY CURRENT								
I_{CC}	Power Supply Current	AmZ8103	CD = V_I = 2.0V, V_{CC} = MAX			70	100	mA
			CD = 0.4V, V_{INA} = T/$\overline{R}$ = 2.0V, V_{CC} = MAX			100	150	
		AmZ8104	CD = 2.0V, V_I = 0.4V, V_{CC} = MAX			70	100	mA
			CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2.0V, V_{CC} = MAX			90	140	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameters	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	19	25	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	7	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	22	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	23	33	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	22	33	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	26	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	27	35	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

FUNCTIONAL TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{Receive}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

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AC ELECTRICAL CHARACTERISTICS over operating range

Parameters	Description	Test Conditions	AmZ8103 COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Max	AmZ8103 MIL T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	16	19	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	20	23	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	28	33	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	24	29	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	16	19	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	25	30	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	19	22	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	23	26	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	38	43	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	26	30	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	38	43	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	38	43	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	38	43	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	41	47	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	41	47	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameters	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	19	25	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	26	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	28	38	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	28	38	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	31	40	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	31	40	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is LOW and are transmit inputs when T/$\overline{R}$ is HIGH.

B_0-B_7 B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW.

CD Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$).

T/$\overline{R}$ Transmit/$\overline{Receive}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH A port is the input and B port is the output. With T/$\overline{R}$ LOW A port is the output and B port is the input.

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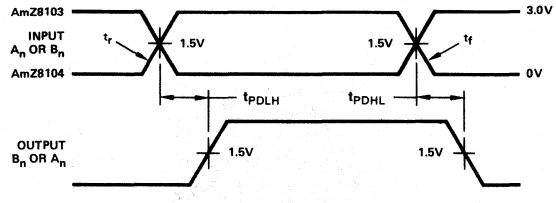
AC ELECTRICAL CHARACTERISTICS over operating range

Parameters	Description	Test Conditions	AmZ8104 COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Max	AmZ8104 MIL T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	21	24	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	21	24	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	28	33	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	28	34	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	25	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	28	34	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	25	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	23	26	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	38	43	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	26	30	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	38	43	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	42	48	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	42	48	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	45	51	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	45	51	ns

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



$t_r = t_f < 10ns$
10% to 90%

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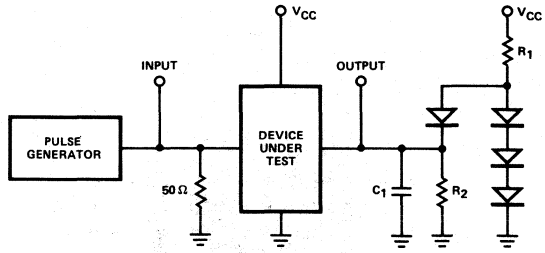
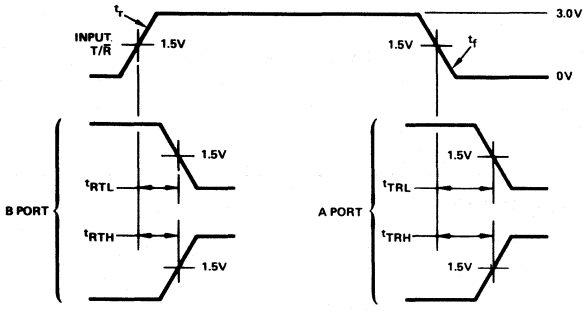


Note: C_1 includes test fixture capacitance.

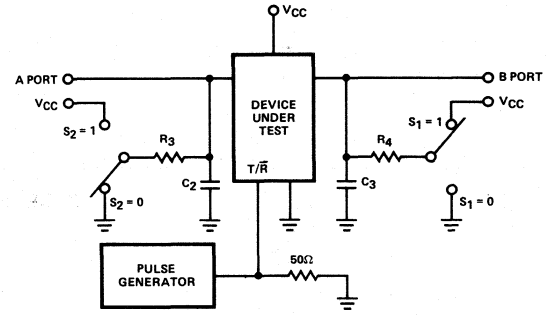
BLI-172

Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.



$t_r = t_f < 10ns$
10% to 90%

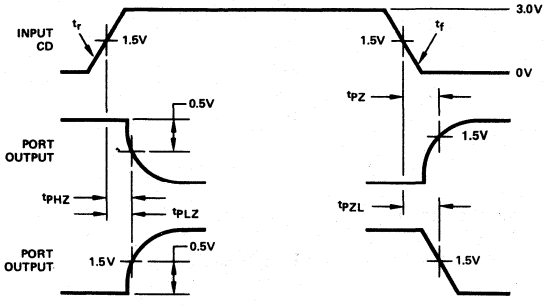
BLI-173



Note: C_2 and C_3 include test fixture capacitance.

BLI-174

Figure 2. Propagation Delay from T/$\overline{R}$ to A Port or B Port.



$t_r = t_f < 10ns$
10% to 90%

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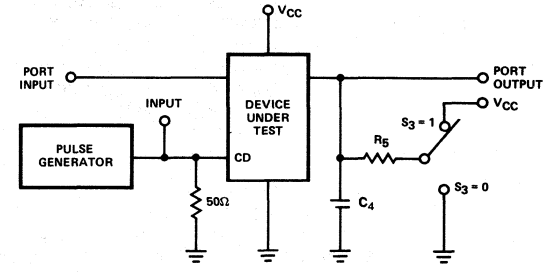

Note: C_4 includes test fixture capacitance.
Port input is in a fixed logical condition.

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Figure 3. Propagation Delay from CD to A Port or B Port.

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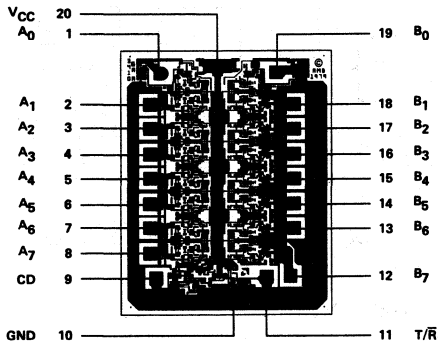
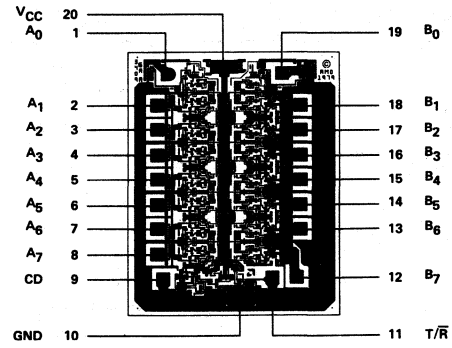
Metallization and Pad Layouts

AmZ8103



DIE SIZE .069" X .089"

AmZ8104



DIE SIZE .069" X .089"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

AmZ8103 Order Number	AmZ8104 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AMZ8103DC	AMZ8104DC	D-20	C	C-1
AMZ8103DCB	AMZ8104DCB	D-20	C	B-1
AMZ8103DM	AMZ8104DM	D-20	M	C-3
AMZ8103DMB	AMZ8104DMB	D-20	M	B-3
AMZ8103PC	AMZ8104PC	P-20	C	C-1
AMZ8103PCB	AMZ8104PCB	P-20	C	B-1

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

AmZ8107 • AmZ8108

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} −1.15V V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- AmZ8107 has inverting transceivers
- AmZ8108 has noninverting transceivers
- Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

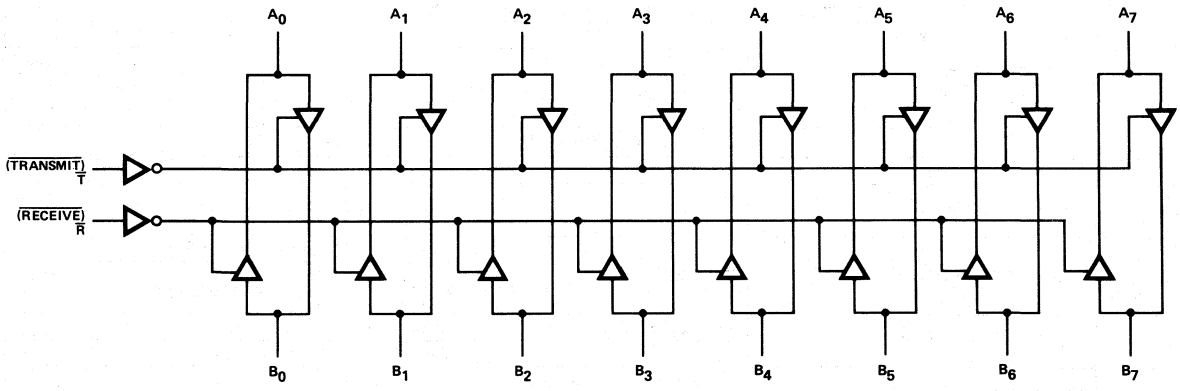
GENERAL DESCRIPTION

The AmZ8107 and AmZ8108 are 8-bit, 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables are provided for microprocessor system with separated read and write control bus lines.

The output high voltage (V_{OH}) is specified at V_{CC} −1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

AmZ8108 LOGIC DIAGRAM



AmZ8107 has inverting transceivers

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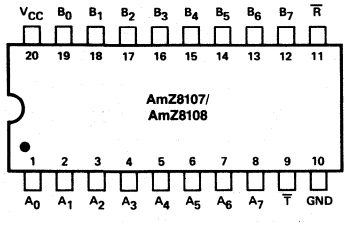
CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.
AmZ8107 is inverting from Ai to Bi

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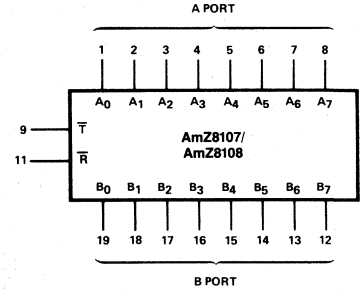
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL T_A = −55 to +125°C V_{CC} MIN = 4.5V V_{CC} MAX = 5.5V
COM'L T_A = 0 to +70°C V_{CC} MIN = 4.75V V_{CC} MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description		Test Conditions			Min	Typ (Note 1)	Max	Units
A PORT (A_0-A_7)									
V_{IH}	Logical "1" Input Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V			2.0			Volts
V_{IL}	Logical "0" Input Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V		COM'L			0.8	Volts
					MIL			0.7	
V_{OH}	Logical "1" Output Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.7		Volts
				I_{OH} = −3.0mA		2.7	3.95		
V_{OL}	Logical "0" Output Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OL} = 12mA			0.3	0.4	Volts
				COM'L	I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2			−10	−38	−75	mA
I_{IH}	Logical "1" Input Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V				−200	μA
				V_O = 4.0V				80	
B PORT (B_0-B_7)									
V_{IH}	Logical "1" Input Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V			2.0			Volts
V_{IL}	Logical "0" Input Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V		COM'L			0.8	Volts
					MIL			0.7	
V_{OH}	Logical "1" Output Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.8		Volts
				I_{OH} = −5.0mA		2.7	3.9		
				I_{OH} = −10mA		2.4	3.6		
V_{OL}	Logical "0" Output Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OL} = 20mA			0.3	0.4	Volts
				I_{OL} = 48mA			0.4	0.5	
I_{OS}	Output Short Circuit Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_O = 0V V_{CC} = MAX, Note 2			−25	−50	−150	mA
I_{IH}	Logical "1" Input Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V				−200	μA
				V_O = 4.0V				200	
CONTROL INPUTS $\overline{T}$, $\overline{R}$									
V_{IH}	Logical "1" Input Voltage					2.0			Volts
V_{IL}	Logical "0" Input Voltage				COM'L			0.8	Volts
					MIL			0.7	
I_{IH}	Logical "1" Input Current		V_I = 2.7V				0.5	20	μA
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX, V_I = V_{CC} MAX					1.0	mA
I_{IL}	Logical "0" Input Current		V_I = 0.4V		$\overline{R}$		−0.1	−0.25	mA
					$\overline{T}$		−0.25	−0.5	
V_C	Input Clamp Voltage		I_{IN} = −12mA				−0.8	−1.5	Volts
POWER SUPPLY CURRENT									
I_{CC}	Power Supply Current	AmZ8107	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 2.0V, V_{CC} = MAX				70	100	mA
			$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2.0V, V_{CC} = MAX				100	150	
		AmZ8108	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 0.4V, V_{CC} = MAX				70	100	mA
			$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2.0V, V_{CC} = MAX				90	140	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	20	27	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	8	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	18	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	25	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	16	25	ns

FUNCTION TABLE

Control Inputs		Resulting Conditions	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	Out	In
0	1	In	Out
1	1	3-State	3-State
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

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AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	AmZ8107 COM'L $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max	AmZ8107 MIL $T_A = -55$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	19	16	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	23	20	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, R = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	29	24	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	19	16	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	30	25	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	19	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ	Max	Units
	A PORT DATA/MODE SPECIFICATIONS				
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	20	27	ns
	B PORT DATA/MODE SPECIFICATIONS				
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	17	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	24	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	17	25	ns

DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 A port inputs/outputs are receiver output drivers when $\overline{\text{Receive}}$ is LOW and $\overline{\text{Transmit}}$ is HIGH, and are transmit inputs when $\overline{\text{Receive}}$ is HIGH and $\overline{\text{Transmit}}$ is LOW.

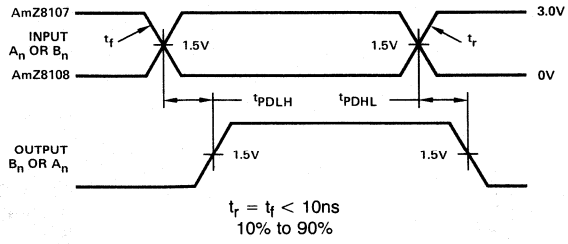
B_0-B_7 B port inputs/outputs are transmit output drivers when $\overline{\text{Transmit}}$ is LOW and $\overline{\text{Receive}}$ is HIGH, and are receiver inputs when $\overline{\text{Transmit}}$ is HIGH and $\overline{\text{Receive}}$ is LOW.

$\overline{\text{Transmit}}$, $\overline{\text{Receive}}$ These controls determine whether A port and B port drivers are in 3-state. With both $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ HIGH both ports are in 3-state. $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ both LOW activate both drivers and may cause oscillations. This is not an intended logic condition. With Transmit HIGH and Receive LOW A port is the output and B port is the input. With $\overline{\text{Transmit}}$ LOW and $\overline{\text{Receive}}$ HIGH B port is the output and A port is the input.

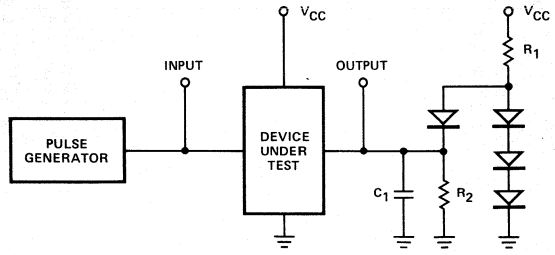
AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	AmZ8108 COM'L $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max	AmZ8108 MIL $T_A = -55$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

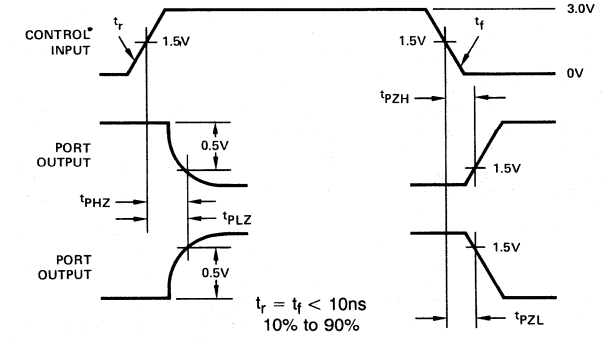


$t_r = t_f < 10ns$
10% to 90%

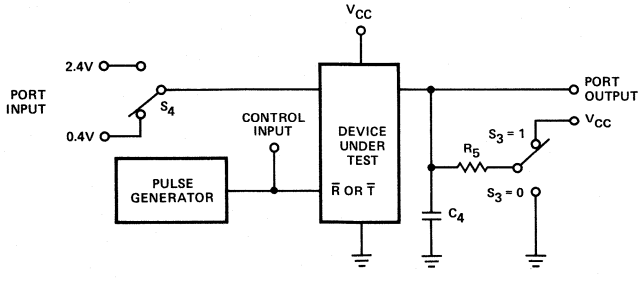


Note: C_1 includes test fixture capacitance.

Figure A. Propagation Delay from A Port to B Port or from B Port to A Port



$t_r = t_f < 10ns$
10% to 90%



Note: C_4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

Figure B. Propagation Delay to/from Three-State from $\overline{R}$ to A Port and $\overline{T}$ to B Port

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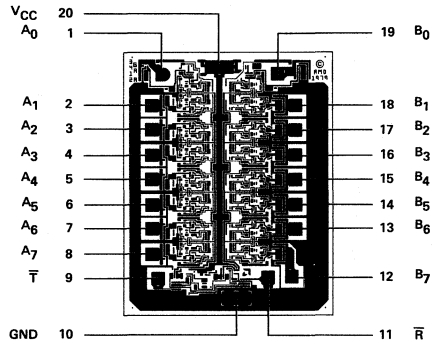
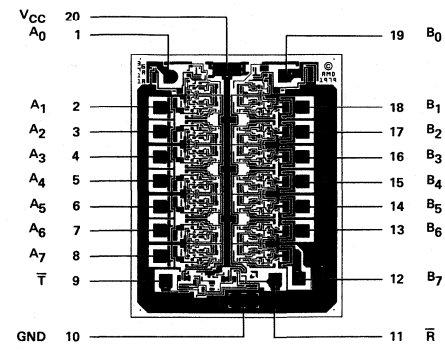
Metallization and Pad Layouts

AmZ8107



DIE SIZE .069" X .089"

AmZ8108



DIE SIZE .069" X .089"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

AmZ8107 Order Number	AmZ8108 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AMZ8107DC	AMZ8108DC	D-20	C	C-1
AMZ8107DCB	AMZ8108DCB	D-20	C	B-1
AMZ8107DM	AMZ8108DM	D-20	M	C-3
AMZ8107DMB	AMZ8108DMB	D-20	M	B-3
AMZ8107PC	AMZ8108PC	P-20	C	C-1
AMZ8107PCB	AMZ8108PCB	P-20	C	B-1

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpack. Number following letter is number of leads.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

AmZ8127

AmZ8000 Clock Generator

Product Specification
March 1981

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- **High-drive high-level clock output**
  Special output provides clock signal matched to requirements of AmZ8000 CPU, MMU and DMA devices.
- **Four TTL-level clocks**
  Generates synchronized TTL compatible clocks at 16MHz, 2MHz and 1MHz to drive memory circuits and LSI peripheral devices. An additional TTL clock is synchronized with the CPU high-level clock for registers, latches and other peripherals.
- **Synchronized $\overline{\text{WAIT}}$ state and time-out controls**
  On-chip logic generates $\overline{\text{WAIT}}$ signal under control of Halt, Single-step, Status and Ready signals. Automatic time-out of peripheral wait requests.
- **100% MIL-STD-883 reliability assurance testing.**

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	$0°C \leq T_A \leq 70°C$	AMZ8127DC
Hermetic DIP	$-55°C \leq T_A \leq +125°C$	AMZ8127DM

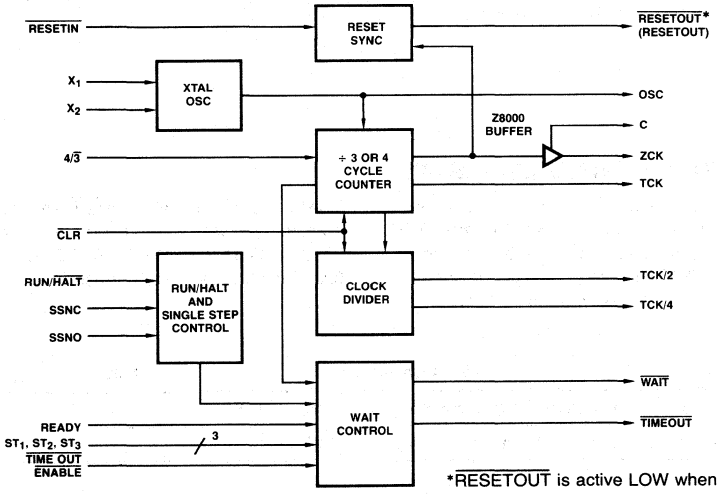
FUNCTIONAL DESCRIPTION

The AmZ8127 Clock Generator and Controller provides the clock oscillator, frequency dividers and clock drivers for the complete array of AmZ8000 CPUs, peripherals and memory system configurations. In addition to the special 4MHz output driver for the AmZ8001 and AmZ8002 CPUs, a standard buffered TTL 16MHz oscillator output is provided for dynamic memory timing and control. The AmZ8127 forms an integral part of the dynamic memory support chip set including the AmZ8163 EDC and Refresh Controller, AmZ8164 Dynamic Memory Controller, AmZ8160 Error Detection and Correction Unit and AmZ8161/AmZ8162 EDC Bus Buffers. The oscillator is designed to operate with a 16MHz crystal or with external 16MHz drive. The AmZ8127 uses an internal divide-by-4 to provide 4MHz clock drive to the AmZ8001/AmZ8002 CPU. Additional dividers generate synchronous buffered 4, 2 and 1MHz clock outputs for use by peripheral devices. The clock divider counters are clearable to allow synchronizing the multiple clock outputs.

The controller functions include $\overline{\text{RESET}}$, RUN/$\overline{\text{HALT}}$, SINGLE-STEP, READY and a READY TIMEOUT counter which limits a peripheral's wait request to 16 clock cycles. The CPU's WAIT input is controlled by RUN/$\overline{\text{HALT}}$, Single-Step, Status and READY. When RUN/$\overline{\text{HALT}}$ is LOW the AmZ8127 drives the $\overline{\text{WAIT}}$ output LOW causing the CPU to add wait states (TW). The READY input is used by peripherals to request wait states. The active LOW input timeout enable, $\overline{\text{TOEN}}$, is used to force $\overline{\text{TIMEOUT}}$ LOW and $\overline{\text{WAIT}}$ HIGH 16 clock cycles after a peripheral has requested a wait but fails to release the request. The CPU status lines ST_1, ST_2 and ST_3 are decoded in the AmZ8127 to disable the $\overline{\text{TIMEOUT}}$ counter during CPU "Internal Operations" and during refresh.

The 4/$\overline{3}$ input controls the clock duty cycle. An internal pull-up resistor pulls this input high for AmZ8000 CPUs. A LOW input causes the cycle counter to output a 33% duty cycle for 8086 family CPUs.

BLOCK DIAGRAM
CLOCK GENERATOR



*$\overline{\text{RESETOUT}}$ is active LOW when 4/$\overline{3}$ = HIGH

AMZ-017

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)
MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions (Note 1)				Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN	ZCK	I_{OH} = −0.1mA		V_{CC}−0.4	V_{CC}−0.1		Volts
			TTL Outputs	I_{OH} = −1mA	MIL	2.4	3.4		Volts
				I_{OH} = −2.6mA	COM'L				
V_{OL}	Output LOW Voltage	V_{CC} = MIN		I_{OL} = 0.1mA, ZCK Output				0.4	Volts
				I_{OL} = 16mA, TTL Output				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input HIGH Voltage		$\overline{RESETIN}$		2.8	2.25		Volts
				ST_1, ST_2, ST_3, $\overline{CLR}$, $\overline{TOEN}$, X_1, READY		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input LOW voltage		ST_1, ST_2, ST_3, $\overline{CLR}$, $\overline{TOEN}$, X_1, READY				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA (Note 3)						−1.5	Volts
$V_{IN}-V_{IL}$	$\overline{RESETIN}$ Hysteresis	V_{CC} = MIN				400	650		mV
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		SSNO				−1.6	mA
				SSNC, 4/3, RUN/$\overline{HALT}$, READY				−1.2	mA
				$\overline{TOEN}$, $\overline{CLR}$, X_1				−0.72	mA
				$\overline{RESETIN}$, ST_1, ST_2, ST_3				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		4/3, SSNC, SSNO RUN/$\overline{HALT}$			(Note 4)	−300	μA
				$\overline{RESETIN}$			(Note 4)	−200	μA
				$\overline{CLR}$, READY, $\overline{TOEN}$ ST_1, ST_2, ST_3				+50	μA
				X_1				+600	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		$\overline{CLR}$, READY, $\overline{TOEN}$ ST_1, ST_2, ST_3				+1.0	mA
I_{SC}	Output Short Circuit Current (Note 5)	V_{CC} = MAX		ZCK Output		−50		−240	mA
				Others		−40		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX		X_1 = 2.4V, ZCK = TCK's = LOW			95	140	mA
				Operating, $f_{OSC} \leq$ 24MHz (Note 6)			120	180	

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not applicable to X_1.
4. Specification is negative because of internal input pull-up resistors.
5. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
6. For oscillator frequencies up to 24MHz, outputs open.

STATIC INPUT ELECTRICAL CHARACTERISTICS

The static control inputs, SSNO, SSNC (Single Step), RUN/$\overline{HALT}$ and 4/$\overline{3}$ (clock duty cycle control), are Low-Power Schottky TTL compatible inputs with internal pull-up resistors to the +5V supply. They may be left open for a HIGH input (e.g., 4/$\overline{3}$ is left open for operation with AmZ8001/8002), or grounded for a LOW input. SSNO, SSNC and RUN/$\overline{HALT}$ are intended to be grounded or opened by switches. 4/$\overline{3}$ is normally wired LOW for operation with 8086 or left open for AmZ8001/8002. These inputs are specified at 0.4V/2.4V for test convenience.

Parameter	Description	Test Conditions		Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH input voltage	RUN/$\overline{HALT}$, SSNO	2.4			Volts
V_{IL}	Input LOW Voltage	Guaranteed LOW input voltage	SSNC, 4/$\overline{3}$			0.4	Volts

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature		−65 to +150°C
Temperature (Ambient) Under Bias		−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous		−0.5 to +7V
DC Voltage Applied to Outputs for HIGH Output State		−0.5V to +V_{CC} max
DC Input Voltage	X_1, 4/$\overline{3}$, SSNO, SSNC, RUN/$\overline{HALT}$	−0.5V to V_{CC} +0.5V
	Other Inputs	−0.5 to +5.5V
DC Voltage Applied to C		−0.5 to +8V
DC Output Current, Into Outputs		30 mA
DC Input Current		−30 to +5.0mA

SWITCHING CHARACTERISTICS – OSCILLATOR, $\overline{WAIT}$ AND ZCK OUTPUT

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min	Typ	Max	Units	Tests Conditions
f_{MAX}	Oscillator Frequency		24			MHz	See Test Circuits (Note 7)
t_{rC}	ZCK Rise Time	C_L = 80pF		9	12	ns	ZCK C_L = 80pF (Note 8)
t_{fC}	ZCK Fall Time			7.6	11	ns	
t_{rC}	ZCK Rise Time	C_L = 200pF		15.4	20	ns	ZCK C_L = 200pF (Note 8)
t_{fC}	ZCK Fall Time			14.0	20	ns	
t_{PLH}	READY to $\overline{WAIT}$			8	14	ns	See Test Circuits
t_{PHL}				11.5	16	ns	
t_{PLH}	Status ST_i to $\overline{WAIT}$			13	17	ns	
t_{PHL}				17.2	21	ns	
t_S	$\overline{CLR}$ to OSC (↓) Set-up Time			15	18	ns	
t_H	$\overline{CLR}$ to OSC (↓) Hold Time			−11	−6	ns	

Notes: 7. Specification is based on fundamental mode crystal. See application section.
8. ZCK rise and fall times are based on a bootstrap capacitor value of 27pF.

SWITCHING CHARACTERISTICS – 4/$\overline{3}$ = HIGH (AmZ8000 Mode)

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min	Typ	Max	Units	Test Conditions
t_S	READY to ZCK Set-up Time	(Note 9)	T/4 + 10	T/4 + 4.5		ns	See Test Circuits ZCK C_L = 80pF
t_H	READY to ZCK Hold Time		T/4 + 2	T/4		ns	
t_S	Status ST_i to ZCK Set-up Time		T/4 + 12	T/4 + 9.5		ns	
t_H	Status ST_i to ZCK Hold Time		T/4 − 3	T/4 −7.5		ns	
t_S	$\overline{TOEN}$ to ZCK Set-up Time					ns	
t_H	$\overline{TOEN}$ to ZCK Hold Time					ns	
t_{SKEW}	ZCK to OSC		3	6	10	ns	
t_{SKEW}	ZCK to TCK		0	4.0	7	ns	
t_{PLH}	ZCK to $\overline{RESETOUT}$ Propagation Delay			9.0	13	ns	
t_{PHL}				4	8	ns	

Note: 9. T = ZCK period.

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SWITCHING CHARACTERISTICS – 4/$\overline{3}$ = LOW (8086 Mode)

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min	Typ	Max	Units	Test Conditions
t_S	READY to ZCK Set-up Time				ns	See Test Circuits ZCK C_L = 80pF
t_H	READY to ZCK Hold Time				ns	
t_S	Status ST_i to ZCK Set-up Time				ns	
t_H	Status ST_i to ZCK Hold Time				ns	
t_S	$\overline{TOEN}$ to ZCK Set-up Time				ns	
t_H	$\overline{TOEN}$ to ZCK Hold Time				ns	
t_{SKEW}	ZCK to OSC Skew				ns	
t_{SKEW}	ZCK to TCK Skew				ns	
t_{PLH}	ZCK to $\overline{RESETOUT}$ Propagation Delay				ns	
t_{PHL}					ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – OSCILLATOR, $\overline{WAIT}$ AND ZCK OUTPUTS*

Parameters	Description		AmZ8127 COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% Min	AmZ8127 COM'L Max	AmZ8127 MIL T = −55 to +125°C V_{CC} = 5.0V ±10% Min	AmZ8127 MIL Max	Units	Tests Conditions
f_{MAX}	Oscillator Frequency		24		24		MHz	(Note 7)
t_{rC}	ZCK Rise Time	C_L = 80pF		15			ns	C_L = 80pF (Note 8)
t_{fC}	ZCK Fall Time			14			ns	
t_{rC}	ZCK Rise Time	C_L = 200pF		25			ns	C_L = 200pF (Note 8)
t_{fC}	ZCK Fall Time			25			ns	
t_{PLH}	READY to WAIT Propagation Delay			17			ns	See Test Circuits
t_{PHL}				19			ns	
t_{PLH}	Status ST_i to $\overline{WAIT}$ Propagation Delay			20			ns	
t_{PHL}				25			ns	
t_S	$\overline{CLR}$ to OSC (↓) Set-up Time			21			ns	
t_H	$\overline{CLR}$ to OSC (↓) Hold Time			−3			ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

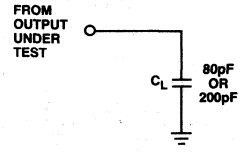
SWITCHING CHARACTERISTICS OVER OPERATING RANGE – 4/$\overline{3}$ = HIGH (AmZ8000 Mode)

Parameters	Description	AmZ8127 COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% Min	AmZ8127 COM'L Max	AmZ8127 MIL T = −55 to +125°C V_{CC} = 5.0V ±10% Min	AmZ8127 MIL Max	Units	Tests Conditions
t_S	READY to ZCK Set-up Time	T/4 + 14				ns	See Test Circuits ZCK C_L = 80pF
t_H	READY to ZCK Hold Time	T/4 + 5				ns	
t_S	Status ST_i to ZCK Set-up Time	T/4 + 15				ns	
t_H	Status ST_i to ZCK Hold Time	T/4				ns	
t_S	$\overline{TOEN}$ to ZCK Set-up Time					ns	
t_H	$\overline{TOEN}$ to ZCK Hold Time					ns	
t_{SKEW}	ZCK to OSC Skew	2	14			ns	
t_{SKEW}	ZCK to TCK Skew	−2	10			ns	
t_{PLH}	ZCK to $\overline{RESETOUT}$ Propagation Delay		16			ns	
t_{PHL}			12			ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – $4/\overline{3}$ = LOW (8086 Mode)

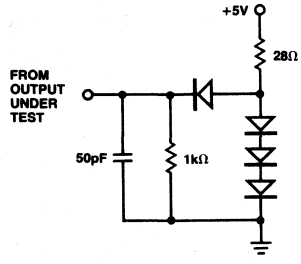
Parameters	Description	AmZ8127 COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Min	AmZ8127 COM'L Max	AmZ8127 MIL T = −55 to +125°C, V_{CC} = 5.0V ±10% Min	AmZ8127 MIL Max	Units	Tests Conditions
t_S	READY to ZCK Set-up Time					ns	See Test Circuits ZCK C_L = 80pF
t_H	READY to ZCK Hold Time					ns	
t_S	Status ST_i to ZCK Set-up Time					ns	
t_H	Status ST_i to ZCK Hold Time					ns	
t_S	$\overline{TOEN}$ to ZCK Set-up Time					ns	
t_H	$\overline{TOEN}$ to ZCK Hold Time					ns	
t_{SKEW}	ZCK to OSC Skew					ns	
t_{SKEW}	ZCK to TCK Skew					ns	
t_{PLH}	ZCK to $\overline{RESETOUT}$ Propagation Delay					ns	
t_{PHL}						ns	

SWITCHING TEST CIRCUITS



ZCK Output

AMZ-018

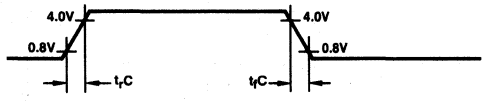


TTL Outputs

AMZ-019

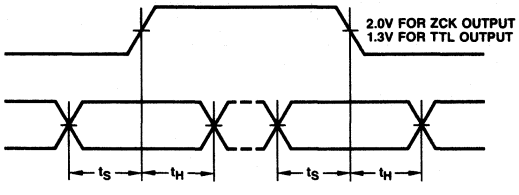
SWITCHING TEST WAVEFORMS

ZCK RISE AND FALL TIMES



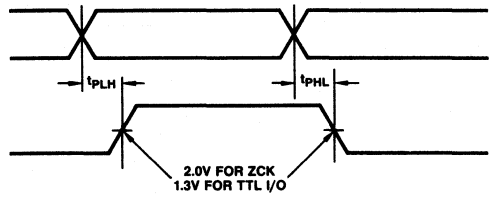
AMZ-020

SET-UP AND HOLD TIMES



AMZ-021

PROPAGATION DELAY TIMES



AMZ-022

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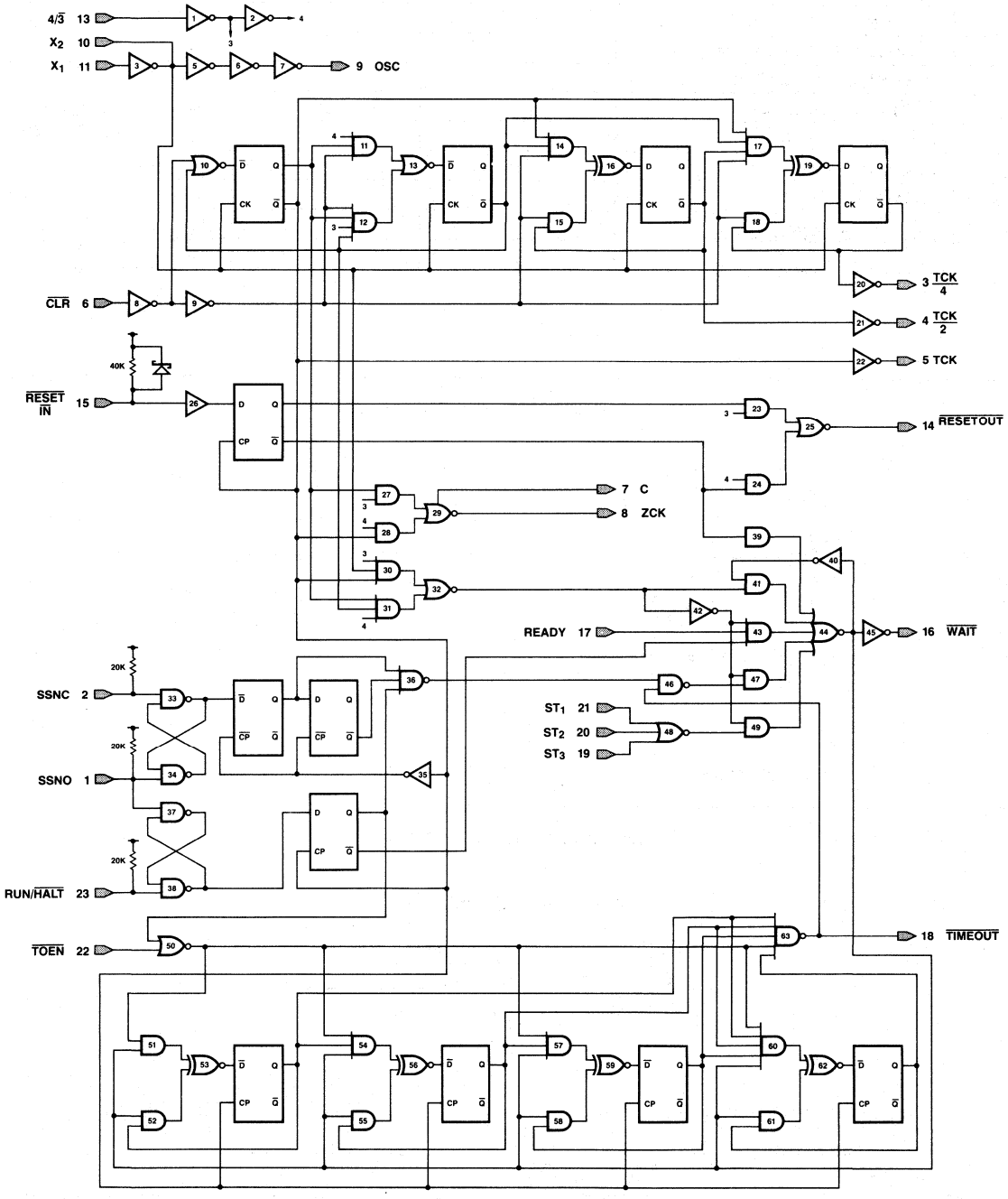
LOGIC DIAGRAM



AMZ-023

DEFINITION OF FUNCTIONAL TERMS

ZCK Buffered clock output for CPU and peripherals. This output has under/overshoot control and provides the high level output voltage required (V_{CC} – 0.4V). This output is capable of driving multiple CPU clock inputs (or DMA, MMU, etc).

C Bootstrap input. The capacitor C_B is connected from the ZCK clock output to C to provide faster ZCK risetime.

TCK TTL level buffered clock output. TCK is the same frequency as ZCK and is synchronized with ZCK. TCK is in phase with ZCK when the 4/$\overline{3}$ duty cycle control input is HIGH (50% duty cycle) and out of phase with ZCK when 4/$\overline{3}$ is LOW (33% ZCK duty cycle).

TCK/2, TCK/4 TTL buffered clocks for peripherals. TCK/2 and TCK/4 are 1/2 and 1/4 the TCK frequency and are synchronized with the rising edge of TCK.

OSC The clock oscillator TTL buffered output. This output provides a high speed clock for dynamic memory timing (e.g. AmZ8000 uses this output to generate $\overline{RAS}$/MUX-Select/$\overline{CAS}$ timing for dynamic RAMs) or other system application. The ZCK and TCK outputs are synchronized to the OSC rising edge.

4/$\overline{3}$ Clock duty cycle control for ZCK and TCK. A HIGH input (no connection – input has internal pull-up) will result in a 50% duty cycle for AmZ8000 application. A LOW input will cause a 33% duty cycle ZCK output for 8086 (66% duty cycle TCK).

$\overline{CLR}$ The clear active LOW input for internal counters. A LOW input meeting set-up and hold time requirements will clear the internal clock counters on the rising edge of OSC.

$\overline{WAIT}$ The $\overline{WAIT}$ output for connection to the CPU $\overline{WAIT}$ input. This latched output controls when the CPU enters wait states in response to the READY, ST_1, ST_2, ST_3, RUN/$\overline{HALT}$ and Single Step inputs.

READY The active HIGH READY input is used by peripherals to request wait states. Ready inputs must meet the wait latch set-up and hold time requirements.

$\overline{TIMEOUT}$ The Timeout Counter active LOW output. The Timeout Counter counts ZCK/TCK clock cycles and is used to force $\overline{WAIT}$ HIGH 15 clock cycles after a peripheral has requested a wait but has failed to release the request. This output is normally used to interrupt the CPU.

$\overline{TOEN}$ The Timeout Enable active LOW input. A LOW input allows the Timeout Counter to count, causes the $\overline{TIMEOUT}$ output to go LOW for one ZCK/TCK clock period after 15 cycles and forces $\overline{WAIT}$ HIGH at the rising edge of the 16th cycle. A HIGH input disables the counter and allows $\overline{WAIT}$ to be controlled by the READY, RUN/$\overline{HALT}$ and Single Step inputs.

$\overline{RESETOUT}$ (RESETOUT) The Reset Output to the CPU. It is active LOW when the 4/$\overline{3}$ input is HIGH and active HIGH when the 4/$\overline{3}$ input is LOW.

$\overline{RESETIN}$ The active LOW Reset Input. A LOW input will cause $\overline{RESETOUT}$ to go LOW synchronous with ZCK ↓ . Pushbutton reset is implemented by momentarily grounding RESETIN. Power-up reset is implemented by connecting a capacitor from RESETIN to ground. Capacitor values from 10μF to 22μF will provide a power-up of less than one second.

RUN/$\overline{HALT}$ A debounced input to allow halt and Single Step control modes. A HIGH input allows the CPU to run. A LOW input forces the $\overline{WAIT}$ output LOW causing the CPU to enter continuous wait states until the ZCK period after RUN/$\overline{HALT}$ is returned to HIGH.

SSNO, SSNC Single Step control inputs. These debounced input allow the CPU to Single Step from one wait state to the next by momentarily disconnecting SSNC from ground and grounding SSNO. RUN/$\overline{HALT}$ must be LOW for Single Step operation.

ST_1, ST_2, ST_3 Status inputs from AmZ8000 CPU's and peripherals. Continuous LOW inputs indicate that the CPU is executing "internal operation" or "refresh." During this time the time out is disabled to avoid signaling an inappropriate interrupt. The status inputs are subject to the set-up and hold time requirements of the $\overline{WAIT}$ latch.

X_1, X_2 External crystal connections (see application section). X_1 may be driven directly by a TTL input.

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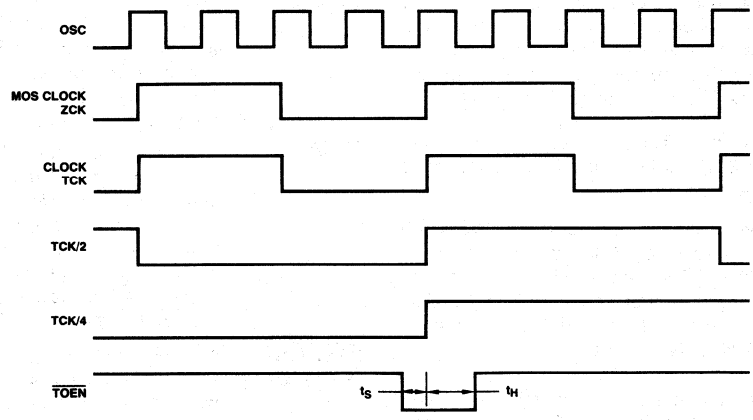
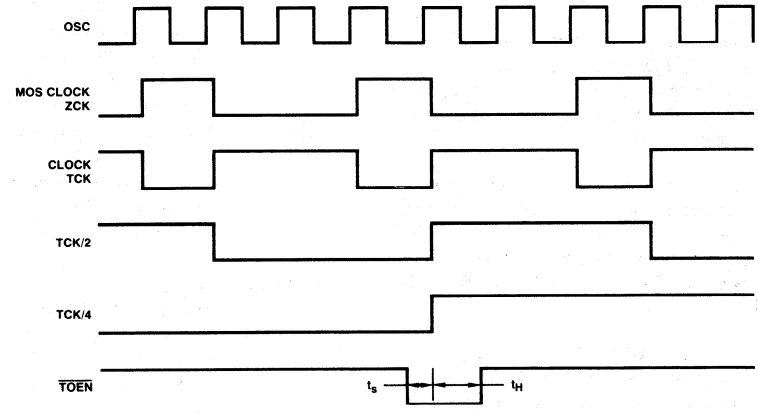
Am8127 CLOCK OUTPUTS
DIVIDE BY 4 MODE (AmZ8000)



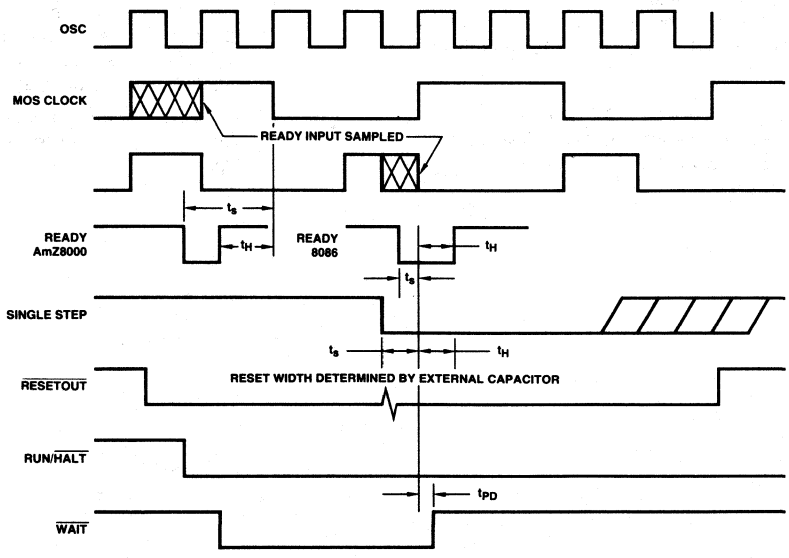
AMZ-024

DIVIDE BY 3 MODE (8086)



AMZ-025

Am8127 READY, WAIT, RESET, AND SINGLE STEP



AMZ-026

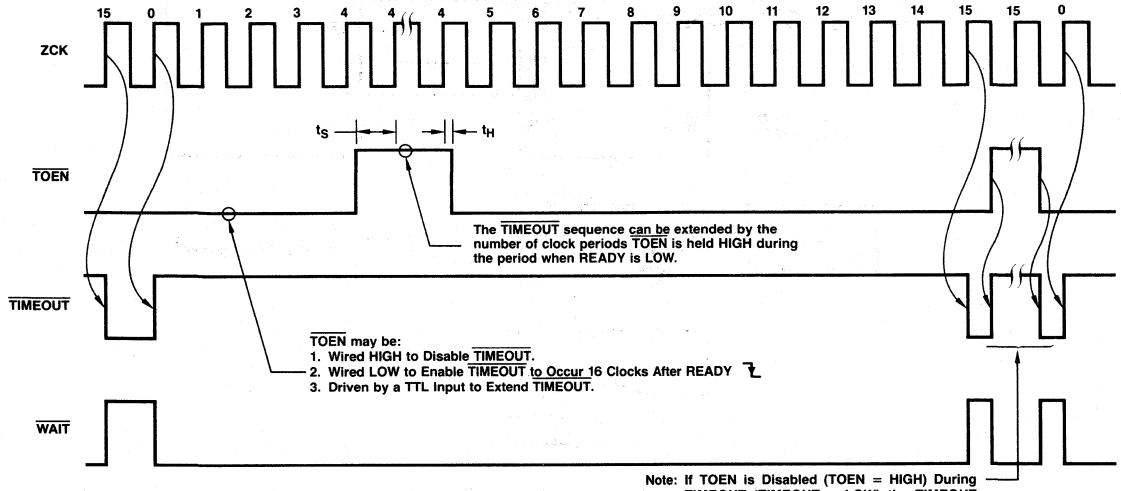
TYPICAL CRYSTAL SPEC

Mode	Fundamental AT cut
Resonance	Parallel or Series
Load	32pF (Net of 56pF C's shown + stray C)
Stability	±0.01% (or to user requirement)

$\overline{\text{WAIT}}$, $\overline{\text{TIMEOUT}}$ FUNCTION TABLE

RUN/$\overline{\text{HALT}}$	SSNC	ST_3	ST_2	ST_1	READY	$\overline{\text{TOEN}}$	$\overline{\text{TIMEOUT}}$ COUNTER	$\overline{\text{TIMEOUT}}$	$\overline{\text{WAIT}}$
H	X	L	L	L	H	X	Cleared	H	H
		L	L	L	L	X	Hold	H	L
		Any ST_i = H			H	L	Cleared	H	H
					L	H	Count + 1 on ZCK ↓	H until 15 clocks after ready ↓, then LOW one ZCK period	L until 15 clocks after ready ↓, then LOW one ZCK period
L	L	X			X	X	Hold	H	L
	H								HIGH one ZCK period

$\overline{\text{TIMEOUT}}$ COUNTER TIMING



AMZ-027

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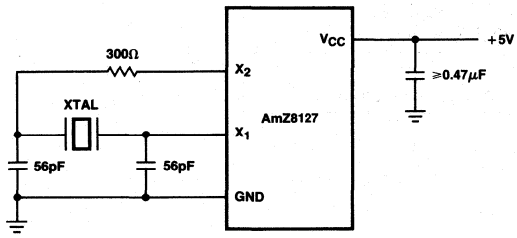
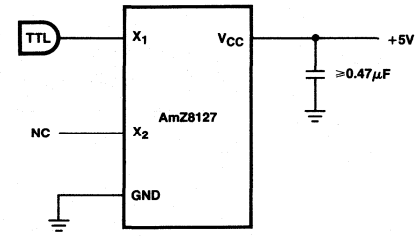
CRYSTAL CONTROLLED OSCILLATOR



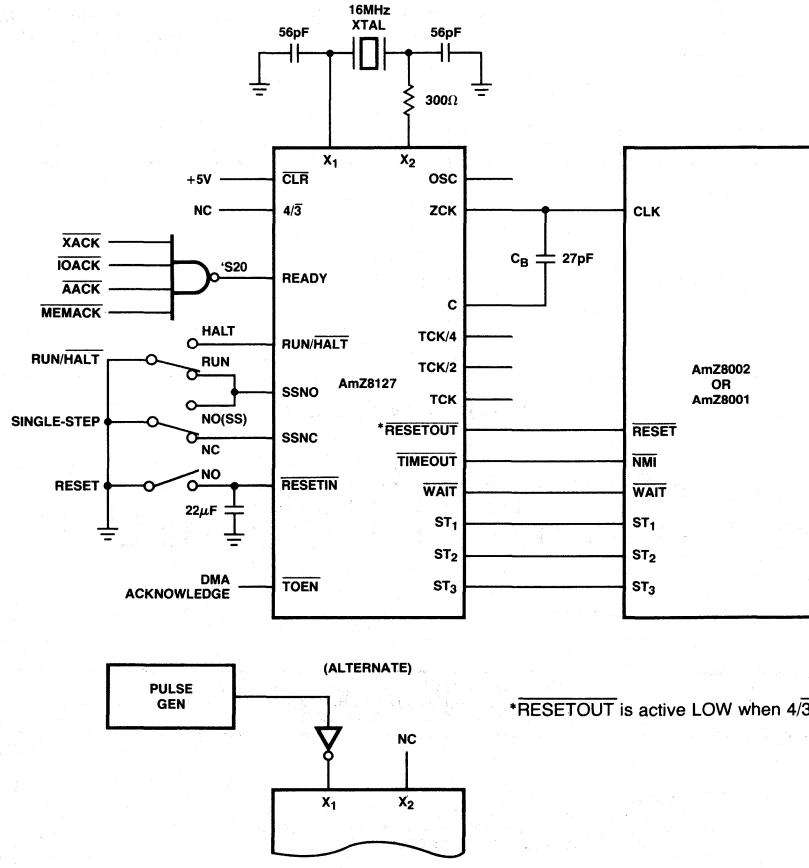
AMZ-028

EXTERNAL CLOCK DRIVE



AMZ-029

AmZ8000 APPLICATION
(50% Duty Cycle ZCK)

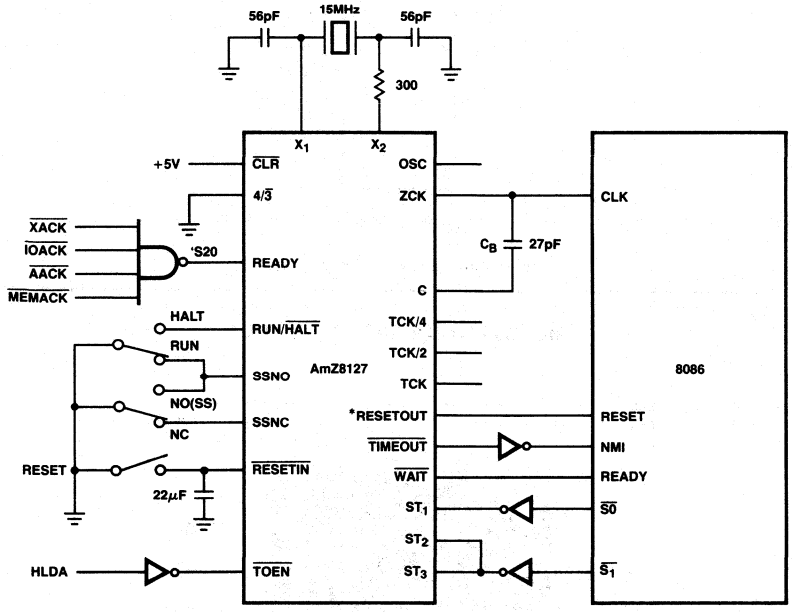


*$\overline{\text{RESETOUT}}$ is active LOW when 4/$\overline{3}$ = HIGH

AMZ-030

The typical operating configuration for AmZ8127 is shown above. The component values shown provide a 4MHz clock output for the AmZ8002 CPU. The 27pF capacitor from C to ZCK is a bootstrap to ensure clock rise to $V_{CC}-0.4V$ within the specified rise time. The 22μF reset capacitor is chosen to guarantee reset, plus adequate delay for reset during power-up with a slowly rising V_{CC} supply voltage. Ground SSNO if RUN/$\overline{\text{HALT}}$ or S-S isn't used.

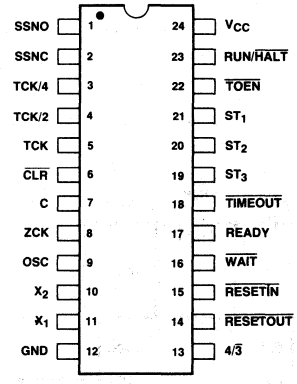
8086 APPLICATION
(33% Duty Cycle ZCK)



AMZ-031

*RESETOUT is active HIGH when 4/$\overline{3}$ = LOW

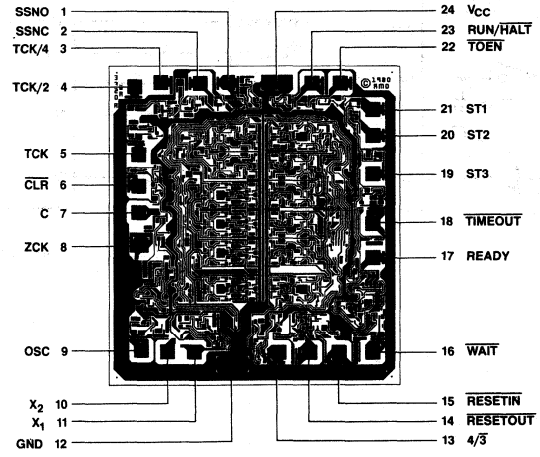
CONNECTION DIAGRAM
Top View



24 Pin 0.3" wide

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.098" X 0.088"

Am3212•Am8212

Eight-Bit Input/Output Port

istinctive Characteristics

Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.

4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.

Input load current 250μA max.

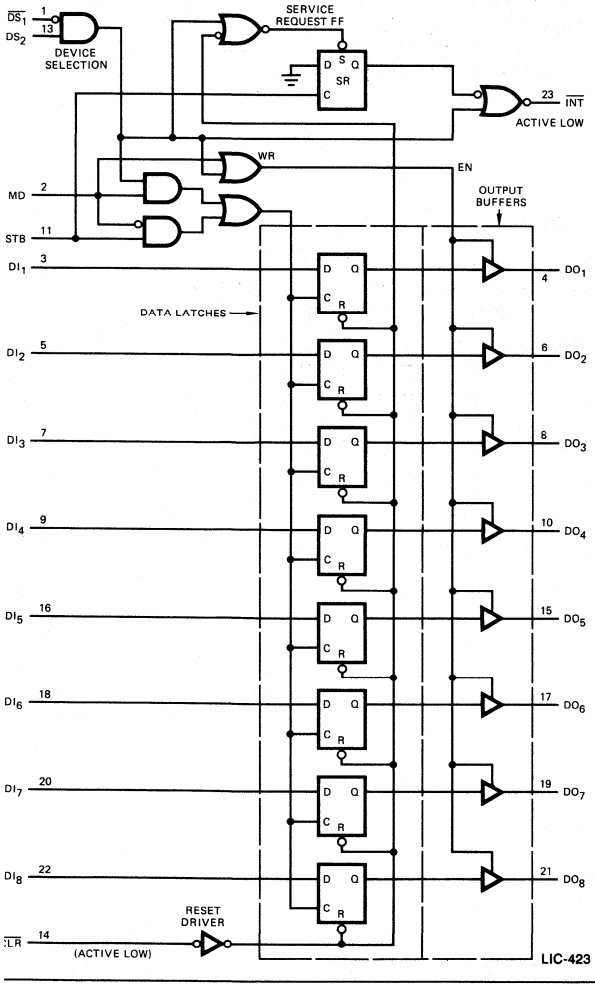
Reduces system package count

- Available for operation over both commercial and military temperature ranges.
- Advanced Schottky processing with 100% reliability assurance testing in compliance with MIL-STD-883.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

FUNCTIONAL DESCRIPTION

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am3212 • Am8212. The Am3212 • Am8212 input/output port consists of an 8-latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

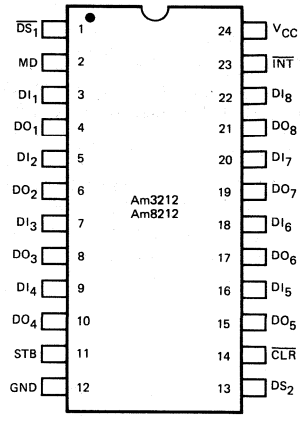
LOGIC DIAGRAM



LIC-423

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-424

PIN DEFINITION

$DI_1 - DI_8$	DATA IN
$DO_1 - DO_8$	DATA OUT
$\overline{DS_1} - DS_2$	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM8212DM
Hermetic DIP	0°C to +70°C	D8212
Molded DIP	0°C to +70°C	P8212
Dice	0°C to +70°C	AM8212XC
Hermetic DIP	0°C to +70°C	D3212
Hermetic DIP	–55°C to +125°C	MD3212
Molded DIP	0°C to +70°C	P3212

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FUNCTIONAL DESCRIPTION (Cont'd)

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$)).

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state). This high-impedance state allows the Am3212 • Am8212 to be connected directly onto the microprocessor bi-directional data bus.

Control Logic

The Am3212 • Am8212 has control inputs $\overline{DS_1}$, DS_2, MD And STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS_1}$, DS_2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS_1}$ is low and DS_2 is high ($\overline{DS_1} \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS_1} \cdot DS_2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS_1} \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The SR flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS_1} \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

TRUTH TABLE

STB	MD	$\overline{DS_1} - DS_2$	Data Out Equals
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

CLR	$\overline{DS_1} - DS_2$	STB	SR*	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	↘	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↘	1	0

$\overline{CLR}$ — Resets Data Latch
— Sets SR Flip-Flop (no effect on Output Buffer)
* Internal SR Flip-Flop

IAXIMUM RATINGS (Above which the useful life may be impaired)

torage Temperature	−65°C to +150°C
emperature (Ambient) Under Bias	−55°C to +125°C
upply Voltage	−0.5V to +7.0V
utput Voltage	−0.5V to +7.0V
iput Voltages	−1.0V to +5.5V
utput Current (Each Output)	125mA

LECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

212, D8212, P3212, D3212 (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ± 5%
n8212DM, MD3212 (MIL) T_A = −55°C to +125°C V_{CC} = 5.0V ± 10%

C CHARACTERISTICS

rameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_F	Input Load Current ACK, DS_2, CR, DI_1 – DI_8 Inputs	V_F = 0.45V				−0.25	mA
I_F	Input Load Current MD Input	V_F = 0.45V				−0.75	mA
I_F	Input Load Current DS_1 Input	V_F = 0.45V				−1.0	mA
I_R	Input Leakage Current ACK, DS, CR, DI_1 – DI_8 Inputs	V_R = 5.25V				10	µA
I_R	Input Leakage Current MO Input	V_R = 5.25V				30	µA
I_R	Input Leakage Current DS_1 Input	V_R = 5.25V				40	µA
V_C	Input Forward Voltage Clamp	I_C = −5.0mA	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage		COM'L			0.85	Volts
			MIL			0.80	
V_{IH}	Input HIGH Voltage			2.0			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 15mA				0.45	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0mA	COM'L	3.65	4.0		Volts
			MIL	3.3	4.0		
		I_{OH} = −0.5mA	MIL	3.4	4.0		
I_{SC}	Short Circuit Output Current	V_O = 0V		−15		−75	mA
$\|I_O\|$	Output Leakage Current High Impedance	V_O = 0.45V/5.25V				20	µA
I_{CC}	Power Supply Current	Note 2			90	130	mA

C CHARACTERISTICS (Note 3)

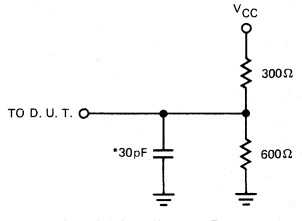
rameters	Description	Min.	Typ. (Note 1)	Max.	Units
t_{pw}	Pulse Width	30	8		ns
t_{pd}	Data to Output Delay		12	30	ns
t_{we}	Write Enable to Output Delay		18	40	ns
t_{set}	Data Set-up Time	15			ns
t_h	Data Hold Time	20			ns
t_r	Reset to Output Delay		18	40	ns
t_s	Set to Output Delay		15	30	ns
t_e	Output Enable/Disable Time		14	45	ns
t_c	Clear to Output Delay		25	55	ns

APACITANCE (Note 4)

= 1.0MHz, V_{BIAS} = 2.5V, V_{CC} = +5.0V, T_A = 25°C

rameters	Description	Typ.	Max.	Units
C_{IN}	DS_1 MD Input Capacitance	9.0	12	pF
C_{IN}	DS_2, CK, ACK, DI_1–DI_8 Input Capacitance	5.0	9.0	pF
C_{OUT}	DO_1–DO_8 Output Capacitance	8.0	12	pF

TEST LOAD (15mA and 30pF)



*Including Jig and Probe Capacitance.

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tes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. CLR = STB = HIGH; DS_1 = DS_2 = MD = LOW; all data inputs are gound, all data outputs are open.
3. Conditions of Test: a) Input pulse amplitude = 2.5V
b) Input rise and fall times 5.0ns
c) Between 1.0V and 2.0V measurements made at 1.5V with 15mA and 30pF Test Load.
4. This parameter is sampled and not 100% tested.

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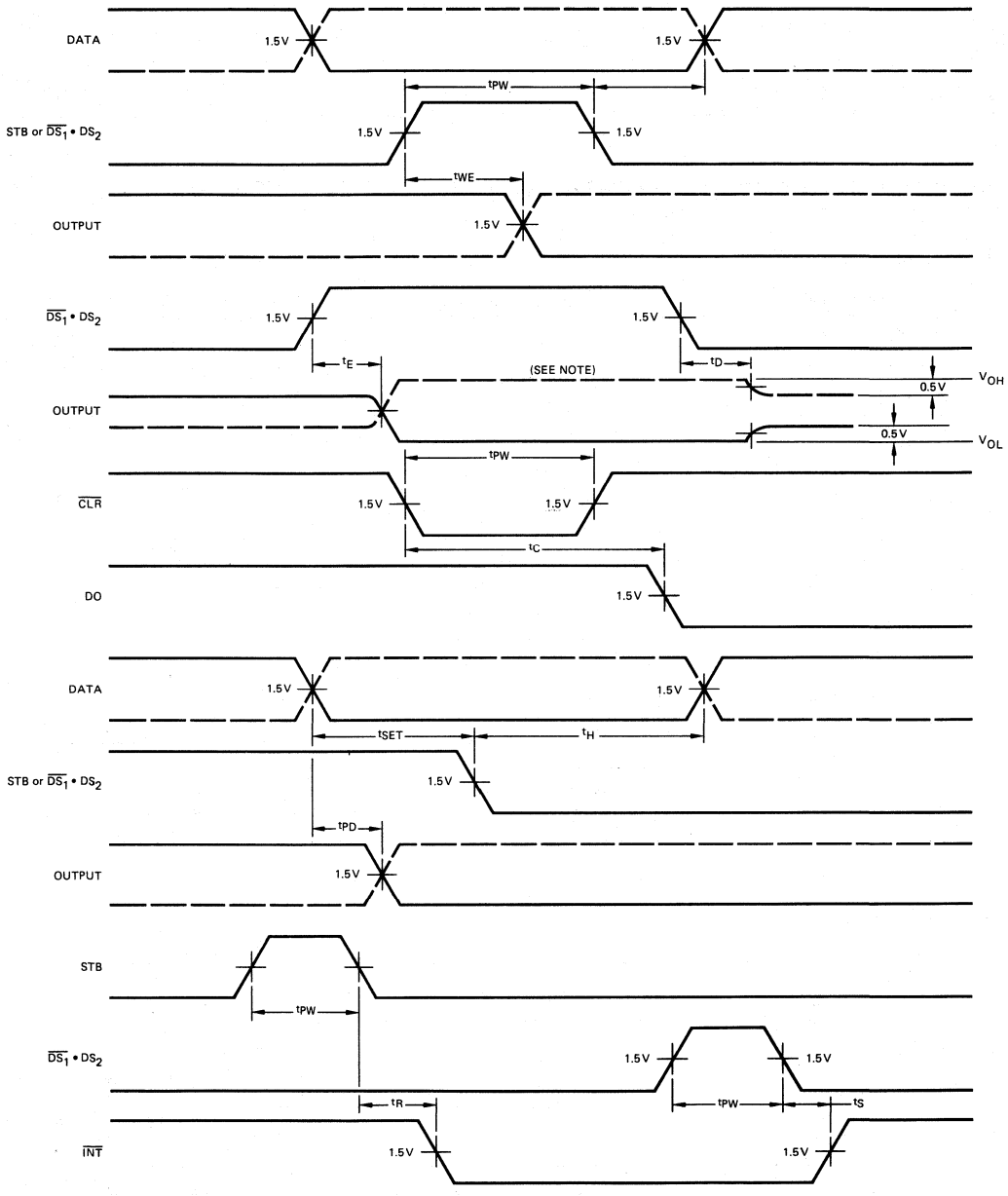
TIMING DIAGRAM



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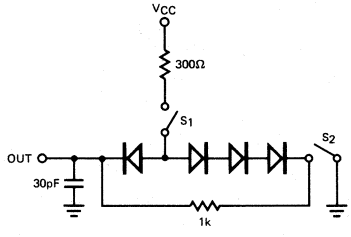
Note: Alternative Test Load.



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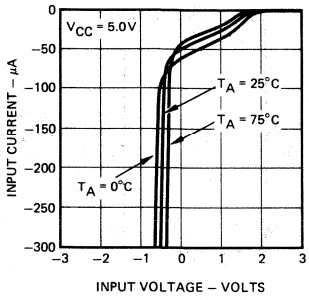
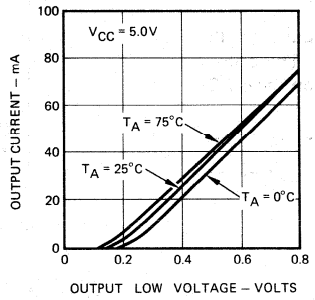
TYPICAL CHARACTERISTICS

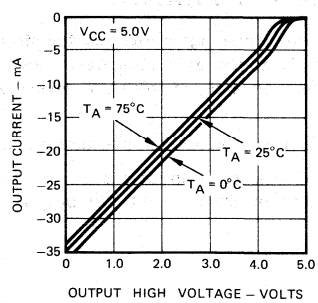
Input Current Versus Input Voltage



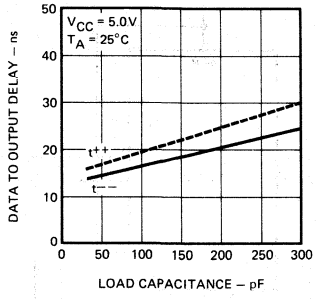
Output Current Versus Output LOW Voltage



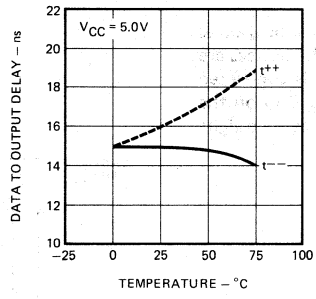
Output Current Versus Output HIGH Voltage



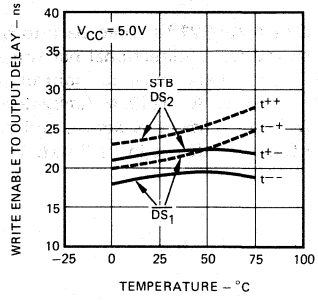
Data to Output Delay Versus Load Capacitance



Data to Output Delay Versus Temperature



Write Enable to Output Delay Versus Temperature



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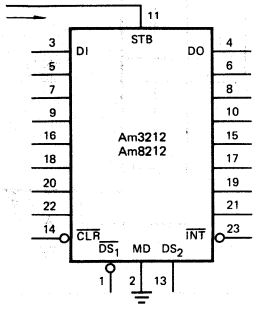
LOGIC SYMBOLS

INPUT DEVICE

Detailed



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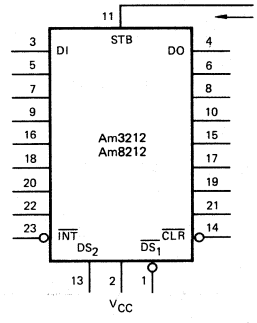
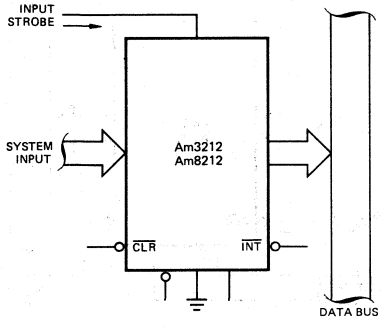
OUTPUT DEVICE

Detailed



LIC-430

Symbolic



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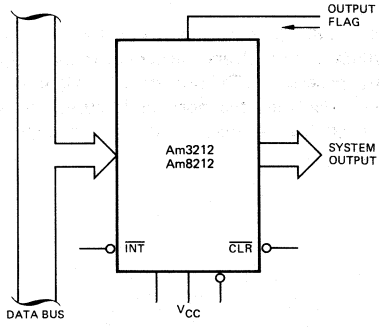

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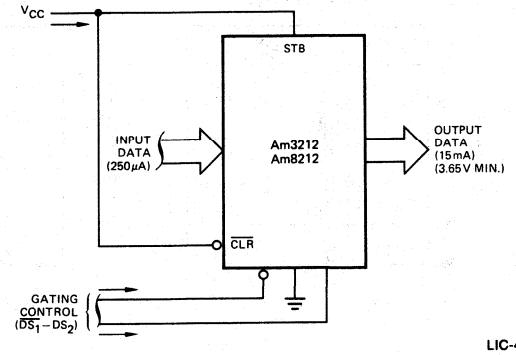
TYPICAL APPLICATIONS OF THE Am8212

GATED BUFFER (3-STATE)

By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS_1}$ and DS_2.

When the device selection logic is false, the outputs are 3-state.

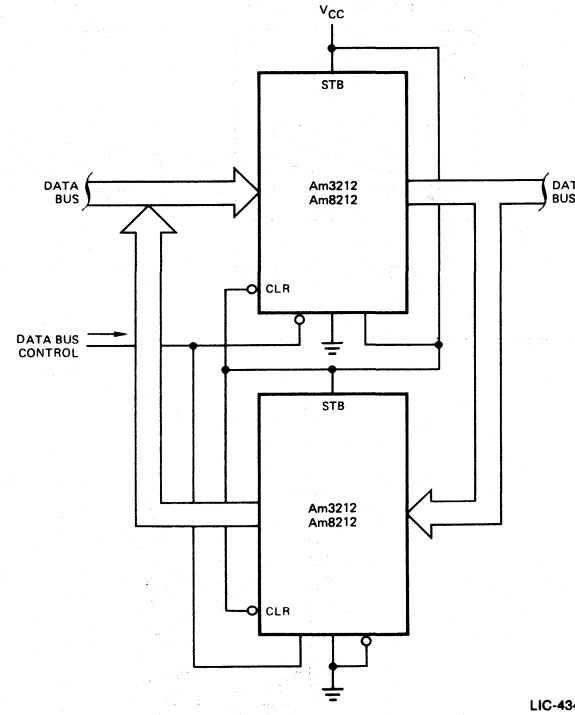
When the device selection logic is true, the input data from the system is directly transferred to the output.



LIC-433

Bi-Directional Bus Driver

Two Am3212 • Am8212's wired back-to back can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS_1}$ on the first Am3212 • Am8212 and to DS_2 on the second. While one device is active, and acting as a straight through buffer the other is in its 3-state mode.



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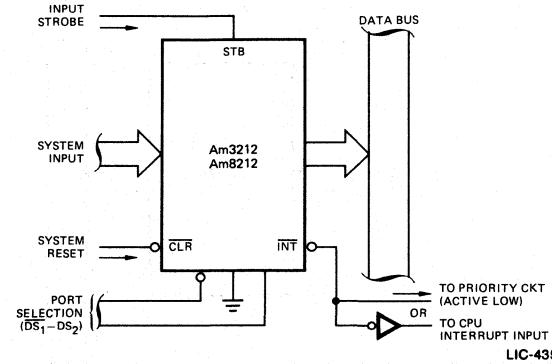
Interrupting Input Port

The Am3212 • Am8212 accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true — enabling the system input data onto the data bus.

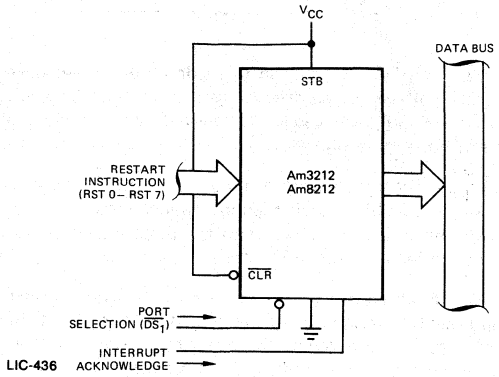


LIC-435

TYPICAL APPLICATIONS OF THE Am8212 (Cont'd)

Interrupt Instruction Port

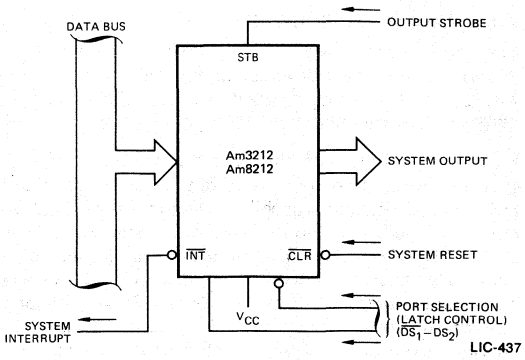
The Am3212 • Am8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS_1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).



LIC-436

Output Port (With Hand-Shaking)

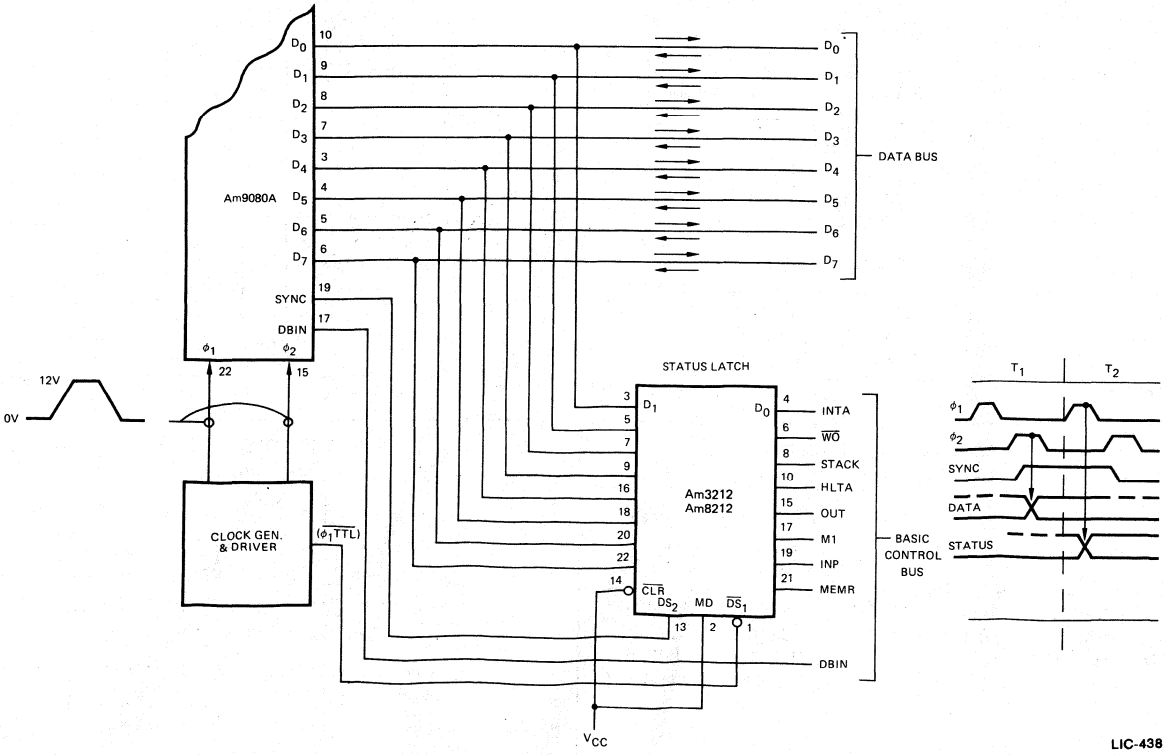
The Am3212 • Am8212 is used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of date. The selection of the port comes from the device selection logic. ($\overline{DS_1} \cdot DS_2$).



LIC-437

Am9080A Status Latch

The input to the Am3212 • Am8212 latch comes directly from the Am9080A data bus. Timing shows that when the SYNC signal is true ($\overline{DS_1}$ input), and $\phi 1$ is true, ($\overline{DS_1}$ input) then the status data will be latched into the Am3212 • Am8212. The mode signal is tied high so that the output on the latch is active and evabled all the time.



LIC-438

Am8216 • Am8226

Four-Bit Parallel Bidirectional Bus Driver

Distinctive Characteristics

- Data bus buffer driver for 8080 type CPU's
- Low input load current – 0.25mA maximum
- High output drive capability for driving system data bus – 50mA at 0.5V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Am8216 has non-inverting outputs
- Output high voltage compatible with direct interfac to MOS
- Three-state outputs
- Advanced Schottky processing
- Available in military and commercial temperatur range
- Am8226 has inverting outputs

FUNCTIONAL DESCRIPTION

The Am8216 and Am8226 are four-bit, bi-directional bus drivers for use in bus oriented applications. The non-inverting Am8216, and inverting Am8226 drivers are provided for flexibility in system design.

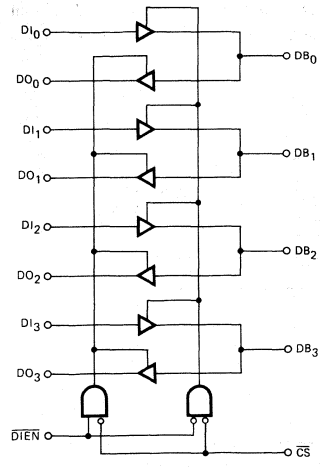
Each buffered line of the four bit driver consists of two separate buffers that are three-state to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "LOW" the device is enabled and the direction of the data flow is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the direction of data flow which is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

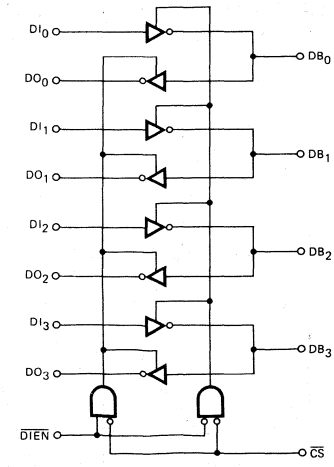
LOGIC DIAGRAMS

Am8216



LIC-439

Am8226



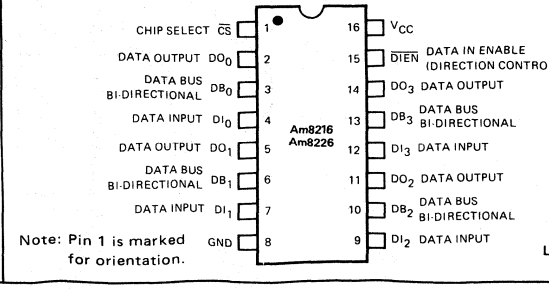
LIC-440

ORDERING INFORMATION

Package Type	Temperature Range	Am8216 Order Number	Am8226 Order Number
Hermetic DIP	–55°C to +125°C	MD8216	MD8226
Hermetic DIP	0°C to +70°C	D8216	D8226
Molded DIP	0°C to +70°C	P8216	P8226
Dice	0°C to +70°C	AM8216XC	AM8226XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-441

IAXIMUM RATINGS (Above which the useful life may be impaired)

emperature (Ambient) Under Bias	−55°C to +125°C
orage Temperature	−65°C to +150°C
H Output and Supply Voltages	−0.5 V to +7.0 V
II Input Voltages	−1.0 V to +5.5 V
utput Currents	125 mA

m8216 AND Am8226 MILITARY

LECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (−55°C to +125°C)

he following conditions apply unless otherwise specified:

D8216, MD8226 (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

C CHARACTERISTICS

arameters	Description		Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		$V_F = 0.45$			−0.15	−0.5	mA
I_{F2}	Input Load Current All Other Inputs		$V_F = 0.45$			−0.08	−0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		$V_R = 5.5V$				80	μA
I_{R2}	Input Leakage Current DI Inputs		$V_R = 5.5V$				40	μA
V_C	Input Forward Voltage Clamp		$I_C = -5.0mA$				−1.2	Volts
V_{IL}	Input LOW Voltage	Am8216					0.95	Volts
		Am8226					0.9	
V_{IH}	Input HIGH Voltage				2.0			Volts
I_O	Output Leakage Current (Three-State)	DO	$V_O = 0.45V/5.5V$				20	μA
		DB					100	
I_{CC}	Power Supply Current	Am8216				95	130	mA
		Am8226				85	120	
V_{OL1}	Output LOW Voltage		DO Outputs $I_{OL} = 15mA$ DB Outputs $I_{OL} = 25mA$			0.3	0.45	Volts
V_{OL2}	Output LOW Voltage		DB Outputs $I_{OL} = 45mA$			0.5	0.6	Volts
V_{OH1}	Output HIGH Voltage		DO Outputs	$I_{OH} = -0.5mA$	3.4	4.0		Volts
				$I_{OH} = -2.0mA$	2.4			
V_{OH2}	Output HIGH Voltage		DB Outputs $I_{OH} = -5.0mA$		2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V, $V_{CC} = 5.0V$		−15	−35	−65	mA
			DB Outputs = 0V, $V_{CC} = 5.0V$		−30	−75	−120	

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (−55°C to +125°C)

arameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		$C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am8216	$C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$		20	33	ns
		Am8226			16	25	
t_E	Output Enable Time	Am8216	Note 2		45	75	ns
		Am8226	Note 3		35	62	
t_D	Output Disable Time	Am8216	Note 4		20	40	ns
		Am8226			16	38	

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Am8216 AND Am8226 COMMERCIAL ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (0°C to +70°C)

The following conditions apply unless otherwise specified:

D8216, D8226, P8216, P8226 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

DC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		$V_F = 0.45$		−0.15	−0.5	mA
I_{F2}	Input Load Current All Other Inputs		$V_F = 0.45$		−0.08	−0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		$V_R = 5.25V$			20	μA
I_{R2}	Input Leakage Current DI Inputs		$V_R = 5.25V$			10	μA
V_C	Input Forward Voltage Clamp		$I_C = -5.0mA$			−1.0	Volts
V_{IL}	Input LOW Voltage					0.95	Volts
V_{IH}	Input HIGH Voltage			2.0			Volts
$\|I_O\|$	Output Leakge Current (Three-State)	DO	$V_O = 0.45V/5.5V$			20	μA
		DB				100	
I_{CC}	Power Supply Current	Am8216			95	130	mA
		Am8226			85	120	
V_{OL1}	Output LOW Voltage		DB Outputs $I_{OL} = 15mA$ DB Outputs IOL = 25mA		0.3	0.45	Volts
V_{OL2}	Output LOW Voltage	Am8216	DB Outputs $I_{OL} = 55mA$		0.5	0.6	Volts
		Am8226	DB Outputs $I_{OL} = 50mA$		0.5	0.6	
V_{OH1}	Output HIGH Voltage		DO Outputs $I_{OH} = -1.0mA$ COM'L	3.65	4.0		Volts
V_{OH2}	Output HIGH Voltage		DB Outputs $I_{OH} = -10mA$	2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V	−15	−35	−65	mA
			DB Outputs $V_{CC} = 5.0V$	−30	−75	−120	

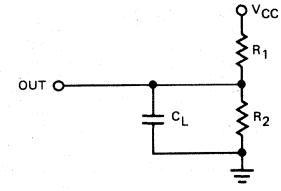
AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (0°C to +70°C)

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		$C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am8216	$C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$		20	30	ns
		Am8226			16	25	
t_E	Output Enable Time	Am8216	Note 2		45	65	ns
		Am8226	Note 3		35	54	
t_D	Output Disable Time		Note 4		20	35	ns

TEST CONDITIONS

Input pulse amplitude of 2.5V.
Input rise and fall times of 5.0ns between 1.0 and 2.0 volts.
Output loading is 5.0mA and 10pF.
Speed measurements are made at 1.5V levels.

TEST LOAD CIRCUIT



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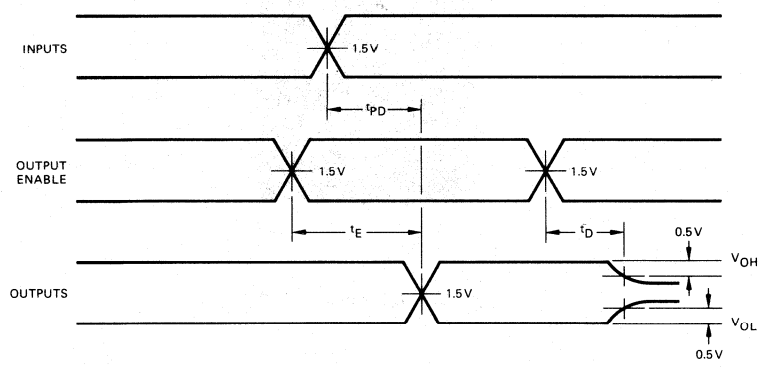
CAPACITANCE (Note 5)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz		4.0	8.0	pF
C_{OUT1}	Output Capacitance			6.0	10	pF
C_{OUT2}	Output Capacitance			13	18	pF

Notes: 1. Typical values are for T_A = 25°C, V_{CC} = 5.0 V.
2. DO outputs, C_L = 30 pF, R_1 = 300/10 kΩ, R_2 = 180/1.0 kΩ; DB outputs, C_L = 300 pF, R_1 = 90/10 kΩ, R_2 = 180/1.0 kΩ.
3. DO outputs, C_L = 30 pF, R_1 = 300/10 kΩ, R_2 = 600/1.0 kΩ; DB outputs, C_L = 300 pF, R_1 = 90/10 kΩ, R_2 = 180/1.0 kΩ.
4. DO outputs, C_L = 5.0 pF, R_1 = 300/10 kΩ, R_2 = 600/1.0 kΩ; DB outputs, C_L = 5.0 pF, R_1 = 90/10 kΩ, R_2 = 180/1.0 kΩ.
5. This parameter is periodically sampled and not 100% tested.

SWITCHING WAVEFORMS



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FUNCTION TABLE

$\overline{DIEN}$	$\overline{CS}$		8216 DB	8216 DO	8226 DB	8226 DO
L	L	DI ⇒ DB	DI	Z	$\overline{DI}$	Z
H	L	DB ⇒ DO	Z	DB	Z	$\overline{DB}$
L	H		Z	Z	Z	Z
H	H		Z	Z	Z	Z

H = HIGH
L = LOW

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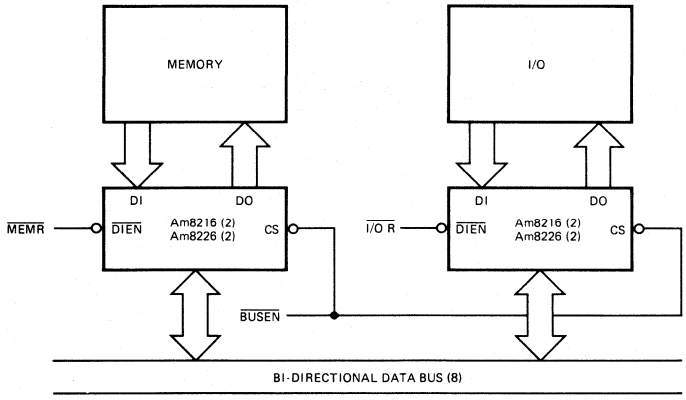
TYPICAL APPLICATION



MEMORY AND I/O INTERFACE TO A BI-DIRECTIONAL BUS

LIC-445

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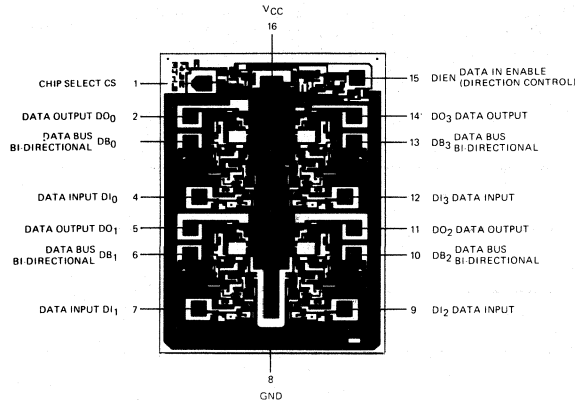
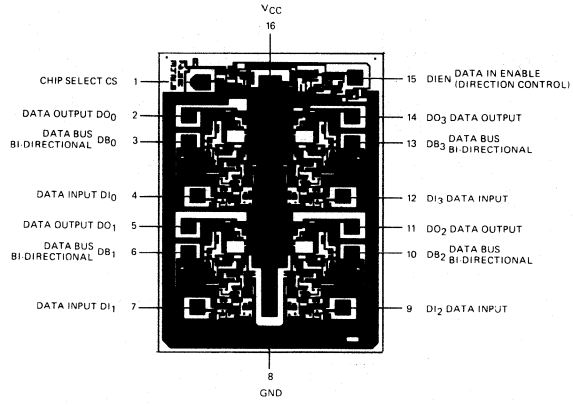
Metallization and Pad Layout

Am8216



DIE SIZE 0.066" X 0.090"

Am8226



DIE SIZE 0.066" X 0.090"

Am8224

Clock Generator and Driver for 8080A Compatible Microprocessors

istinctive Characteristics

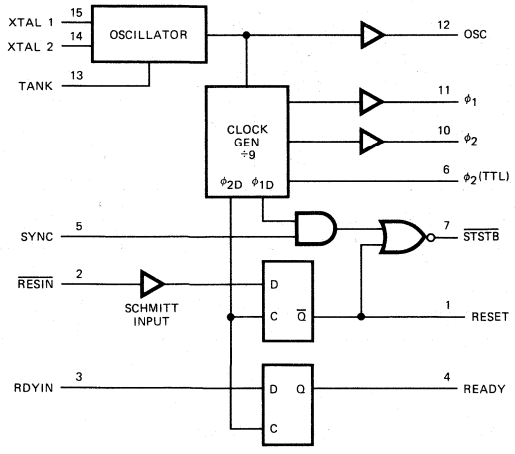
Single chip clock generator/driver for 8080A compatible CPU
Power-up reset for CPU
Ready synchronizing flip-flop
Status strobe signal
Oscillator output for external system timing
Am8224-4 version available for use with 1μsec instruction cycle of Am9080A-4

- Available for operation over both commercial and military temperature ranges
- Crystal controlled for stable system operation
- Reduces system package count
- Advanced Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am8224 is a single chip Clock Generator/Driver for the Am9080A and 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions, including a power-up reset, status strobe and synchronization of ready. Also provided are TTL compatible oscillator and ϕ_2 outputs for external system timing. The Am8224 provides the designer with a significant reduction of packages used to generate clocks and timing for the Am9080A or 8080A for both commercial and military temperature range applications. A high speed version, the Am8224-4, is available for use with the high speed Am9080A-4.

LOGIC DIAGRAM



LIC-619

ORDERING INFORMATION

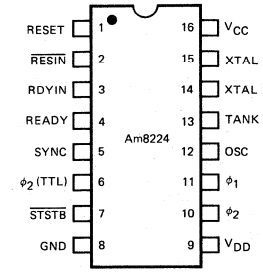
Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM8224DM
Hermetic DIP	0°C to +70°C	D8224
Molded DIP	0°C to +70°C	AM8224PC
Dice	0°C to +70°C	AM8224XC
Hermetic DIP	0°C to +70°C	AM8224-4DC*

* For use with Am9080A-4 with clock period between 250ns and 320ns.

PIN DEFINITION

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
ϕ_2(TTL)	ϕ_2 CLK (TTL LEVEL)
V_{CC}	+5.0V
V_{DD}	+12V
GND	0V
$\overline{\text{RESIN}}$	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
$\overline{\text{STSTB}}$	STATUS STB (ACTIVE LOW)
ϕ_1	Am9080A/8080A CLOCKS
ϕ_2	

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	
V_{CC}	7.5V
V_{DD}	15V
Maximum Output Current ϕ_1 and ϕ_2 (Note 1)	100mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am8224XC, Am8224-4XC (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% V_{DD} = 12V ± 5%
Am8224XC (MIL) T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% V_{DD} = 12V ± 10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 2)	Max.	Units
I_F	Input Current Loading	V_F = 0.45V				−0.25	mA
I_R	Input Leakage Current	V_R = 5.25V				10	µA
V_C	Input Forward Clamp Voltage	I_C = −5.0mA	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage	V_{CC} = 5.0V				0.8	Volts
V_{IH}	Input HIGH Voltage	Reset input	COM'L	2.6	2.2		Volts
			MIL	2.8	2.2		
		All other inputs		2.0			
V_{IH}-V_{IL}	$\overline{RESIN}$ Input Hysteresis	V_{CC} = 5.0V		0.25	0.5		Volts
V_{OL}	Output LOW Voltage	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} = 2.5mA				0.45	Volts
		All other inputs I_{OL} = 15mA				0.45	
V_{OH}	Output HIGH Voltage	ϕ_1, ϕ_2; I_{OH} = −100µA	COM'L	9.4	11		Volts
			MIL	V_{DD} −1.6V	V_{DD} −1.0V		
		READY, RESET; I_{OH} = −100µA	COM'L	3.6	4.0		
			MIL	3.35	4.0		
		All other outputs; I_{OH} = −1.0mA		2.4	3.0		
I_{SC}	Output Short Circuit Current (All Low Voltage Outputs Only)	V_O = 0V V_{CC} = 5.0V		−10		−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 3)			70	115	mA
I_{DD}	Power Supply Current	V_{DD} = MAX.			5.0	12	mA

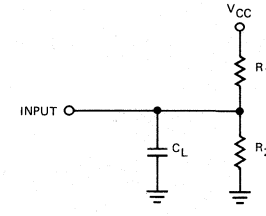
Notes: 1. Caution: ϕ_1 and ϕ_2 outputs do not have short circuit protection.
2. Typical limits are at V_{CC} = 5.0V, V_{DD} = 12V, 25°C ambient and maximum loading.
3. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

CRYSTAL REQUIREMENTS

Tolerance: .005% at 0°C - 70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With frequency in excess of 18MHz use 3rd overtone XTALs and tank circuit.

TEST CIRCUIT



LIC-621

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

			Am8224XM			Am8224XC			Am8224-4XC (Note 2)			
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	C_L=20pF to 50pF	$\frac{2t_{CY}}{9}-23ns$			$\frac{2t_{CY}}{9}-20ns$			45			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		$\frac{5t_{CY}}{9}-35ns$			$\frac{5t_{CY}}{9}-35ns$			110			
t_{D1}	ϕ_1 to ϕ_2 Delay		0			0			0			
t_{D2}	ϕ_2 to ϕ_1 Delay		$\frac{2t_{CY}}{9}-17ns$			$\frac{2t_{CY}}{9}-14ns$			35			
t_{D3}	ϕ_1 to ϕ_2 Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}+22ns$	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}+20ns$	55		76	
t_r	ϕ_1 and ϕ_2 Rise Time				20			20			20	
t_f	ϕ_1 and ϕ_2 Fall Time				20			20			20	
$t_{D\phi 2}$	ϕ_2 to ϕ_2(TTL) Delay	ϕ_2(TTL), C_L = 30pF, R_1 = 300Ω, R_2 = 600Ω	−5.0		15	−5.0		15	−5.0		15	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\overline{STSTB}$, C_L = 15pF, R_1 = 2.0kΩ, R_2 = 4.0kΩ	$\frac{6t_{CY}}{9}-33ns$		$\frac{6t_{CY}}{9}$	$\frac{6t_{CY}}{9}-30ns$		$\frac{6t_{CY}}{9}$	137		167	ns
t_{PW}	$\overline{STSTB}$ Pulse Width		$\frac{t_{CY}}{9}-18ns$			$\frac{t_{CY}}{9}-15ns$			18			
t_{DRS}	RDYIN Set-up Time to Status Strobe		$50ns-\frac{4t_{CY}}{9}$			$50ns-\frac{4t_{CY}}{9}$			−61			
t_{DRH}	RDYIN Hold Time After STSTB		$\frac{4t_{CY}}{9}$			$\frac{4t_{CY}}{9}$			111			
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	Ready and Reset C_L = 10pF, R_1 = 2.0kΩ, R_2 = 4.0kΩ	$\frac{4t_{CY}}{9}-25ns$			$\frac{4t_{CY}}{9}-25ns$			86			ns
t_{CLK}	CLK Period			$\frac{t_{CY}}{9}$			$\frac{t_{CY}}{9}$			28		
$f_{Max.}$	Maximum Oscillating Frequency		27			28.12			36			MHz
C_{in}	Input Capacitance	V_{CC} = 5.0V, V_{DD} = 12V, V_{BIAS} = 2.5V, f = 1.0MHz			8.0			8.0			8.0	pF

AC CHARACTERISTICS (For t_{CY} = 488.28ns)

T_A = 0°C to +70°C V_{CC} = +5.0V ±5% V_{DD} = +12V ±5%

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	ϕ_1 and ϕ_2 Loaded, C_L = 20 to 50pF	89			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		236			ns
t_{D1}	Delay ϕ_1 to ϕ_2		0			ns
t_{D2}	Delay ϕ_2 to ϕ_1		95			ns
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay		296		326	ns
$t_{D\phi 2}$	ϕ_2 to ϕ_2(TTL) Delay		−5.0		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-up Time to $\overline{STSTB}$	Ready and Reset Loaded, C_L = 20 to 50pF, R_1 = 2.0kΩ, R_2 = 4.0kΩ	−167			ns
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$		217			ns
t_{DR}	Ready or Reset to ϕ_2 Delay		192			ns
FREQ	Oscillator Frequency				18.432	MHz

Notes: 1. All measurements referenced to 1.5V unless specified otherwise.
2. Am8224-4 parameter limits are given for t_{CY} = 250ns or an oscillating frequency of 36MHz. Between 28.12MHz and 36MHz min. and max. limits should be ratioed between the calculated Am8224XC limits at 28.12MHz and the given 36MHz parameter limits.

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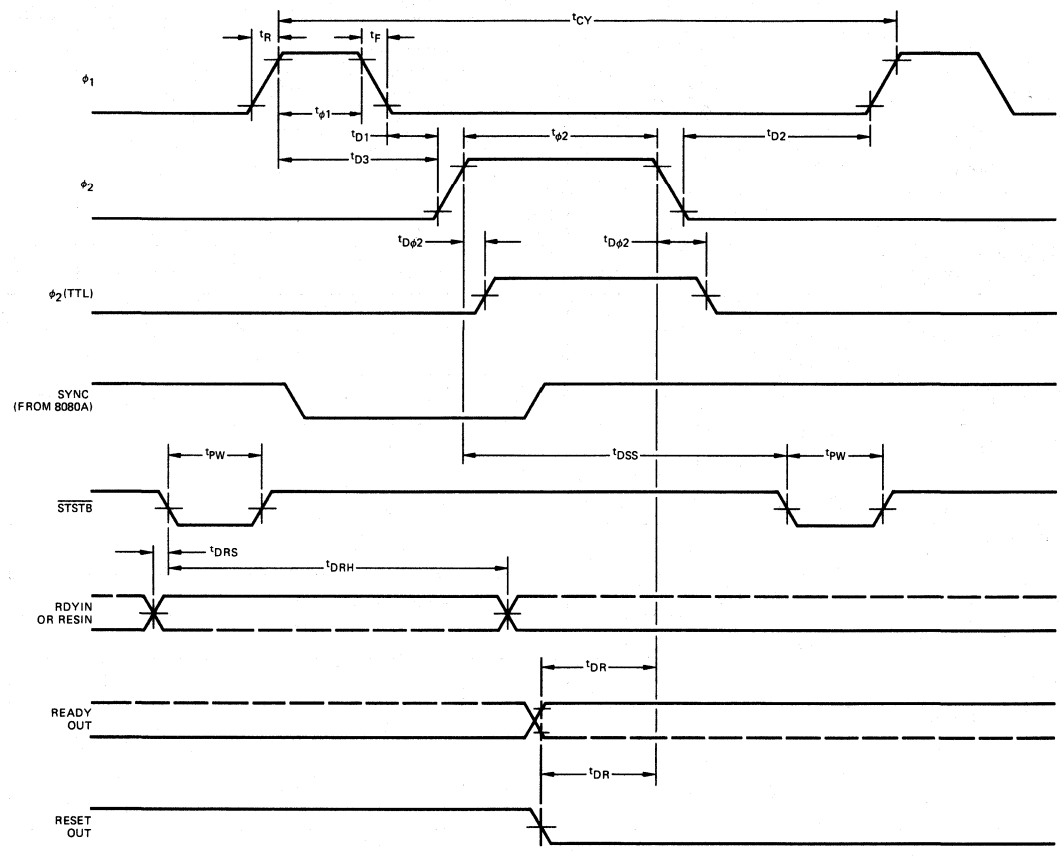
SWITCHING WAVEFORMS



Voltage measurement points: ϕ_1, ϕ_2 Logic "0" = 1.0 V, Logic "1" = 8.0 V.
All other signals measured at 1.5 V.

LIC-622

Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the CPU is to be run. Basically, the oscillator operates at 9 times the desired processor speed.

The formula to determine the crystal frequency is:

$$f(XTAL) = \frac{1}{tCY} \text{ times } 9$$

When using crystals above 10MHz a small amount of frequency "trimming" is necessary to produce the desired frequency. The addition of a selected capacitance (20pF – 30pF) in series with the crystal will accomplish this function.

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has a much lower output at its rated frequency and has a tendency to oscillate at its fundamental.

To avoid the unwanted oscillation and increase the desired frequency output it is necessary to provide a parallel tuned resonant circuit of low impedance. The external LC network is connected to the TANK input and is AC coupled. See typical application with Am8228 and Am9080A in Figure 2.

The formula for the LC network is:

$$F = \frac{1}{2\pi \sqrt{LC}}$$

The output of the oscillator is buffered and brought out on OSC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

Clock Generator

The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; ϕ_1 and ϕ_2, can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be derived.

The outputs of the clock generator are connected to two high level drivers for direct interface to the CPU. A TTL level phase 2 is also brought out ϕ_2 (TTL) for external timing purposes. It is especially useful in DMA dependent activities. This signal is used to gate the requesting device onto the bus once the CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe ($\overline{STSTB}$) is achieved.

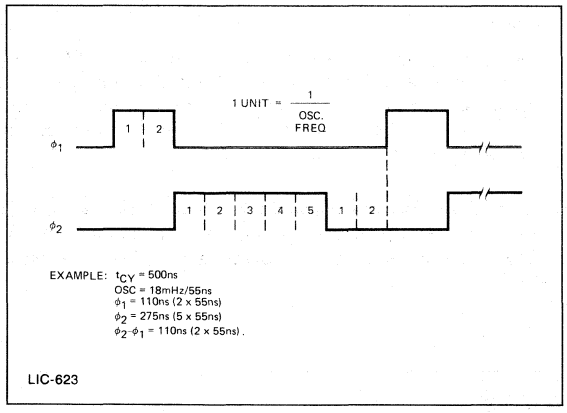


Figure 1. Clock Generator Waveforms.

$\overline{STSTB}$ (Status Strobe)

At the beginning of each machine cycle the CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal (ϕ_{1A}), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The $\overline{STSTB}$ signal connects directly to the Am8228 System Controller.

The power-on Reset also generates $\overline{STSTB}$, but of course, for a longer period of time. This feature allows the Am8228 to be automatically reset without additional pins devoted for this function.

Power-On Reset and Ready Flip-Flops

A common function in microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The Am8224 has a built-in feature to accomplish this feature.

An external RC network is connected to the $\overline{RESIN}$ input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with ϕ_{2D} (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the microprocessor input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the RESIN input in addition to the power-on RC network.

The READY input to the CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flip-flop is required. The Am8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with ϕ_{2D}, a synchronized READY signal at the correct input level, can be connected directly to the CPU.

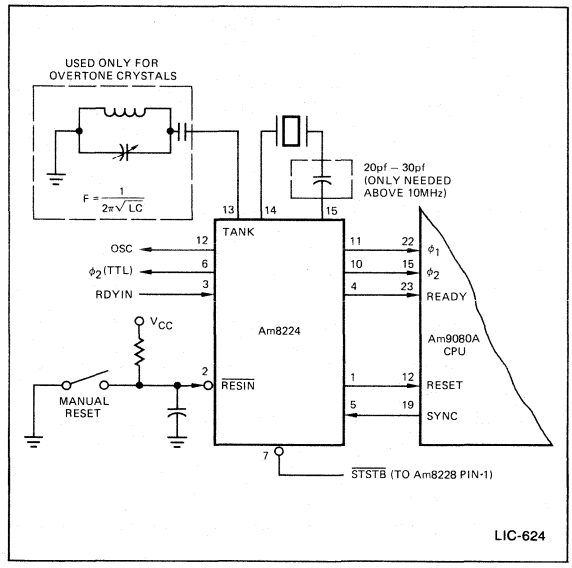


Figure 2. Typical Application with Am8224 and Am9080A.

APPLICATION PRECAUTIONS WHEN USING Am8224 UP TO 36MHz

Usage with Third Harmonic Crystal or Am9080A-4

The use of the Am8224 with a third harmonic crystal requires a minor modification to the external circuitry associated with the Am8224. The changes are as follows:

– Series capacitor in conjunction with the xtal
– Adding a tuned circuit in the "tank" lead
– Tuning of circuit to proper frequency

It is necessary to maintain the crystal activity to a proper level if an xtal controlled circuit is to operate properly. A 20-30pfd capacitor placed in series will help achieve this level in third overtone crystal, while helping to suppress the fundamental mode. The Am8224 has an auxiliary port provided to allow for a tuned circuit. This tuned circuit eliminates the tendency of the circuit to oscillate at the crystal's fundamental. The tank or tuned circuit must have the following properties:

1. It must be parallel resonant at the crystal frequency (third order).
2. The off resonance impedance must be low enough to spoil the AC gain of the Am8224.
3. The circuit must be DC decoupled (or returned to V_{CC}) at a low impedance (substantially below 100Ω).

All frequency determining components must be in close proximity to the Am8224. Insert crystal and tune tank for best waveform at Pin 12 (OSC). If counter is available, adjust for match of crystal marking. The circuit in Figure 3 will accomplish the above result for the 36MHz range.

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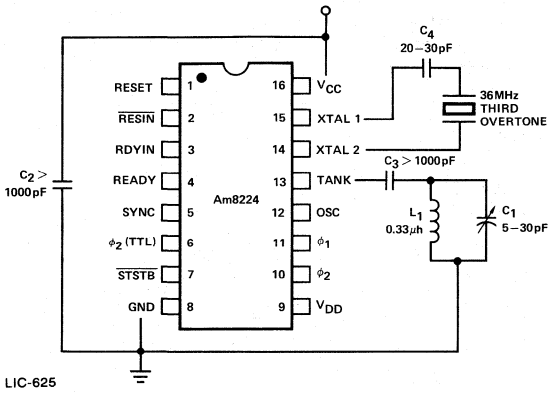


Figure 3.

C_1 = E.F. Johnson
275-0430-005
5-30pF Trimmer or Equiv.

L_1 = J.W. Miller Inductor
9230-08

V_{CC} Ground

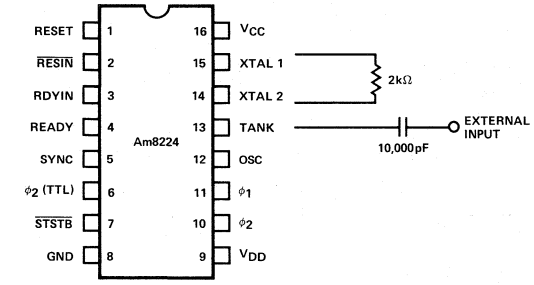
Due to the nature of our device (fast switching, higher voltage) it is necessary to provide a bypass capacitor from V_{CC} to ground in the immediate proximity of the Am8224. This insures proper operation of the device while reducing noise spiking on adjacent circuits.

Resin Bypass

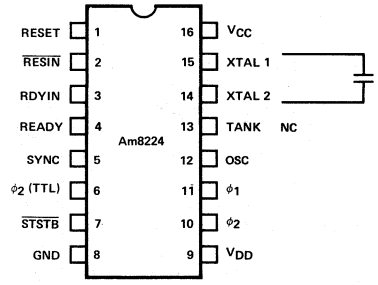
The use of a high impedance capacitor for timing R-C, and/or timing components remotely located from the Am8224 device may cause a disturbance to occur during the linear transition region. The capacitor for this function should be of the ceramic type and a value of 1000pF or greater.

This can be cured by placing a >1000pfd ceramic capacitor from Resin (Pin 2) to Ground (Pin 8) in the immediate proximity of the device. This will allow the timing R-C to be placed at will.

APPLICATIONS

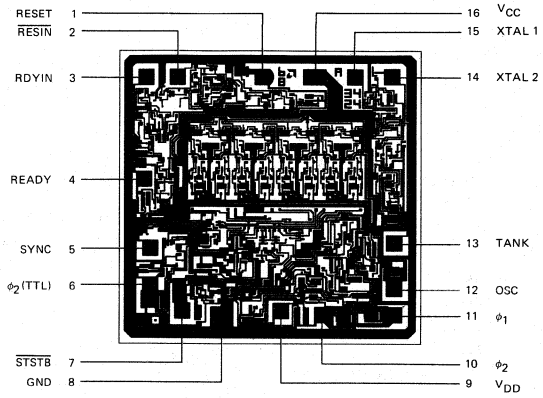


The Am8224 can be driven from an external source of frequency by connecting as shown and driven with approximately 500mV over a wide frequency range.



The Am8224 can oscillate without a xtal by placing a small value capacitor (10→200pF) in place of a crystal.

Metallization and Pad Layout



DIE SIZE 0.085" X 0.084"

Am8228 • Am8238

System Controller and Bus Driver for 8080A Compatible Microprocessors

Distinctive Characteristics

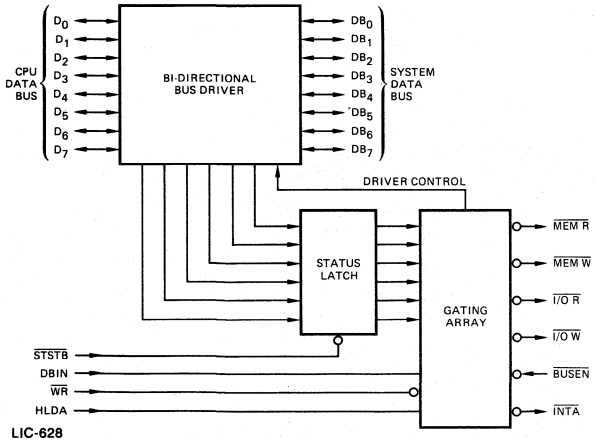
- Multi-byte instruction interrupt acknowledge
- Selectable single level vectored interrupt (RST-7)
- 28-pin molded or hermetic DIP package
- Single chip system controller and data bus driver for Am9080/8080A systems
- Am8238-4 high speed version available for use with 1μsec instruction cycle of Am9080A-4
- Bi-directional three-state bus driver for CPU independent operation
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in military and commercial temperature range
- Am8238 has extended $\overline{IOW}/\overline{MEMW}$ pulse width

FUNCTIONAL DESCRIPTION

The Am8228 and Am8238 are single chip System Controller Data Bus drivers for the Am9080A Microcomputer System. They generate all control signals required to directly interface Am9080A/8080A compatible system circuits (memory and I/O) to the CPU.

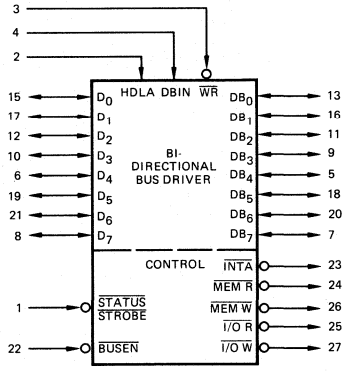
Bi-directional bus drivers with three-state outputs are provided for the system data bus, facilitating CPU independent bus operations such as direct memory access. Interrupt processing is accommodated by means of a single vectored interrupt or by means of the standard 8080A multiple byte interrupt vector operation.

LOGIC DIAGRAM



LIC-628

LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

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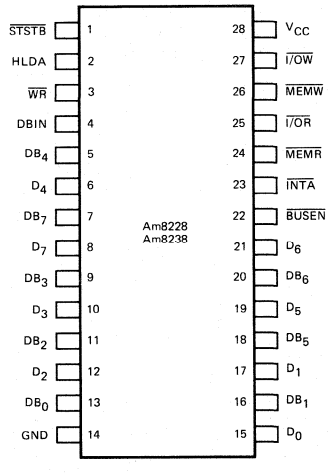
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-630

ORDERING INFORMATION

Package Type	Temperature Range	Am8228 Order Number	Am8238 Order Number
Molded DIP	0°C to +70°C	AM8228PC	AM8238PC
Hermetic DIP	0°C to +70°C	D8228	D8238
Hermetic DIP	−55°C to +125°C	AM8228DM	AM8238DM
Dice	0°C to +70°C	AM8228XC	AM8238XC
Hermetic DIP	0°C to +70°C		AM8238-4DC*
Molded DIP	0°C to +70°C		AM8238-4PC*

*For use with Am9080A-4 with minimum clock period of 250ns.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Volatge to Ground Potential (Pin 28 to Pin 14) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−1.5V to +7.0V
DC Output Current, Into Outputs	50mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Noted:

Am8228XM, Am8238XM: T_A = −55°C to +125°C; V_{CC}MIN. = 4.50V; V_{CC}MAX. = 5.50V
Am8228XC, Am8238XC, Am8238-4XC: T_A = 0°C to +70°C; V_{CC}MIN. = 4.75V; V_{CC}MAX. = 5.25V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 2)				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −10μA	D_0–D_7	MIL	3.35	3.8		Volts
					COM'L	3.6	3.8		
			I_{OH} = −1.0mA	All other outputs		2.4			
V_{OL}	Output Low Voltage	V_{CC} = MIN.	I_{OL} = 2.0mA	D_0–D_7				0.45	Volts
			I_{OL} = 10mA	All other outputs				0.45	
V_C	Input Clamp Voltage (All Inputs)	V_{CC} = MIN., I_C = −5.0mA					−0.75	−1.0	Volts
V_{TH}	Input Threshold Voltage (All Inputs)	V_{CC} = 5.0V				0.8		2.0	Volts
I_F	Input Load Current	V_{CC} = MAX., V_F = 0.45V		$\overline{STSTB}$				−500	μA
				D_2 and D_6				−750	
				All other inputs				−250	
I_R	Input Leakage Current	V_{CC} = MAX., V_R = 5.25V		DB_0–DB_7				20	μA
				All other inputs				100	
I_{INT}	INTA Current	See INTA test circuit						5.0	mA
$I_{O(OFF)}$	Offstate Output Current (All Control Outputs)	V_{CC} = MAX., V_O = 5.25V						100	μA
		V_O = 0.45V						−100	
I_{OS}	Short Circuit Current (All Outputs)	V_{CC} = 5.0V				−15		−90	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.					140	190	mA

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

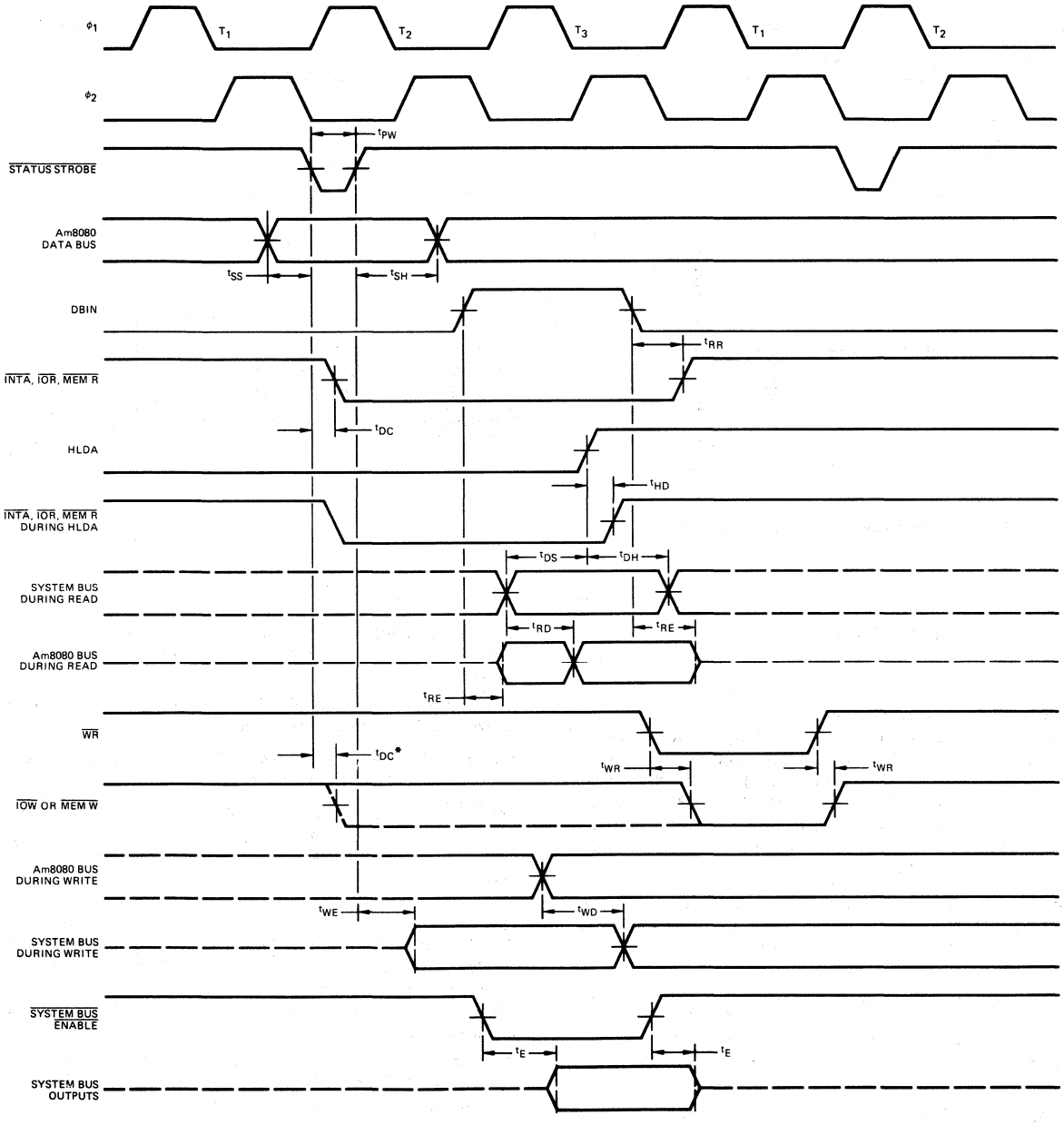
Parameters	Description	Test Conditions	Am8228XM/ Am8238XM Min.	Typ. (Note 1)	Max.	Am8228XC/ Am8238XC Min.	Typ. (Note 1)	Max.	Am8238-4XC Min.	Typ. (Note 1)	Max.	Units
t_{PW}	Width of Status Strobe		22			22			22			ns
t_{SS}	Set-up Time, Status Inputs D_0-D_7		12			8.0			8.0			ns
t_{SH}	Hold Time, Status Inputs D_0-D_7		5.0			5.0			5.0			ns
t_{DC}	Delay from $\overline{STSTB}$ to $\overline{MEMR}$	C_L = 100pF	20	30	60	20	30	60	20	30	40	ns
	Delay from $\overline{STSTB}$ to $\overline{INTA}$, $\overline{IOR}$		20	30	60	20	30	60	20	30	45	
	Delay from $\overline{STSTB}$ to all other Control Signals		20	30	60	20	30	60	20	30	60	
t_{RR}	Delay from DBIN to Control Outputs			15	35		15	30		15	30	ns
t_{RE}	Delay from DBIN to 8080A Bus — Enable	C_L = 25pF		25	45		25	45		12	20	ns
	Delay from DBIN to 8080A Bus — Disable			25	45		25	45		25	35	
t_{RD}	Delay from System Bus to 8080A Bus During Read			15	30		15	30		15	20	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	C_L = 100pF	5.0	20	45	5.0	20	45	5.0	20	45	ns
t_{WE}	Delay to Enable System Bus DB_0-DB_7 After $\overline{STSTB}$			25	36		25	30		25	30	ns
t_{WD}	Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 During Write		5.0	20	40	5.0	20	40	5.0	20	40	ns
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7			25	35		25	30		20	30	ns
t_{HD}	HLDA to Read Status Outputs			15	28		15	25		15	25	ns
t_{DS}	Set-up Time, System Bus Inputs to HLDA		10			10			10			ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		20			20			20			ns

Notes: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under electrical characteristics for the applicable device type.

CAPACITANCE (This parameter is periodically sampled and not 100% tested.)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5V, V_{CC} = 5.0V T_A = 25°C, f = 1.0MHz		8.0	12	pF
C_{OUT}	Output Capacitance Control Signals			7.0	15	pF
I/O	I/O Capacitance (D or DB)			8.0	15	pF

SWITCHING WAVEFORMS



Voltage measurements points: D_0–D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*Extended $\overline{IOW}/\overline{MEMW}$ for Am8238 only.

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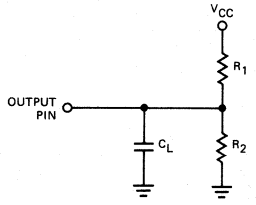
TEST CIRCUITS



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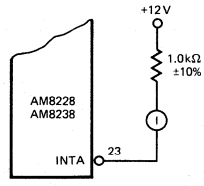
Note 1. For D_0-D_7: $R_1 = 4.0k\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$.
For all other outputs: $R_1 = 500\Omega$, $R_2 = 1.0k\Omega$, $C_L = 100pF$.



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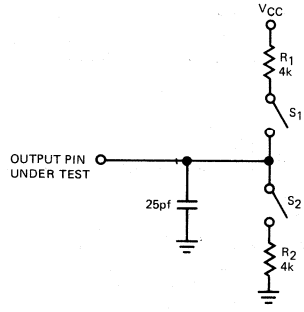
INTA (for RST 7)



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Test Circuit for DBIN to 8080A BUS

t_{RE}	S_1	S_2
Enable 8080 bus, HIGH-Z to logic "0"	Closed	Open
Enable 8080 bus, HIGH-Z to logic "1"	Open	Closed
Disable 8080 bus, logic "0" to HIGH-Z	Closed	Open
Disable 8080 bus, logic "1" to HIGH-Z	Open	Closed

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver: An eight-bit, bi-directional bus driver is provided to buffer the Am9080A/8080A data bus from Memory and I/O devices. The Am9080A data bus has an input requirement of *3.0 volts (min) and can drive (sink) a current of at least 3.2mA. The Am8228 • Am8238 data bus driver matches these input requirements and provides enhanced noise immunity. The output drive is set for 10mA typical for Memory and I/O devices.

The Bi-Directional Bus Drive is controlled by signals from the Gating Array for proper bus flow and the outputs can be forced to high impedance state (three-state) for DMA activities.

Status Latch: The Am8228 • Am8238 stores the status information in the Status Latch when the $\overline{STSTB}$ input goes "LOW". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

Gating Array: The Gating Array generates control signals ($\overline{MEM\ R}$, $\overline{MEM\ W}$, $\overline{I/O\ R}$, $\overline{I/O\ W}$ and $\overline{INTA}$) by gating the outputs of the Status Latch Am9080A signals; i.e., DBIN, WE, and HLDA.

*The 8080A has an input requirement of 3.3V and can drive a maximum current of 1.9mA.

The "read" control signals (MEM R, I/O R and INTA) are derived by combinational logic from Status Bit and the DBIN input.

The "write" control signals (MEM W, I/O W) are similarly derived from the Status Bits and the WR input.

All Control Signals are "active LOW" and directly interface RAM, ROM and I/O components.

The $\overline{INTA}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the Am8228 • Am8238. If only one basic vector is needed in the interrupt structure, the Am8228 • Am8238 can automatically insert a RST 7 instruction onto the bus. To use this option, connect the INTA output of the Am8228 • Am8238 (pin 23) to the +12 volt supply through a series resistor (1k ohms). The voltage is sensed internally by the Am8228 • Am8238 and logic is "set-up" so that when the DBIN input is active, a RST 7 instruction is gated on to the bus when an interrupt is acknowledged.

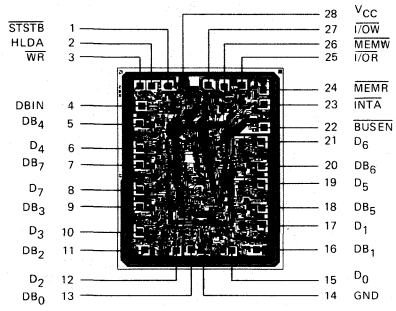
When using a multiple byte instruction as an Interrupt Instruction, the Am8228 • Am8238 will generate an INTA pulse for each of the instruction bytes.

The BUSEN (Bus Enable) input of the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "HIGH". If BUSEN is a "LOW", normal operation of the data buffer and control signals take place. This facilitates CPU independent bus operations such as direct memory access.

DEFINITION OF FUNCTIONAL TERMS

D_7-D_0	Data bus to-from Am9080A/8080A
DB_7-DB_0	Data bus to-from user system
$\overline{I/OR}$	Input/output read strobe output active LOW
$\overline{I/OW}$	Input/output write strobe output active LOW
$\overline{MEM\ R}$	Memory read strobe, output, active LOW
$\overline{MEM\ W}$	Memory write strobe, output, active LOW
DBIN	Data bus input strobe, input active HIGH
$\overline{INTA}$	Interrupt acknowledge strobe, input, active LOW
HLDA	Hold input from Am9080A/8080A active HIGH
$\overline{WR}$	Write input strobe, active HIGH
$\overline{BUSEN}$	BUS ENABLE INPUT, input, 3-state output control, active LOW for 3-state out
$\overline{STSTB}$	Status Strobe, input, strobes status on data bus into status latch, active LOW

Metallization and Pad Layout



DIE SIZE 0.110" X 0.136"

LOADING RULES

Signal	Pin No.	Input Load	Output Sink	Output Source
D_0	15	250μA	2mA	−10μA
D_1	17	250μA	2mA	−10μA
D_2	12	750μA	2mA	−10μA
D_3	10	250μA	2mA	−10μA
D_4	6	250μA	2mA	−10μA
D_5	19	250μA	2mA	−10μA
D_6	21	750μA	2mA	−10μA
D_7	8	250μA	2mA	−10μA
DB_0	13	250μA	10mA	−1mA
DB_1	16	250μA	10mA	−1mA
DB_2	11	250μA	10mA	−1mA
DB_3	9	250μA	10mA	−1mA
DB_4	5	250μA	10mA	−1mA
DB_5	18	250μA	10mA	−1mA
DB_6	20	250μA	10mA	−1mA
DB_7	7	250μA	10mA	−1mA
$\overline{STSTB}$	1	500μA	–	–
DBIN	4	250μA	–	–
$\overline{WR}$	3	250μA	–	–
HLDA	2	250μA	–	–
$\overline{MEM\ R}$	24	–	10mA	−1mA
$\overline{MEM\ W}$	26	–	10mA	−1mA
$\overline{I/OR}$	25	–	10mA	−1mA
$\overline{IOW}$	27	–	10mA	−1mA
$\overline{BUSEN}$	22	250μA	–	–
$\overline{INTA}$	23	–	10mA	−1mA
GND	14			
V_{CC}	28			

STATUS WORD CHART

		TYPE OF MACHINE CYCLE										
Data Bus Bit	Status Information	Instruction Fetch	Memory Read	Memory Write	Stack Read	Stack Write	Input Read	Output Write	Interrupt Acknowledge	Halt Acknowledge	Interrupt Acknowledge While Halt	
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1	
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	1	1	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	
D_5	M_1	1	0	0	0	0	0	0	1	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	
D_7	MEM R	1	1	0	1	0	0	0	0	1	0	

CONTROL SIGNALS:
- ⑩ → $\overline{INTA}$
- ⑨ → $\overline{(NONE)}$
- ⑧ → $\overline{INTA}$
- ⑦ → $\overline{I/O\ W}$
- ⑥ → $\overline{I/O\ R}$
- ⑤ → $\overline{MEM\ W}$
- ④ → $\overline{MEM\ R}$
- ③ → $\overline{MEM\ W}$
- ② → $\overline{MEM\ R}$
- ① → $\overline{MEM\ R}$

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Am82S62

Nine-Input Parity Checker/Generator

Distinctive Characteristics

- ODD/EVEN parity outputs
- Inhibit input to disable both outputs
- High-speed expansion input – P_9
- PNP inputs
- Advanced Schottky technology
- 100% reliability assurance testing in compliance wit MIL-STD-883.

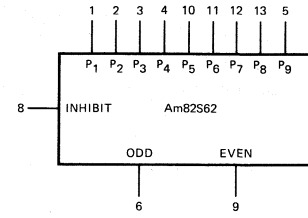
FUNCTIONAL DESCRIPTION

The Am82S62 is a 9-bit parity generator/parity checker with both an ODD parity output and an EVEN parity output. The device can be used to detect errors in data transmission or data retrieval systems as well as to generate this parity check bit.

The Am82S62 features one special high-speed input (P_9) to facilitate expansion. The propagation delay to the outputs through this path is considerably reduced when compared to the P_1 through P_8 paths. This short delay path allows parity checkers/generators of larger size than 9-bits to be built with a minimum of additional delay.

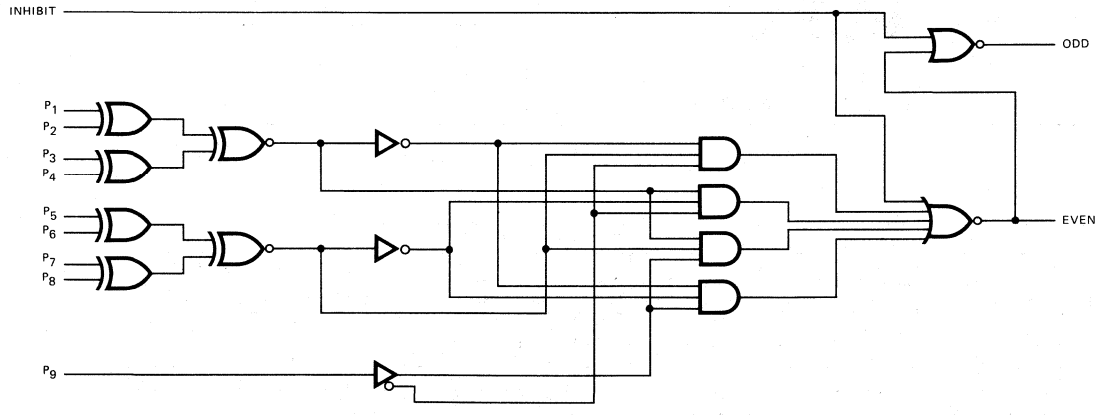
The device is built using advanced Schottky technology and incorporates PNP input transistors to reduce input loading to 0.4 STTL unit loads. The EVEN output is one gate propagation delay time shorter than the ODD output.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

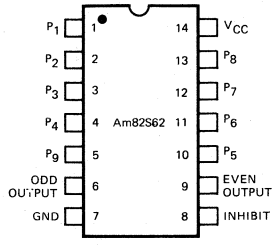
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	N82S62A
Hermetic DIP	0°C to +75°C	N82S62F
Dice	0°C to +75°C	N82S62X
Hermetic DIP	−55°C to +125°C	S82S62F
Dice	−55°C to +125°C	S82S62X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

IAXIMUM RATINGS (Above which the useful life may be impaired)

torage Temperature	−65°C to +150°C
emperature (Ambient) Under Bias	−55°C to +125°C
upply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5V to +7V
C Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
C Input Voltage	−0.5V to +5.5V
C Output Current, Into Outputs	30mA
C Input Current	−30mA to +5.0mA

:LECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

182S62 $T_A = 0°C$ to $+75°C$
:82S62 $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA $V_{IN} = V_{IH}$ or V_{IL}	S82	2.5			Volts
			N82	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA $V_{IN} = V_{IH}$ or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	P9			−0.4	mA
			Others			−0.8	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 4.5V				10	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				67	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. P_1 through P_9 grounded; inhibit at 4.5V; outputs open.

Switching Characteristics ($T_A = +25°C$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	P_1 through P_8 to Even Output	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15 pF			23	ns
t_{PLH} t_{PHL}	P_1 through P_8 to Odd Output				28	ns
t_{PLH} t_{PHL}	P_9 to Even Output				12	ns
t_{PLH} t_{PHL}	P_9 to Odd Output				18	ns
t_{PLH} t_{PHL}	Inhibit to Even Output				9	ns
t_{PLH} t_{PHL}	Inhibit to Odd Output				9	ns

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TRUTH TABLE

INHIBIT	NUMBER OF P INPUTS		OUTPUT	
	LOW	HIGH	ODD	EVEN
L	0	9	H	L
L	1	8	L	H
L	2	7	H	L
L	3	6	L	H
L	4	5	H	L
L	5	4	L	H
L	6	3	H	L
L	7	2	L	H
L	8	1	H	L
L	9	0	L	H
H	X	X	L	L

H = HIGH
L = LOW
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
P_1	1	0.4	–	–
P_2	2	0.4	–	–
P_3	3	0.4	–	–
P_4	4	0.4	–	–
P_9	5	0.2	–	–
ODD	6	–	20	10
GND	7	–	–	–
INHIBIT	8	0.4	–	–
EVEN	9	–	20	10
P_5	10	0.4	–	–
P_6	11	0.4	–	–
P_7	12	0.4	–	–
P_8	13	0.4	–	–
V_{CC}	14	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS

P_1 through P_9 The nine inputs to the parity tree.

INHIBIT A HIGH on the inhibit input forces both the odd output and even output LOW regardless of the P inputs. When the inhibit is LOW, the odd and even outputs will always be of opposite phase.

ODD The odd parity output of the device. When an odd number of P inputs are at a HIGH level, the odd output will be HIGH.

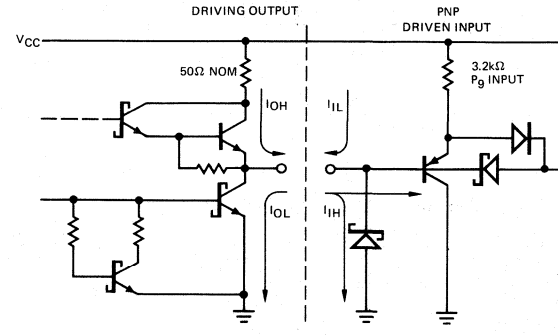
EVEN The even parity output of the device. When an even number of P inputs are at a HIGH level, the even output will be HIGH.

LOGIC EQUATIONS

ODD Output = $P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

EVEN Output = $\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$

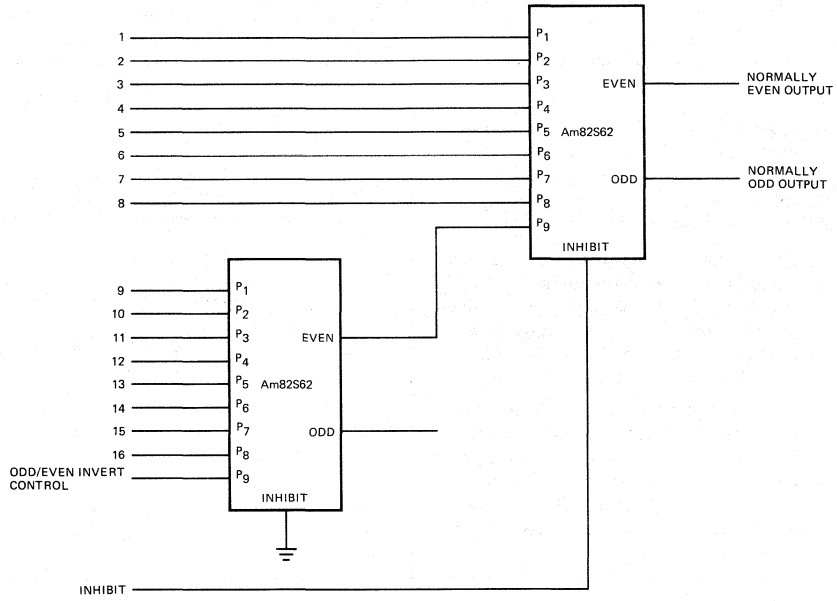
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



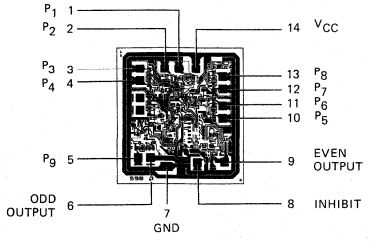
Note: Actual current flow direction shown.

APPLICATION

16-BIT PARITY GENERATOR WITH INVERT CONTROL



Metallization and Pad Layout



DIE SIZE 0.067" X 0.072"

12

Am8T26A•Am8T28

Schottky Three-State Quad Bus Driver/Receiver

Distinctive Characteristics

- Advanced Schottky technology
- 48mA driver sink current
- Three-state outputs on driver and reciever
- PNP inputs
- Am8T26A has inverting outputs
- Am8T28 has non-inverting outputs
- Driver propagation delay — 14ns max. for 8T26A, 17ns max. for 8T28
- Receiver propagation delay — 14ns max. for 8T26A, 17ns max. for 8T28
- 100% reliability assurance testing in compliance with MIL-STD-883

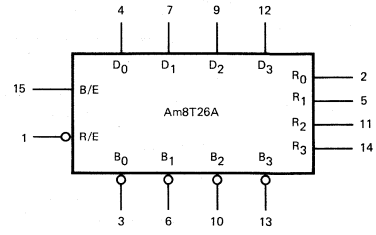
FUNCTIONAL DESCRIPTION

The Am8T26A/Am8T28 are high speed bus transceivers consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

A HIGH on the receiver enable (R/E) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

LOGIC SYMBOL

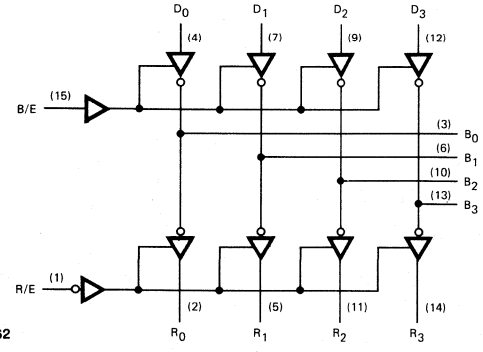


V_{CC} = Pin 16
GND = Pin 8

LIC-561

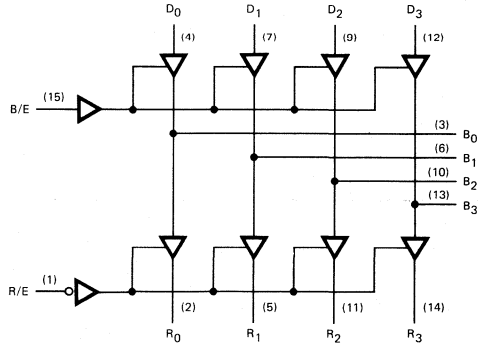
LOGIC DIAGRAMS

Am8T26A
Inverting Output (Three-State)



LIC-562

Am8T28
Non-Inverting Output (Three-State)

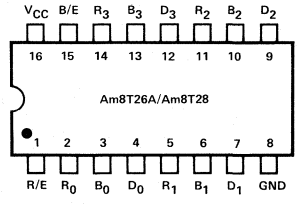


LIC-563

ORDERING INFORMATION

Package Type	Temperature Range	Am8T26A Order Number	Am8T28 Order Number
Molded DIP	0°C to +75°C	N8T26AB	N8T28B
Hermetic DIP	0°C to +75°C	N8T26AF	N8T28F
Dice	0°C to +75°C	AM8T26AXC	AM8T28XC
Hermetic DIP	−55°C to +125°C	S8T26AF	S8T28F
Dice	−55°C to +125°C	AM8T26AXM	AM8T28XM

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.

LIC-564

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Receiver)	30mA
DC Output Current, Into Outputs (BUS)	80mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

M8T26A, N8T28 $T_A = 0°C$ to $+75°C$ (COM'L) MIN. = 4.75V MAX. = 5.25V

S8T26A, S8T28 $T_A = -55°C$ to $+125°C$ (MIL) MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description		Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
Driver							
I_{IL}	Low Level Input Current		$V_{IN} = 0.4V$			−200	μA
I_{IL}	Low Level Input Current (Disabled)		$V_{IN} = 0.4V$			−50	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)		$V_{IN} = V_{CC}$MAX.			25	μA
V_{OL}	Low Level Output Voltage		$I_{OUT} = 48mA$ (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage		$I_{OUT} = -10mA$, $V_{CC} = V_{CC}$MIN. (Note 6)	2.4			Volts
I_{OS}	Short Circuit Output Current		$V_{OUT} = 0V$, $V_{CC} = V_{CC}$MAX. (Note 4)	−50		−150	mA
Receiver							
I_{IL}	Low Level Input Current		$V_{IN} = 0.4V$			−200	μA
I_{IH}	High Level Input Current (R_E)		$V_{IN} = V_{CC}$MAX.			25	μA
V_{OL}	Low Level Output Voltage		$I_{OUT} = 20mA$ (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage		$I_{OUT} = -100μA$, $V_{CC} = 5.0V$	3.5			Volts
			$I_{OUT} = -2.0mA$ (Note 6)	2.4			
I_{OS}	Short Circuit Output Current		$V_{OUT} = 0V$, $V_{CC} = V_{CC}$MAX.	−30		−75	mA
Both Driver and Receiver							
V_{TL}	Low Level Input Threshold Voltage			0.85			Volts
V_{TH}	High Level Input Threshold Voltage					2.0	Volts
I_O	Low Level Output Off Leakage Current		$V_{OUT} = 0.5V$			−100	μA
	High Level Output Off Leakage Current		$V_{OUT} = 2.4V$			100	μA
V_I	Input Clamp Voltage		$I_{IN} = -12mA$			−1.0	Volts
P_{WR}/I_{CC}	Power/Current Consumption	Am8T26A	$V_{CC} = V_{CC}$MAX.			457/87	mW/mA
		Am8T28	$V_{CC} = V_{CC}$MAX.			578/110	

Switching Characteristics ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Am8T26A Min.	Am8T26A Typ.	Am8T26A Max.	Am8T28 Min.	Am8T28 Typ.	Am8T28 Max.	Units
t_{PLH}	Driver Input to Bus	Figure 1		10	14		13	17	ns
t_{PHL}				10	14		13	17	
t_{PLH}	Bus to Receiver Output	Figure 2		9.0	14		12	17	ns
t_{PHL}				6.0	14		9.0	17	
t_{ZL}	Driver Enable to Bus	Figure 3		19	25		21	28	ns
t_{LZ}				15	20		18	23	
t_{ZL}	Receiver Enable to Receiver Output	Figure 4		15	20		18	23	ns
t_{LZ}				10	15		13	18	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Output sink current is supplied through a resistor to V_{CC}.
6. Measurements apply to each output and the associated data input independently.

DEFINITION OF FUNCTIONAL TERMS

D_0, D_1, D_2, D_3 The four driver inputs.

B_0, B_1, B_2, B_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

B/E Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

R/E Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	LOW Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
R/E	1	1/8	–	–
R_0	2	–	50	10
B_0	3	1/16	250	25
D_0	4	1/8	–	–
R_1	5	–	50	10
B_1	6	1/16	250	25
D_1	7	1/8	–	–
GND	8	–	–	–
D_2	9	1/8	–	–
B_2	10	1/16	250	25
R_2	11	–	50	10
D_3	12	1/8	–	–
B_3	13	1/16	250	25
R_3	14	–	50	10
B/E	15	1/8	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as −1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

DRIVER FUNCTION TABLE

INPUTS		Am8T26A OUTPUT	Am8T28 OUTPUT
B/E	D_i	B_i	B_i
L	X	Z	Z
H	L	H	L
H	H	L	H

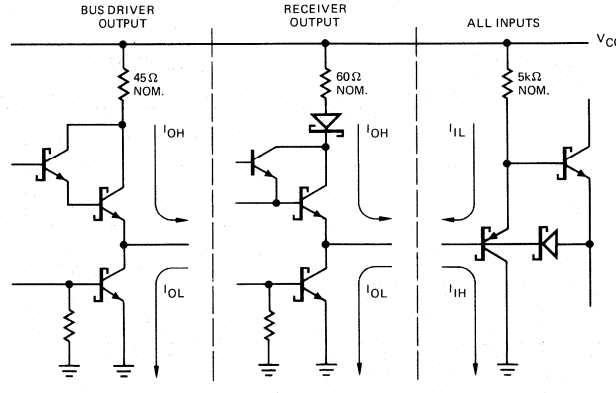
L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

RECEIVER FUNCTION TABLE

INPUTS		Am8T26A OUTPUT	Am8T28 OUTPUT
R/E	B_i	R_i	R_i
H	X	Z	Z
L	L	H	L
L	H	L	H

L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

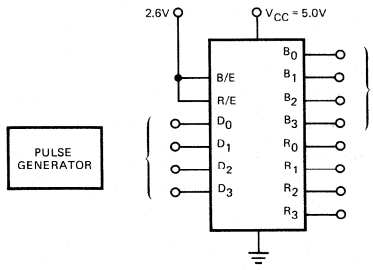


Note: Actual current flow direction shown.

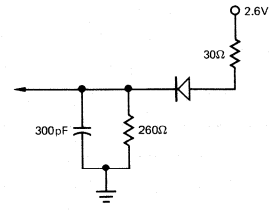
LIC-565

AC TEST CIRCUITS AND WAVEFORMS

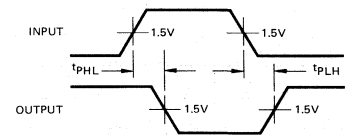
PROPAGATION DELAY (Data In to Bus)



LIC-566



LIC-567

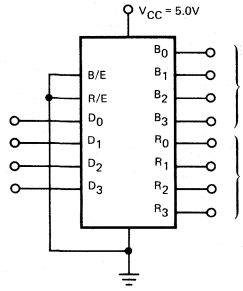


INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

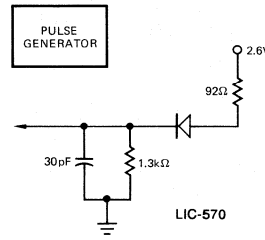
LIC-568

Figure 1

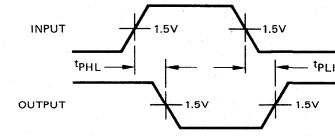
PROPAGATION DELAY (Bus to Receiver Out)



LIC-569



LIC-570

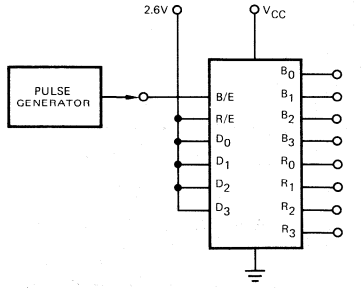


INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

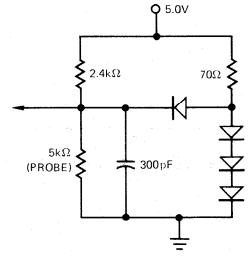
LIC-571

Figure 2

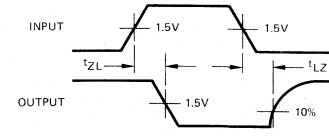
PROPAGATION DELAY (Bus Enable to Bus Output)



LIC-572



LIC-573

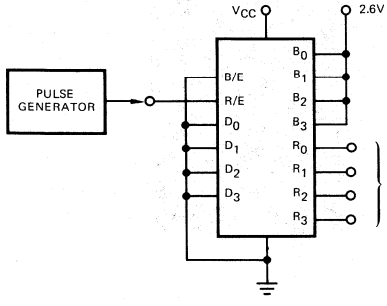


INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% duty cycle)
Amplitude = 2.6V

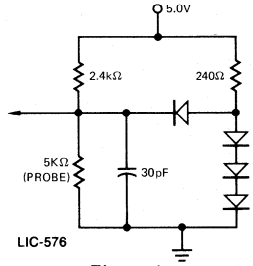
LIC-574

Figure 3

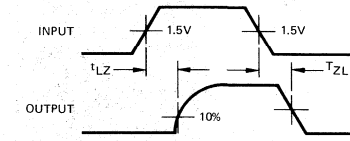
PROPAGATION DELAY (Receive Enable to Receive Output)



LIC-575



LIC-576



INPUT PULSE
$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% duty cycle)
Amplitude = 2.6V

LIC-577

Figure 4

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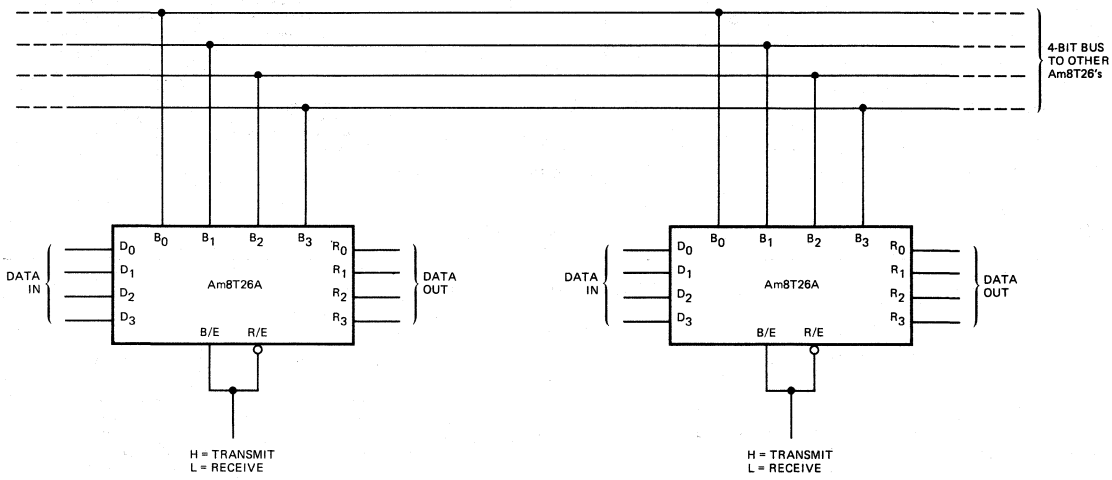
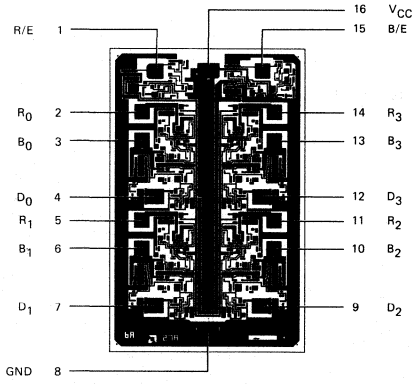
APPLICATION



LIC-578

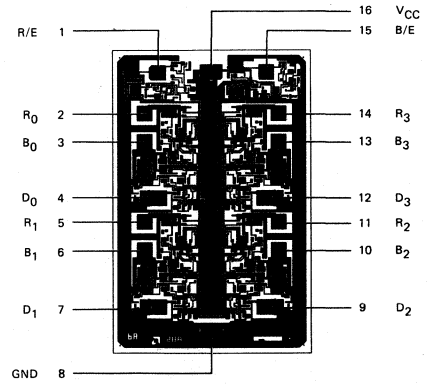
Metallization and Pad Layouts

Am8T26A



DIE SIZE 0.058" X 0.091"

Am8T28



DIE SIZE 0.058" X 0.091"

Am93S10 • Am93S16

BCD Decade/Four-Bit Binary Counters

istinctive Characteristics

Fully synchronous counting

Fully synchronous parallel loading

- Edge-triggered clock action
- Advanced Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883.

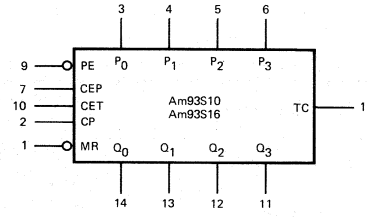
FUNCTIONAL DESCRIPTION

The Am93S10 and Am93S16 are fully synchronous 4-bit decimal and binary counters. With the parallel enable ($\overline{PE}$) LOW, data on the P_0-P_3 inputs is parallel loaded on the positive clock transition. When $\overline{PE}$ is HIGH and both count enables CEP and CET are also HIGH, counting will occur on the LOW-to-HIGH clock transition.

The terminal count state (1001 for the Am93S10 and 1111 for the Am93S16) is decoded and ANDed with CET in the terminal count (TC) output. If CET is HIGH and the counter is in its terminal count state, then TC is HIGH.

Both counters have an asynchronous master reset ($\overline{MR}$). A LOW on the $\overline{MR}$ input forces the Q outputs LOW independent of all other inputs. The only requirements on the $\overline{PE}$, CEP, CET and P_0-P_3 inputs is that they meet the set-up time requirements before the clock LOW-to-HIGH transition.

LOGIC SYMBOL

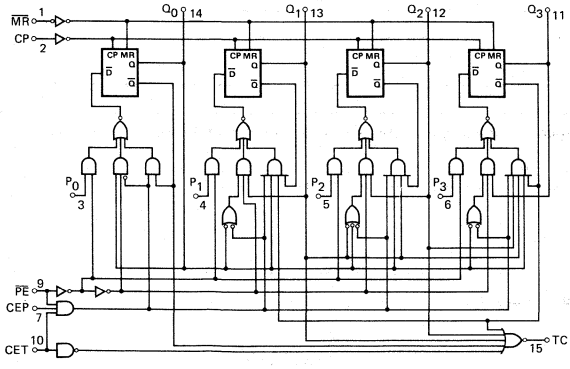


V_{CC} = Pin 16

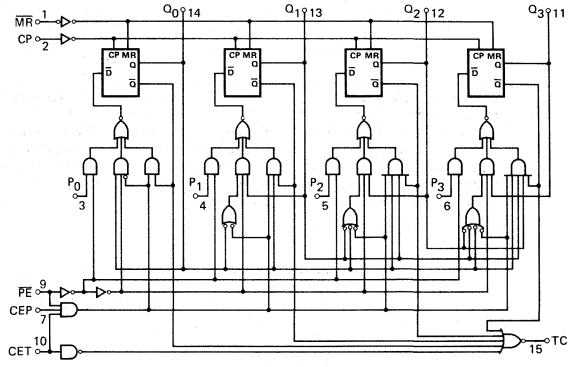
GND = Pin 8

LOGIC DIAGRAMS

Am93S10



Am93S16

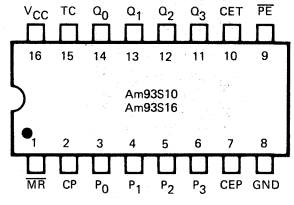


ORDERING INFORMATION

Package Type	Temperature Range	Am93S10 Order Number	Am93S16 Order Number
Molded DIP	0°C to +75°C	93S10PC	93S16PC
Hermetic DIP	0°C to +75°C	93S10DC	93S16DC
Dice	0°C to +75°C	93S10XC	93S16XC
Hermetic DIP	−55°C to +125°C	93S10DM	93S16DM
Hermetic Flat Pak	−55°C to +125°C	93S10FM	93S16FM
Dice	−55°C to +125°C	93S10XM	93S16XM

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} ma:
DC Input Voltage	−0.5V to +5.5
DC Output Current, Into Outputs	30m
DC Input Current	−30mA to +5.0m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

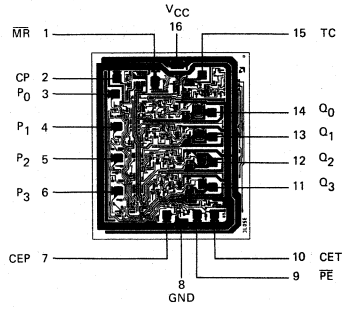
Am93S10XC, Am93S16XC	T_A = 0°C to 75°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am93S10XM, Am93S16XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	XM	2.5	3.4		Volts
			XC	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}			0.35	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	P; MR; CEP			−2.0	mA
			CET			−3.0	
			$\overline{PE}$			−4.0	
			CP			−5.0	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	P; $\overline{MR}$; CEP			50	µA
			CET			75	
			$\overline{PE}$			100	
			CP			125	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−40	−65	−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			82	127	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; $\overline{MR}$ = 0V; all other inputs HIGH.

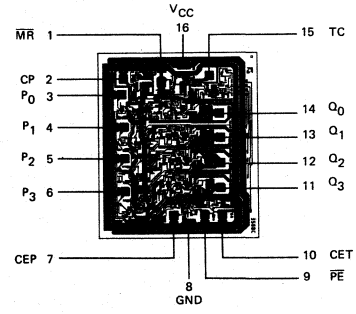
Metallization and Pad Layouts

Am93S10



DIE SIZE 0.078" X 0.096"

Am93S16



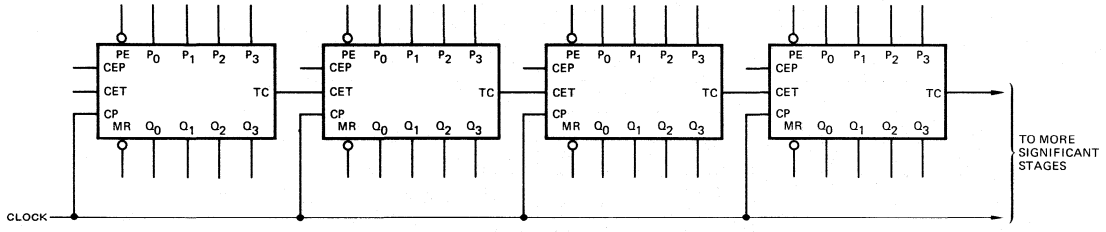
DIE SIZE 0.078" X 0.096"

SWITCHING CHARACTERISTICS (T_A = +25°)

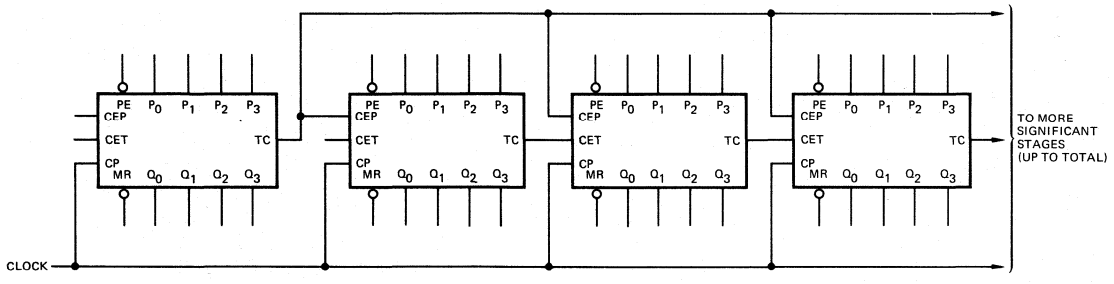
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Count Frequency	V_{CC} = 5.0V, C_L = 15 pF, R_L = 280Ω	70	100		MHz
t_{PLH}	Clock to Q			6	9	ns
t_{PHL}				8.5	13	
t_{PLH}	Clock to TC			12	18	ns
t_{PHL}				8	12	
t_{PLH}	CET to TC			6.5	10	ns
t_{PHL}				6.5	10	
t_{PHL}	$\overline{MR}$ to Q			14	20	ns
t_s	Recovery Time for MR (inactive)		6			ns
t_{pw}	Master Reset Pulse Width		13			ns
t_{pw}	Clock Pulse Width HIGH		6			ns
	Clock Pulse Width LOW		10			
t_s	Data to Clock		8			ns
t_h			0			
t_s	$\overline{PE}$ to Clock		16			ns
t_h			0			
t_s	CEP or CET to Clock		12			ns
t_h			0			

APPLICATIONS

SYNCHRONOUS MULTISTAGE COUNTING USING CET INPUT ONLY



FASTER SYNCHRONOUS MULTISTAGE COUNTING USING CET AND CEP INPUTS



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DEFINITION OF FUNCTIONAL TERMS

$\overline{PE}$ Parallel Enable. When $\overline{PE}$ is LOW, the parallel inputs, P_0 through P_3, are enabled. When $\overline{PE}$ is HIGH, the count function is possible.

CEP Count Enable Parallel. CEP is one of the count enable inputs that must be HIGH for the counter to count.

CET Count Enable Trickle. CET is one of the count enable inputs that must be HIGH for the counter to count. In addition, CET is included in the TC output gate and must be HIGH for TC to be HIGH.

CP Clock Pulse. Causes the required output change on the LOW-to-HIGH transition (Edge-triggered).

$\overline{MR}$ Master Reset. When the asynchronous master reset is LOW, the Q_0 through Q_3 outputs will be LOW regardless of the other inputs.

P_0, P_1, P_2, P_3 The parallel data inputs for the four internal flip-flops.

Q_0, Q_1, Q_2, Q_3 The four parallel outputs from the counter.

TC Terminal Count. The terminal count output will be HIGH for CET HIGH and binary nine on the Am93S10 or CET HIGH and binary 15 on the Am93S16.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{MR}$	1	1	–	–
CP	2	2.5	–	–
P_0	3	1	–	–
P_1	4	1	–	–
P_2	5	1	–	–
P_3	6	1	–	–
CEP	7	1	–	–
GND	8	–	–	–
$\overline{PE}$	9	2	–	–
CET	10	1.5	–	–
Q_3	11	–	20	10
Q_2	12	–	20	10
Q_1	13	–	20	10
Q_0	14	–	20	10
TC	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

FUNCTION TABLE

INPUTS									OUTPUTS			
CP	$\overline{MR}$	$\overline{PE}$	CEP	CET	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3
X	L	X	X	X	X	X	X	X	L	L	L	L
↑	H	L	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
↑	H	H	L	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	L	H	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	H	X	X	X	X	COUNT			

H = HIGH
L = LOW
X = Don't Care

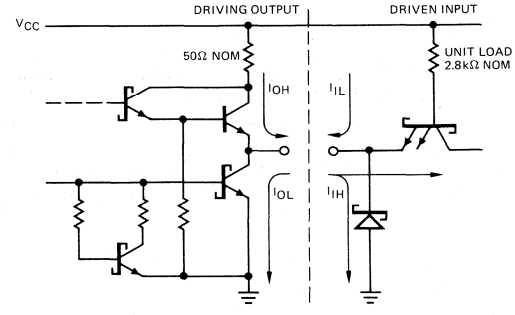
NC = No Change
D_i may be either HIGH or LOW
↑ LOW-to-HIGH Transition

TERMINAL COUNT (TC) TRUTH TABLE

Am93S10					Am93S16					TC
CET	Q_0	Q_1	Q_2	Q_3	CET	Q_0	Q_1	Q_2	Q_3	
H	H	L	L	H	H	H	H	H	H	H
L	X	X	X	X	L	X	X	X	X	L
X	L	X	X	X	X	L	X	X	X	L
X	X	H	X	X	X	X	L	X	X	L
X	X	X	H	X	X	X	X	L	X	L
X	X	X	X	L	X	X	X	X	L	L

H = HIGH
L = LOW
X = Don't Care

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am93S48

Twelve-Input Parity Checker/Generator

Distinctive Characteristics

Generates or checks parity over 12 bits

Advanced Schottky technology

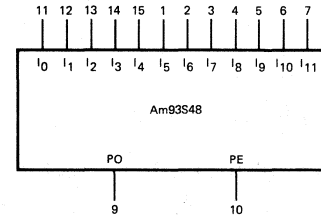
- Same delay to EVEN and ODD parity outputs
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am93S48 is a high-speed, 12-input parity checker or parity generator. The device is built using advanced Schottky technology and also incorporates PNP input transistors to reduce the input loading to only 0.4 STTL Unit Loads.

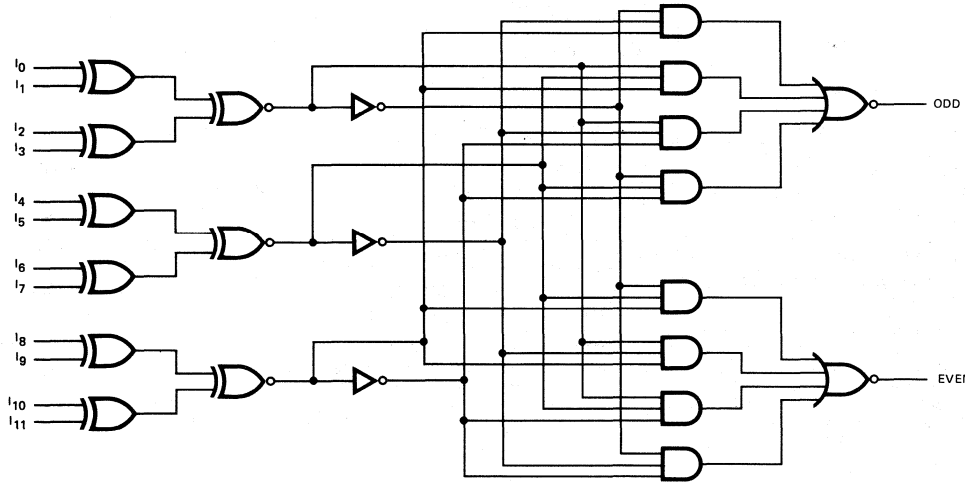
Both an ODD parity output and an EVEN parity output are obtained with the same propagation delay. This is accomplished by using an output structure that looks at the input as three 4-bit parity trees.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

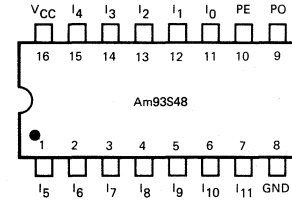
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	93S48PC
Hermetic DIP	0°C to +70°C	93S48DC
Dice	0°C to +70°C	93S48XC
Hermetic DIP	−55°C to +125°C	93S48DM
Hermetic Flat Pak	−55°C to +125°C	93S48FM
Dice	−55°C to +125°C	93S48XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} ma
DC Input Voltage	−0.5V to +5.5
DC Output Current, Into Outputs	30m
DC Input Current	−30mA to +5.0m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93S48XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am93S48XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	XC XM	2.7 2.5			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−0.8	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			57	80	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Both outputs open; all inputs at 4.5V.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	I_0 through I_{11} to Even Output	V_{CC} = 5.0V, C_L = 15 pF, R_L = 280Ω		19	28	ns
t_{PHL}				19	28	ns
t_{PLH}	I_0 through I_{11} to Odd Output			19	28	ns
t_{PHL}				19	28	ns

TRUTH TABLE

NUMBER OF I INPUTS		OUTPUT	
LOW	HIGH	ODD	EVEN
0	12	L	H
1	11	H	L
2	10	L	H
3	9	H	L
4	8	L	H
5	7	H	L
6	6	L	H
7	5	H	L
8	4	L	H
9	3	H	L
10	2	L	H
11	1	H	L
12	0	L	H

H = HIGH
L = LOW
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
I_5	1	0.4	–	–
I_6	2	0.4	–	–
I_7	3	0.4	–	–
I_8	4	0.4	–	–
I_9	5	0.4	–	–
I_{10}	6	0.4	–	–
I_{11}	7	0.4	–	–
GND	8	–	–	–
PO	9	–	20	10
PE	10	–	20	10
I_0	11	0.4	–	–
I_1	12	0.4	–	–
I_2	13	0.4	–	–
I_3	14	0.4	–	–
I_4	15	0.4	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS

I_0 through I_{11} The twelve inputs to the parity tree.

ODD The ODD parity output of the device. When an ODD number of I inputs are at a HIGH level, the ODD output will be HIGH.

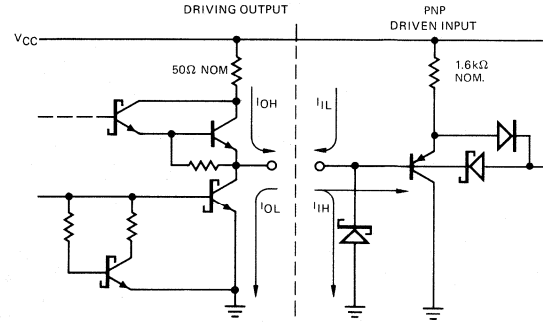
EVEN The EVEN parity output of the device. When an EVEN number of I inputs are at a HIGH level, the EVEN output will be HIGH.

LOGIC EQUATIONS

Odd Output = $I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$

Even Output = $\overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

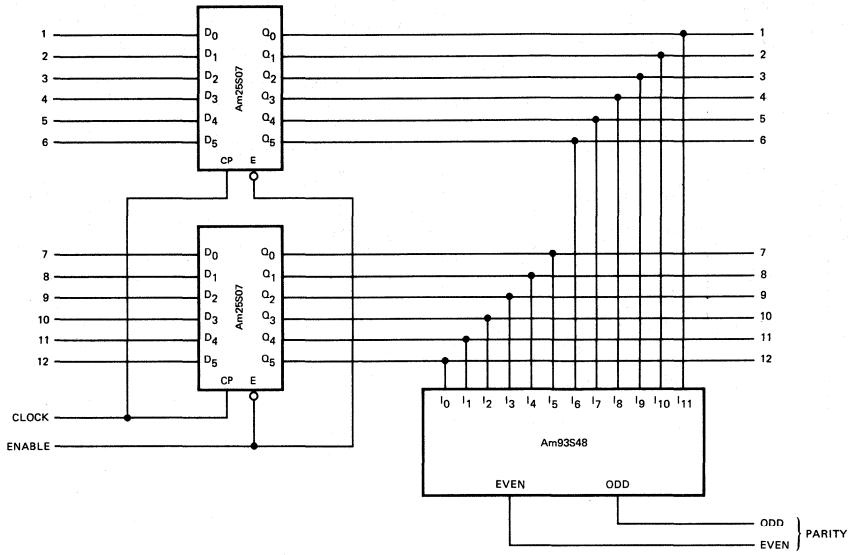


Note: Actual current flow direction shown.

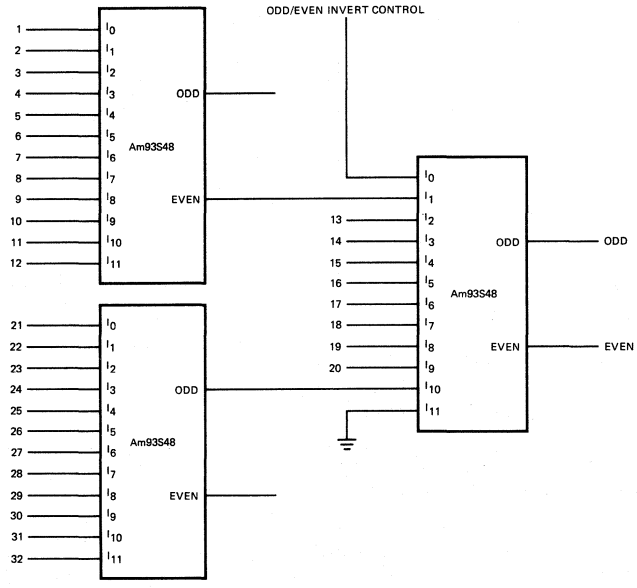
12

APPLICATIONS

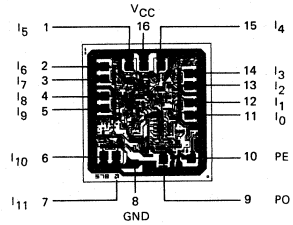
12-BIT PARALLEL ODD/EVEN PARITY CHECKER/GENERATOR



32-BIT PARITY CHECKER/GENERATOR



Metallization and Pad Layout



DIE SIZE 0.067" X 0.072"

General Information

Advanced Micro Devices Commitment to Excellence

Product Assurance Programs for Military and Commercial Integrated Circuits

13

A COMMITMENT TO EXCELLENCE

Advanced Micro Devices was conceived on the premise that there was a place in the semiconductor community for a manufacturer dedicated to excellence.

In product assurance procedures, Advanced Micro Devices is unique. Only Advanced Micro Devices processes all integrated circuits, commercial as well as military, to the demanding requirements of MIL-STD-883. The Rome Air Development Center (RADC), which is the Air Force's principal authority on component reliability, has issued MIL-HDBK-217B which indicates that parts processed to Military Standard 883, Level C (Advanced Micro Devices' standard processing) yield a product nearly ten times better in failure rates than the industry commercial average.

Our Sunnyvale facility has been certified by the Defense Electronics Supply Center (DESC) to produce parts to JAN Class B and C under Military Specification MIL-M-38510. The National Aeronautics and Space Administration (NASA) has certified this production line for the manufacture of Class A products for programs requiring the highest levels of reliability. Advanced Micro Devices is the only integrated circuit company formed within the last ten years to achieve such line certification.

This brochure outlines Advanced Micro Devices' standard programs for Class B, C and A devices for military and commercial operating range applications. These will cover the majority of system requirements today. Alternative screening flows for specific user needs can be performed on request. Check with your local sales office for further information.

ADVANCED MICRO DEVICES' STANDARD PRODUCTS ARE MANUFACTURED TO MIL-STD-883 REQUIREMENTS

Advanced Micro Devices' product assurance programs are based on two key documents.

MIL-M-38510 – General Specification for Microcircuits

MIL-STD-883 – Test Methods and Procedures for Microelectronics

The screening charts in this brochure show that every integrated circuit shipped by Advanced Micro Devices receives the critical screening procedures defined in MIL-STD-883, Method 5004 for Class C product. This includes molded plastic devices.

In addition, documentation, design, processing and assembly workmanship guidelines are patterned after MIL-M-38510 specifications.

Commercial and industrial users receive the quality and reliability benefits of this aerospace-type screening and documentation at no additional cost.

STANDARD PRODUCT TESTING CATEGORIES

Advanced Micro Devices offers integrated circuits to three standard testing categories.

1. Commercial operating range product (typically 0 to 70°C)
2. Military operating range product (typically −55 to +125°C)
3. JAN qualified product

Categories 1 and 2 are available on most Advanced Micro Devices circuits. Category 3 is offered on a more limited line. Additional testing and screening services are available to special order. Check with your local sales office for details.

STANDARD PRODUCT ASSURANCE CATEGORIES

Devices produced to the above testing categories are available to the three standard classes of product assurance defined by MIL-STD-883. As a minimum, every device shipped by Advanced Micro Devices meets the screening requirements of Class C.

Class C – For commercial and ground-based military systems where replacement can be accomplished without difficulty.

According to MIL-HDBK-217B, this assures relative failure rates 9.4 times better than that of regular industry commercial product.

Class B – For flight applications and commercial systems where maintenance is difficult or expensive and where reliablity is vital.

Devices are upgraded from Class C to Class B by burn-in screening and additional testing.

According to MIL-HDBK-217B, Class B failure rate is improved 30 times over regular industry commercial product. Advanced Micro Devices Class B processing conforms to MIL-STD-883 requirements. MIL-HDBK-217B indicates that this may provide failure rates as much as two times better than some other manufacturers' "equivalent" or "pseudo" Class B programs.

Class S – For space applications where replacement is extremely difficult or impossible and reliability is imperative.

Class S screening includes x-ray and other special inspections tailored to the specific requirements of the user.

The 100% screening and quality conformance testing performed within these Advanced Micro Devices' programs is shown in TABLES I, II and III. A full description of the process flow is provided in Product Assurance Document 15-010, available on request.

CLASS C SCREENING FLOW FOR COMMERCIAL SYSTEMS AND GROUND BASED MILITARY SYSTEMS

TABLE I
CLASS C
INTEGRATED CIRCUITS

		COMMERCIAL OPERATING RANGE	MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES	HERMETIC PACKAGE ONLY	
Screening Procedure per MIL-STD-883 Method 5004, Class C		Flow C1	Flow C3	Flow C4
Screen	Test Method	Commercial Product	Military Product	Jan Qualified Product
VISUAL AND MECHANICAL				
Internal visual	2010, Condition B	100%	100%	100%
High temperature storage	1008, Condition C, 24 hours	100%	100%	100%
Temperature cycle	1010, Condition C	100%	100%	100%
Constant acceleration	2001	100% (1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (1)	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(2)	–	–
Functional	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(2)	–	–
Switching (ac) or Dynamic	At 25°C, nominal power supply	(2)	–	–
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample
Sample Tests	Group B	–	–	Sample
	Group C	–	–	Sample
	Group D	–	–	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%

TABLE II
GROUP A QUALITY CONFORMANCE LEVELS

Advanced Micro Devices employs the military-recommended LTPD sampling system to assure quality. MIL-STD-883, Method 5005, TABLE I, Group A, subgroups 1 through 9 as appropriate to the device family are performed on every lot. Quality levels defined for Class B product are applied by Advanced Micro Devices to both Class B and Class C orders.

	LTPD	INITIAL SAMPLE SIZE
Subgroup 1 – Static tests at 25°C	5	45
Subgroup 2 – Static tests at maximum rated operating temperature	7	32
Subgroup 3 – Static tests at minimum rated operating temperature	7	32
Subgroup 4 – Dynamic tests at 25°C – LINEAR devices	5	45
Subgroup 5 – Dynamic tests at maximum rated operating temperature – LINEAR devices	7	32
Subgroup 6 – Dynamic tests at minimum rated operating temperature – LINEAR devices	7	32
Subgroup 7 – Functional tests at 25°C	5	45
Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 – Switching tests at 25°C – DIGITAL devices	7	32
Subgroup 10 – Switching tests at maximum rated operating temperatures – DIGITAL devices	*	
Subgroup 11 – Switching tests at minimum rated operating temperatures – DIGITAL devices	*	

*These subgroups, where applicable, are usually performed during initial characterization only for all except JAN Qualified product.

CLASS B SCREENING FLOW FOR HIGH RELIABILITY COMMERCIAL AND MILITARY SYSTEMS

TABLE III
CLASS B
INTEGRATED CIRCUITS
(Class C plus burn in screening and additional testing.)

Screening Procedure per MIL-STD-883 Method 5004, Class B		COMMERCIAL OPERATING RANGE	MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES	HERMETIC PACKAGE ONLY	
Screen	Test Method	Flow B1 Commercial Product	Flow B3 Military Product	Flow B4 Jan Qualified Product
VISUAL AND MECHANICAL				
Internal visual	2010, Condition B	100%	100%	100%
High temperature storage	1008, Condition C, 24 hours	100%	100%	100%
Temperature cycle	1010, Condition C	100%	100%	100%
Constant acceleration	2001	100% (1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (1)	100%	100%
BURN IN				
Interim (pre burn in) electricals	Per applicable device specification	100%	100%	100%
Burn in	1015, 160 hours at 125°C or equivalent.*	100% (3)	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(2) (3)	100%	100%
Functional	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(2) (3)	100%	100%
Switching (ac) or Dynamic	At 25°C, nominal power supply	(2)	100%	100%
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample
Sample Tests	Group B	–	(4)	Sample
	Group C	–	(4)	Sample
	Group D	–	(4)	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%

Notes: 1. Not applicable to molded packages.
2. All MOS RAMs and many other MOS devices receive a.c. testing and 100% d.c. screening at high temperature and power supply extremes as standard. Other products sampled at Group A (Table II).
3. Am2900 LSI products receive a 96 hour burn-in, plus 100% d.c. screening at high temperature and power supply extremes.
4. Unless device data sheet specifies different limits.
5. Without optical aid for commercial devices.

*(Unless device data sheet specifies otherwise).

CLASS S
FOR AEROSPACE SYSTEMS. (FORMERLY CLASS A)

Advanced Micro Devices offers Class S programs based on screening defined in MIL-STD-883, Method 5004. Contact your local Advanced Micro Devices' sales office for more information.

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Table IV – Class S Screening Flow

Screening Procedure Class S		MILITARY OPERATING RANGE HERMETIC PACKAGE ONLY	MILITARY OPERATING RANGE HERMETIC PACKAGE ONLY
Screen	**Test Method**	**Flow S1 Basic S Flow**	**Flow S2 Extended Class S Processing**
SEM			Contact Advanced Micro Devices Sales for Details
Scanning Electron Microscope	2018	Wafer Lot Sample	
ASSEMBLY			
Class S Process Monitors		Periodic sampling	
VISUAL AND MECHANICAL			
Internal Visual	2010, Condition A	100%	
High Temperature Storage	1008, Condition C, 24 hours	100%	
Temperature Cycle	1010, Condition C	100%	
Constant Acceleration	2001, Condition E	100%	
PIND			
Particle Impact Noise Detection	2020, Condition A or B	100% (Note 1)	
Serialization		100%	
X-RAY			
Radiographic	2012, Two views	100%	
BURN-IN			
Interim (Pre Burn-in) Electricals	Per applicable device specification	100% (Note 2)	
Burn-in	1015, 240 hours at 125°C or equivalent	100% (Note 3)	
Interim (Post Burn-in) Electricals	Per applicable device specification	100% (Note 2)	
FINAL ELECTRICAL TESTS		AMD Data Sheet	
Static (dc)	a) At 25°C, and power supply extremes	100%	
	b) At temperature and power supply extremes	100%	
Functional	a) At 25°C and power supply extremes	100%	
	b) At temperature and power supply extremes	100%	
Switching (ac) or Dynamic	At 25°C nominal power supply	100%	
SEAL			
Hermeticity, Fine and Gross	1014	100%	
QUALITY CONFORMANCE			
	5005, Group A (See Table II)	Sample	
Sample Tests	Group B	Sample (Note 4)	
	Group D	Sample (Note 4)	
EXTERNAL VISUAL	2009	100%	

Notes: 1. 100% screen, one pass.
2. Read and record requirements to be specified as applicable to particular device type.
3. Consult device data sheet.
4. Available to special order.

STANDARD PRODUCT
SCREENING SUMMARY AND ORDERING INFORMATION

1. COMMERCIAL PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic and molded packages.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class C and Class B options.

Class C

- Order standard AMD part number.
- Marked same as order number.

Examples: AM25LS374DC, SN74LS374J

Class B

- Burn in performed in AMD circuit condition.
- Order standard AMD part number, add suffix B (or /883B for 1, 2 and 300 Series Linear devices).
- Marked same as order number.

Examples: AM25LS374DC-B, SN74LS374J-B

2. MILITARY PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic package only.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class B and Class C options.

Class C

- Order standard AMD part number.
- Marked same as order number.

Examples: AM25LS374DM, SN54LS374J

Class B

- Burn in performed in AMD circuit condition.
- AC at 25°C, d.c. and functional testing at 25°C as well as temperature and power supply extremes performed on 100% of every lot.
- Quality conformance testing, Method 5005, Groups B, C and D available to special order.
- Order standard AMD part number, add suffix B.
- Marked same as order number.

Examples: AM25LS374DM-B, SN54LS374J-B

3. JAN QUALIFIED PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested to JAN detail specification (slash sheet).
- Manufactured in Defense Logistics Agency certified facility.
- Quality conformance testing, Method 5005, Groups A, B, C and D performed as standard and must be completed prior to shipment.
- It is a product for which AMD has gained QPL listing.*

Class B (Flow B4)

- Burn in performed in circuit condition approved for JAN devices.
- Order per military document.
- Marked per military document.

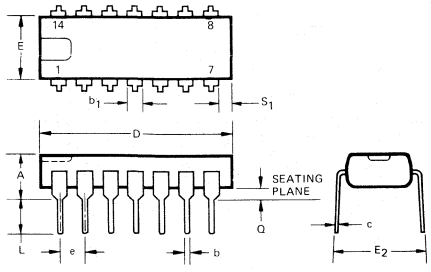
Example: JM38510/30106BEB

*In certain cases where JAN Qualified product is specified but is not available, Advanced Micro Devices can provide devices to the electrical limits and burn-in criteria of the slash sheet. This class of product has been called JAN Equivalent and marked M38510/ by some manufacturers. This identification is no longer permitted by DESC. Check with your local sales office for availability of specific device types.

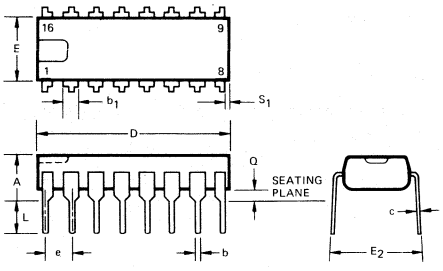
PACKAGE OUTLINES

MOLDED DUAL IN-LINE PACKAGES

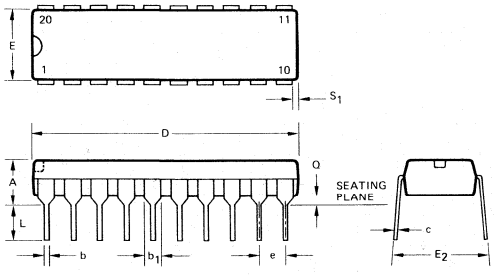
P-14-1



P-16-1



P-20-1



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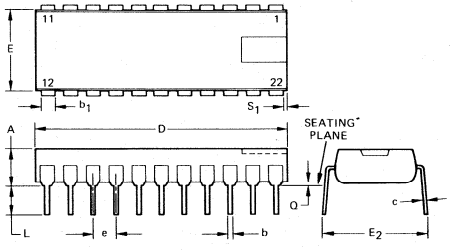
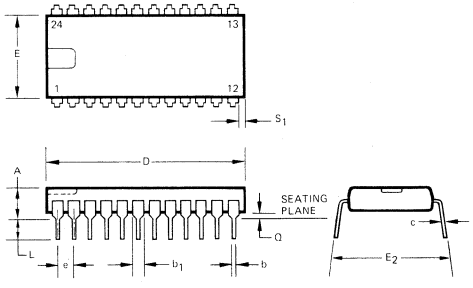


P-24-1



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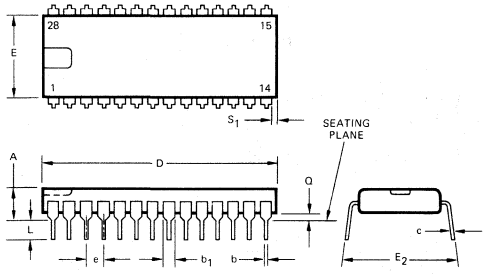
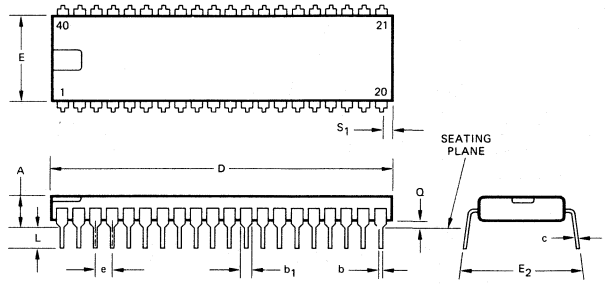
PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES (Cont.)

P-28-1



P-40-1



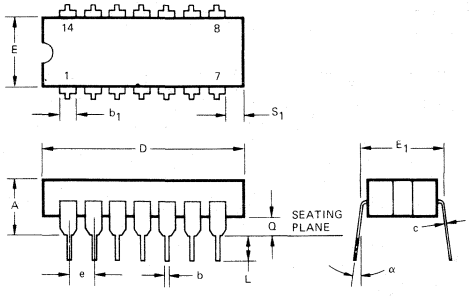
AMD Pkg.	P-14-1		P-16-1		P-20-1		P-22-1		P-24-1		P-28-1		P-40-1	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.150	.200	.150	.200	.150	.200	.150	.200	.170	.215	.150	.200	.150	.200
b	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020
b_1	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065
c	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011
D	.745	.775	.745	.775	1.010	1.050	1.080	1.120	1.240	1.270	1.450	1.480	2.050	2.080
E	.240	.260	.240	.260	.250	.290	.330	.370	.515	.540	.530	.550	.530	.550
E_2	.310	.385	.310	.385	.310	.385	.410	.480	.585	.700	.585	.700	.585	.700
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.125	.150	.125	.160	.125	.160	.125	.160	.125	.160
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S_1	.040	.065	.010	.040	.025	.055	.015	.045	.035	.065	.040	.070	.040	.070

Notes: 1. Standard lead finish is tin plate or solder dip.
2. Dimension E_2 is an outside measurement.

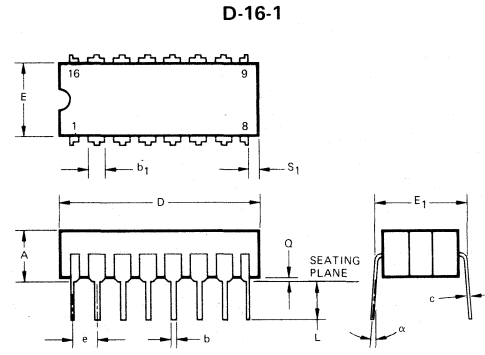
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES

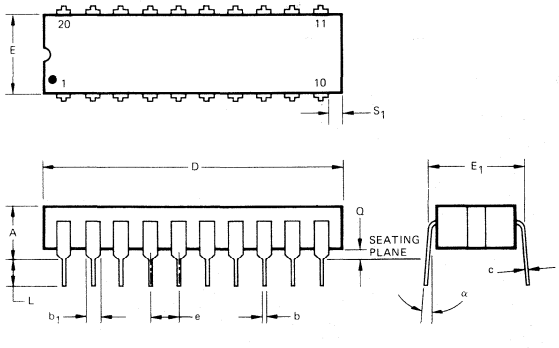
D-14-1



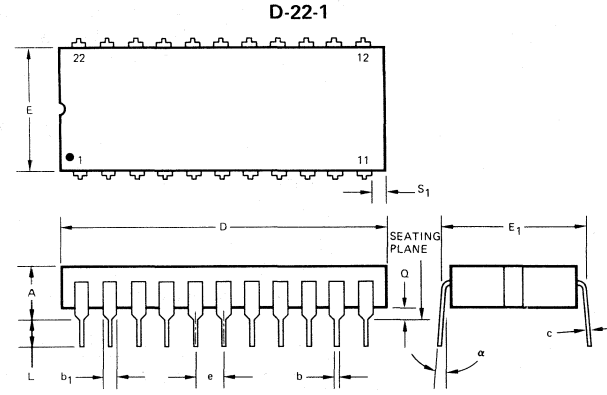
D-16-1



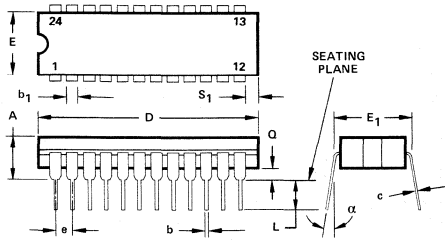
D-20-1



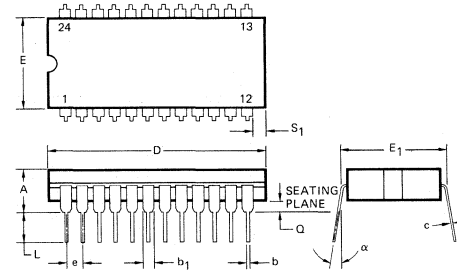
D-22-1



D-24-Slim



D-24-1 and D-24-4



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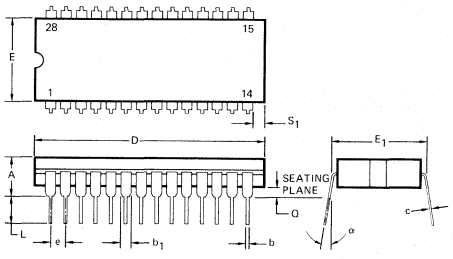
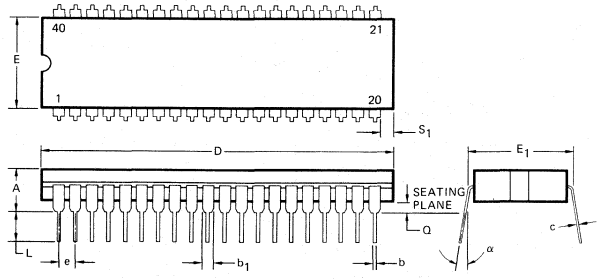
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

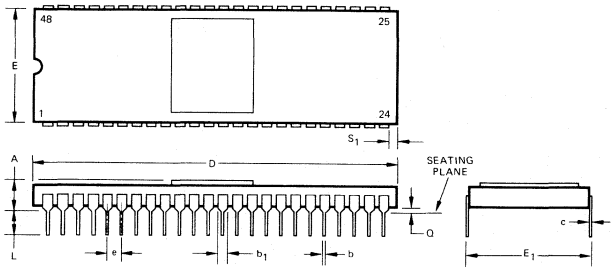
D-28-1



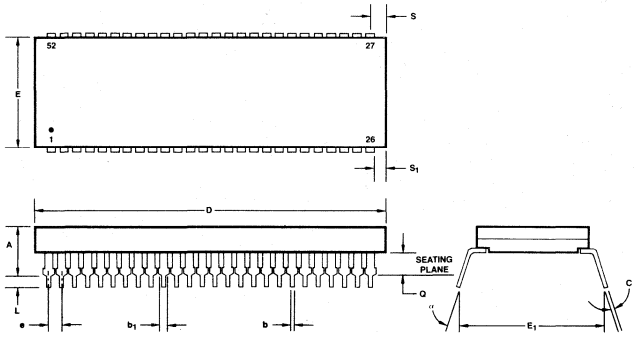
D-40-1



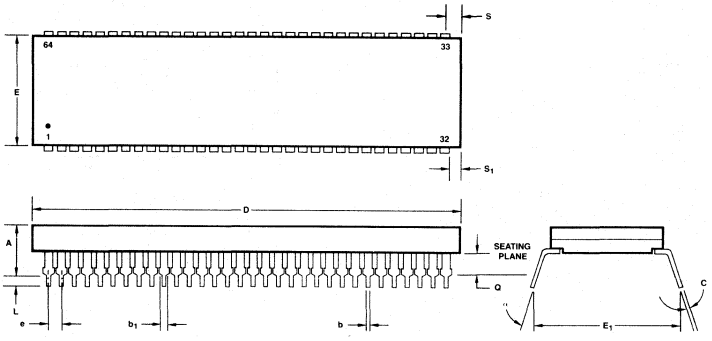
D-48-2



D-52-3



D-64-3



PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

AMD Pkg	D-14-1		D-16-1		D-20-1		D-22-1		D-24-Slim		D-24-1	
Common Name	CERDIP		CERDIP		CERDIP		CERDIP		CERDIP		CERDIP	
38510 Appendix C	D-1(1)		D-2(1)		–		–		–		D-3(1)	
Parameters	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	.130	.200	.130	.200	.140	.220	.140	.220	.140	.220	.150	.225
b	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020
b_1	.050	.070	.050	.070	.050	.070	.045	.065	.045	.065	.045	.065
c	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011
D	.745	.785	.745	.785	.935	.970	1.045	1.110	1.230	1.285	1.230	1.285
E	.240	.285	.240	.310	.245	.285	.360	.405	.245	.285	.510	.545
E_1	.290	.320	.290	.320	.290	.320	.390	.420	.290	.320	.600	.620
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.125	.150	.125	.150	.120	.150	.120	.150
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S_1	.010		.005		.005		.005		.010		.010	
α	3°	13°	3°	13°	3°	13°	3°	13°	3°	13°	3°	13°
Standard Lead Finish	b		b		b		b		b		b	

AMD Pkg	D-24-4/D-24-4*		D-28-1		D-40-1		D-48-2		D-52-3		D-64-3	
Common Name	CERVIEW		CERDIP		CERDIP		SIDE-BRAZED		TOP BRAZED		TOP BRAZED	
38510 Appendix C	–		–		D-5		–		–		–	
Parameters	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	.150	.225	.150	.225	.150	.225	.100	.200	.135	.450	.135	.450
b	.016	.020	.016	.020	.016	.020	.015	.022	.015	.022	.015	.022
b_1	.045	.065	.045	.065	.045	.065	.030	.060	.030	.060	.030	.060
c	.009	.011	.009	.011	.009	.011	.008	.013	.008	.013	.008	.013
D	1.235	1.280	1.440	1.500	2.020	2.100	2.370	2.430	2.540	2.660	3.140	3.260
E	.510	.550	.510	.550	.510	.550	.570	.610	.775	.825	.775	.825
E_1	.600	.630	.600	.630	.600	.630	.590	.620	.880	.920	.880	.920
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.120	.150	.120	.150	.120	.150	.125	.160	.120	.160	.120	.160
Q	.015	.060	.015	.060	.015	.060	.020	.060	.040	.100	.040	.100
S*												.098
S_1**	.010		.005		.005		.005				.005	
α	3°	13°	3°	13°	3°	13°			0°	15°	0°	15°
Standard Lead Finish			b		b		b or c					

Notes: 1. Load finish b is tin plate. Finish c is gold plate.
2. Used only for LM108/LM108A.
3. Dimensions E and D allow for off-center lid, meniscus and glass overrun.

* From centerline of end lead.
** From edge of end lead.

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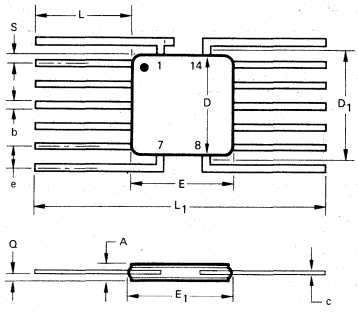
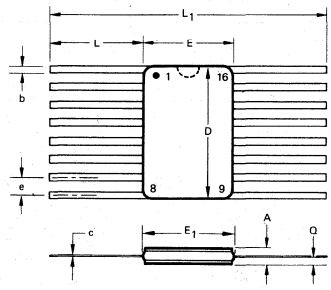
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES

F-14-1

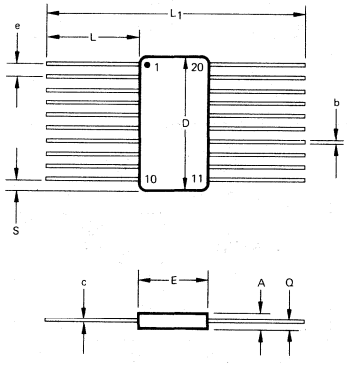


F-16-1

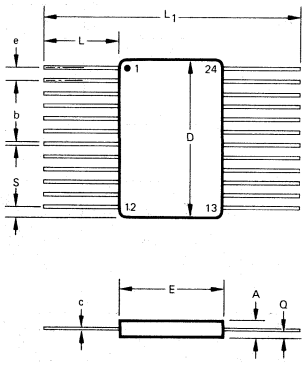


Note: Notch is pin 1 index on cerpack.

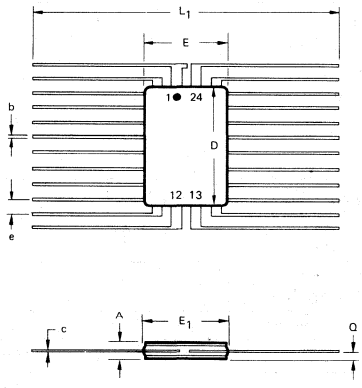
F-20-1



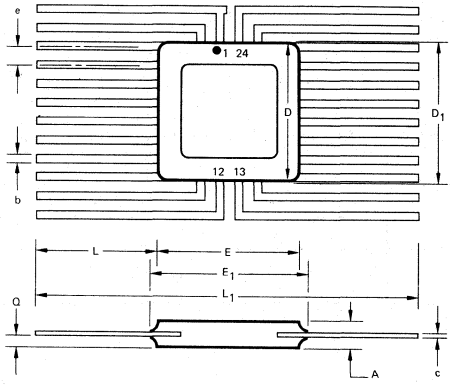
F-24-1



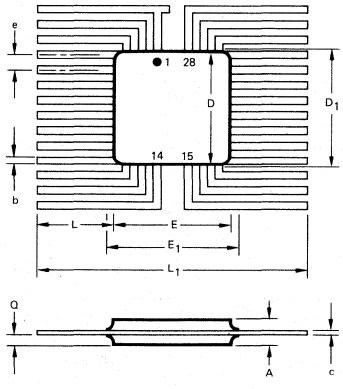
F-24-2



F-24-3



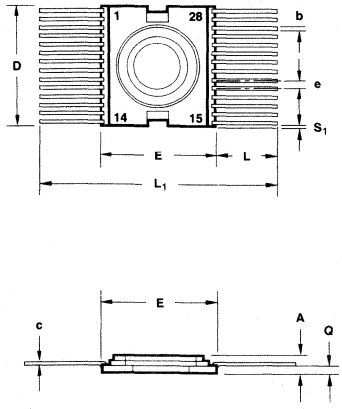
F-28-1



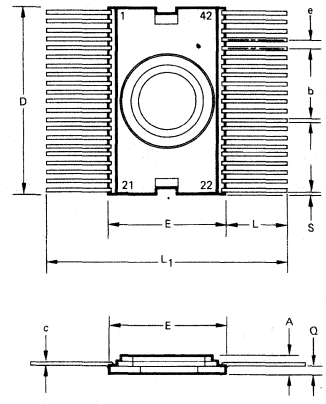
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES (Cont.)

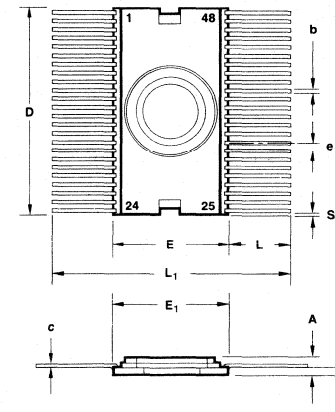
F-28-2



F-42-1



F-48-2



AMD Pkg.	F-14-1		F-16-1		F-20-1	
Common NAME	CERPACK		CERPACK		CERPACK	
38510 Appendix C	.F-1		F-5		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.
A	.045	.080	.045	.085	.045	.085
b	.015	.019	.015	.019	.015	.019
c	.004	.006	.004	.006	.004	.006
D	.230	.255	.370	.425	.490	.520
D_1						
E	.240	.260	.245	.285	.245	.285
E_1		.275		.290		.290
e	.045	.055	.045	.055	.045	.055
L	.300	.370	.300	.370	.300	.370
L_1	.920	.980	.920	.980	.920	.980
Q	.010	.040	.020	.040	.020	.040
S_1	.005		.005		.005	
Standard Lead Finish	b		b		b	

AMD Pkg.	F-24-1		F-24-2		F-24-3		F-28-1		F-28-2		F-42-1		F-48-2	
Common Name	CERPACK		METAL FLAT PAK		METAL FLAT PAK		METAL FLAT PAK		CERAMIC FLAT PAK		CERAMIC FLAT PAK		CERAMIC FLAT PAK	
38510 Appendix C	F-6		F-8		–		–		–		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.050	.090	.045	.090	.045	.090	.045	.080	.065	.085	.070	.115	.070	.110
b	.015	.019	.015	.019	.015	.019	.015	.019	.016	.025	.017	.023	.018	.022
c	.004	.006	.003	.006	.003	.006	.003	.006	.007	.010	.006	.012	.006	.010
D	.580	.620	.360	.410	.380	.420	.360	.410	.700	.720	1.030	1.090	1.175	1.250
D_1				.420		.440		.410		.720		1.090		1.250
E	.360	.385	.245	.285	.380	.420	.360	.410	.625	.650	.620	.660	.615	.670
E_1		.410		.305		.440		.410		.650		.660		.670
e	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055
L	.265	.320	.300	.370	.250	.320	.270	.320	.415	.435	.320	.370	.320	.370
L_1	.920	.980	.920	.980	.920	.980	.955	1.000	1.475	1.500	1.300	1.370	1.310	1.365
Q	.020	.040	.010	.040	.010	.040	.010	.040	.017	.025	.020	.060	.020	.055
S_1	.005		.005		0		0		.005		.005		.015	
Standard Lead Finish	b		c		c		c		c		c		c	

Notes: 1. Lead finish b is tin plate. Finish c is gold plate.
2. Dimensions E_1 and D_1 allow for off-center lid, meniscus, and glass overrun.

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ORDERING INFORMATION

All Advanced Micro Devices' products listed are stocked locally and distributed nationally by Franchised Distributors. See back of this book for the location nearest you. Please consult them for the latest price revisions. For direct factory orders, call Advanced Micro Devices, 901 Thompson Place, Sunnyvale, California 94086, (408) 732-2400, TWX: 910-339-9280, TELEX: 34-6306.

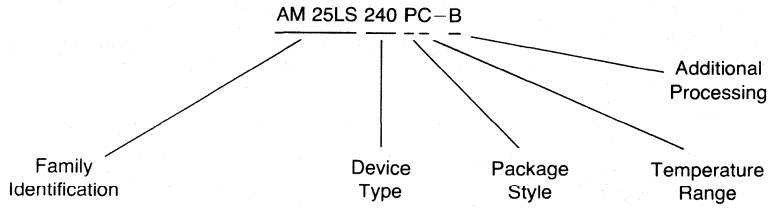
Minimum Order

The minimum direct factory order is $100.00 for a standard product.

The minimum direct factory order for Class B, burned-in, product is $250.00.

Proprietary Product Ordering, Package and Temperature Range Codes

The following scheme is used to identify Advanced Micro Devices' proprietary products.



Package Style

D = Hermetic DIP
F = Flat Package
P = Molded DIP
X = Dice

Temperature Range

C = Commercial
0°C to +70°C
M = Military
−55°C to +125°C

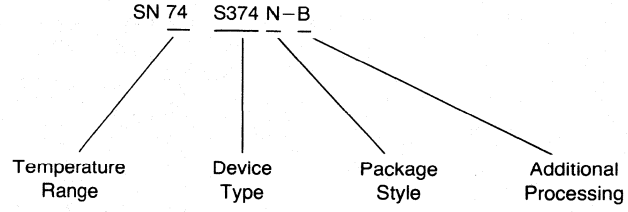
Additional Processing

B = Burn-in (Signifies full MIL-STD-883 Class B product for military temperature range devices)
T = Additional high temperature testing

Second Source Product Ordering, Package and Temperature Range Codes

An order number and marking system identical to the original manufacturer's is used for the Advanced Micro Devices' pin-for-pin and electrically equivalent circuit.

The following example is the ordering scheme for Advanced Micro Devices' second source to Texas Instruments' products.



Package Style

J = Hermetic DIP
N = Molded DIP
W = Flat Package
X = Dice

Temperature Range

74 = Commercial
0°C to +70°C
54 = Military
−55°C to +125°C

Additional Processing

B = Burn-in (Signifies full MIL-STD-883 Class B product for military temperature range devices)
T = Additional high temperature testing

SALES OFFICES

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Advanced Micro Devices
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El Segundo, California 90245
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Advanced Micro Devices
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Phoenix, Arizona 85021
Tel: (602) 242-4400

Advanced Micro Devices
4000 MacArthur Boulevard
Suite 5000
Newport Beach, California 92660
Tel: (714) 752-6262

Advanced Micro Devices
5955 Desoto Avenue, Suite 249
Woodland Hills, California 91367
Tel: (213) 992-4155

Advanced Micro Devices
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Suite 230
San Diego, California 92123
Tel: (714) 560-7030

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Tel: (315) 457-5400

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Tel: (914) 471-8180

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Willowdale, Ontario
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Tel: (416) 224-5193

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Advanced Micro Devices
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Suite 104C
St. Petersburg, Florida 33702
Tel: (813) 577-0754

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